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Second Edition

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Theory and Problems of

ELECTRONIC DEVICES AND CIRCUITS

Second Edition

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PREFACE

The subject matter of electronics may be divided into two broad categories: the application of physical properties of materials in the development of electronic control devices and the utilization of electronic control devices in circuit applications. The emphasis in this book is on the latter category, beginning with the terminal characteristics of electronic control devices. Other topics are dealt with only as necessary to an understanding of these terminal characteristics.

This book is designed to supplement the text for a first course in electronic circuits for engineers. It will also serve as a refresher for those who have previously taken a course in electronic circuits. Engineering students enrolled in a nonmajors' survey course on electronic circuits will find that portions of Chapters 1 to 7 offer a valuable supplement to their study. Each chapter contains a brief review of pertinent topics along with governing equations and laws, with examples inserted to immediately clarify and emphasize principles as introduced. As in other Schaum's Outlines, primary emphasis is on the solution of problems; to this end, over 350 solved problems are presented.

Three principal changes are introduced in the second edition. SPICE method solutions are presented for numerous problems to better correlate the material with current college class methods. The first-edition Chapter 13 entitled "Vacuum Tubes" has been eliminated. However, the material from that chapter relating to triode vacuum tubes has been dispersed into Chapters 4 and 7. A new Chapter 10 entitled "Switched Mode Power Supplies" has been added to give the reader exposure to this important technology.

SPICE is an acronym for Simulation Program with Integrated Circuit Emphasis. It is commonly used as a generic reference to a host of circuit simulators that use the SPICE2 solution engine developed by U.S. government funding and, as a consequence, is public domain software. PSpice is the first personal computer version of SPICE that was developed by MicroSim Corporation (purchased by OrCAD, which has since merged with Cadence Design Systems, Inc.). As a promotional tool, MicroSim made available several evaluation versions of PSpice for free distribution without restriction on usage. These evaluation versions can still be downloaded from many websites. Presently, Cadence Design Systems, Inc. makes available an evaluation version of PSpice for download by students and professors at *www.orcad.com/Products/Simulation/PSpice/eval.asp*.

The presentation of SPICE in this book is at the netlist code level that consists of a collection of element-specification statements and control statements that can be compiled and executed by most SPICE solution engines. However, the programs are set up for execution by PSpice and, as a result, contain certain control statements that are particular to PSpice. One such example is the .PROBE statement. Probe is the proprietary PSpice plot manager which, when invoked, saves all node voltages and branch currents of a circuit for plotting at the user's discretion. Netlist code for problems solved by SPICE methods in this book can be downloaded at the author's website *www.engr.uky.edu/~cathey*. Errata for this book and selected evaluation versions of PSpice are also available at this website.

The book is written with the assumption that the user has some prior or companion exposure to SPICE methods in other formal course work. If the user does not have a ready reference to SPICE analysis methods, the three following references are suggested (pertinent version of PSpice is noted in parentheses):

1. *SPICE: A Guide to Circuit Simulation and Analysis Using PSpice*, Paul W. Tuinenga, Prentice-Hall, Englewood Cliffs, NJ, 1992, ISBN 0-13-747270-6 (PSpice 4).

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2. *Basic Engineering Circuit Analysis*, 6/e, J. David Irwin and Chwan-Hwa Wu, John Wiley & Sons, New York, 1999, ISBN 0-471-36574-2 (PSpice 8).
3. *Basic Engineering Circuit Analysis*, 7/e, J. David Irwin, John Wiley & Sons, New York, 2002, ISBN 0-471-40740-2 (PSpice 9).

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CHAPTER 1

Circuit Analysis: Port Point of View

1.1. INTRODUCTION

Electronic devices are described by their nonlinear terminal voltage-current characteristics. Circuits containing electronic devices are analyzed and designed either by utilizing graphs of experimentally measured characteristics or by linearizing the voltage-current characteristics of the devices. Depending upon applicability, the latter approach involves the formulation of either small-perturbation equations valid about an operating point or a piecewise-linear equation set. The linearized equation set describes the circuit in terms of its interconnected passive elements and independent or controlled voltage and current sources; formulation and solution require knowledge of the circuit analysis and circuit reduction principles reviewed in this chapter.

1.2. CIRCUIT ELEMENTS

The time-stationary (or constant-value) elements of Fig. 1-1(*a*) to (*c*) (the resistor, inductor, and capacitor, respectively) are called *passive elements*, since none of them can continuously supply energy to a circuit. For voltage v and current i, we have the following relationships: For the resistor,

$$v = Ri \qquad \text{or} \qquad i = Gv \tag{1.1}$$

where R is its *resistance* in ohms (Ω), and $G \equiv 1/R$ is its *conductance* in siemens (S). Equation (*1.1*) is known as *Ohm's law*. For the inductor,

$$v = L\frac{di}{dt} \qquad \text{or} \qquad i = \frac{1}{L}\int_{-\infty}^{t} v\,d\tau \tag{1.2}$$

where L is its *inductance* in henrys (H). For the capacitor,

$$v = \frac{1}{C}\int_{-\infty}^{t} i\,d\tau \qquad \text{or} \qquad i = C\frac{dv}{dt} \tag{1.3}$$

where C is its *capacitance* in farads (F). If R, L, and C are independent of voltage and current (as well as of time), these elements are said to be linear: Multiplication of the current through each by a constant will result in the multiplication of its terminal voltage by that same constant. (See Problems 1.1 and 1.3.)

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The elements of Fig. 1-1(*d*) to (*h*) are called *active elements* because each is capable of continuously supplying energy to a network. The *ideal voltage source* in Fig. 1-1(*d*) provides a terminal voltage v that is independent of the current i through it. The *ideal current source* in Fig. 1-1(*e*) provides a current i that is independent of the voltage across its terminals. However, the *controlled* (or *dependent*) *voltage source* in Fig. 1-1(*f*) has a terminal voltage that depends upon the voltage across or current through some other element of the network. Similarly, the *controlled* (or *dependent*) *current source* in Fig. 1-1(*g*) provides a current whose magnitude depends on either the voltage across or current through some other element of the network. If the dependency relation for the voltage or current of a controlled source is of the first degree, then the source is called a *linear* controlled (or dependent) source. The *battery* or *dc voltage source* in Fig. 1-1(*h*) is a special kind of independent voltage source.

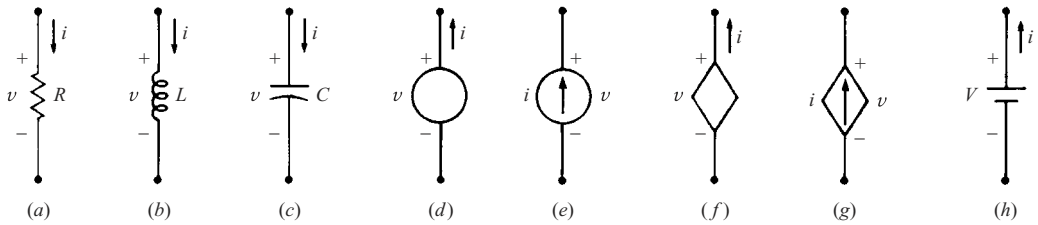


Fig. 1-1

1.3. SPICE ELEMENTS

The passive and active circuit elements introduced in the previous section are all available in SPICE modeling; however, the manner of node specification and the voltage and current sense or direction are clarified for each element by Fig. 1-2. The universal ground node is assigned the number 0. Otherwise, the node numbers n_1 (positive node) and n_2 (negative node) are positive integers

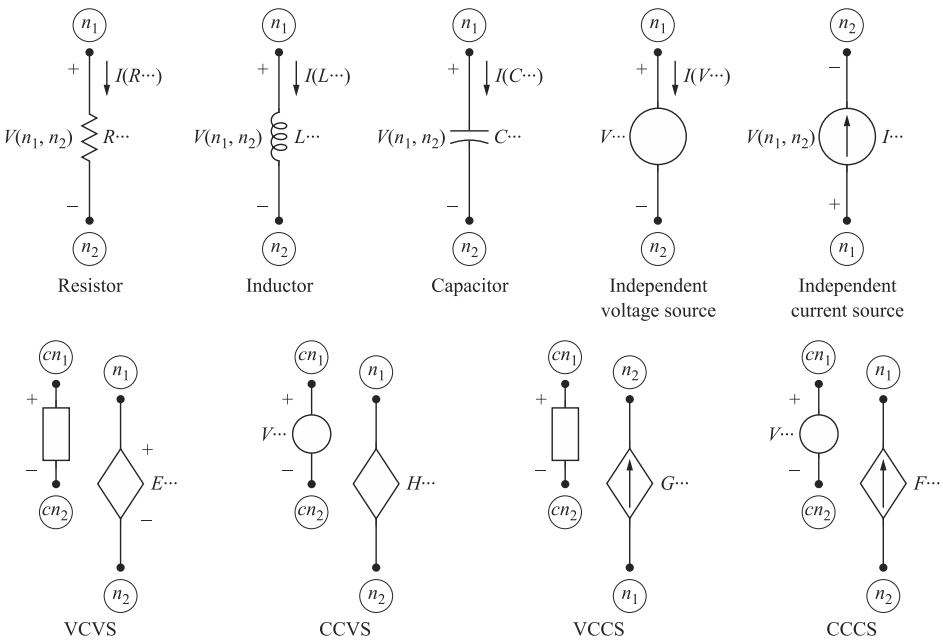


Fig. 1-2

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selected to uniquely define each node in the network. The assumed direction of positive current flow is from node n_1 to node n_2.

The four controlled sources—voltage-controlled voltage source (VCVS), current-controlled voltage source (CCVS), voltage-controlled current source (VCCS), and current-controlled current source (CCCS)— have the associated controlling element also shown with its nodes indicated by cn_1 (positive) and cn_2 (negative). Each element is described by an *element specification statement* in the SPICE netlist code. Table 1-1 presents the basic format for the element specification statement for each of the elements of Fig. 1-2. The first letter of the element name specifies the device and the remaining characters must assure a unique name.

Table 1-1

Element	Name	Signal Type	Control Source	Value
Resistor	R···			Ω
Inductor	L···			H
Capacitor	C···			F
Voltage source	V···	AC or DC[a]		V[b]
Current source	I···	AC or DC[a]		A[b]
VCVS	E···		(cn_1, cn_2)	V/V
CCVS	H···		V···	V/A
VCCS	G···		(cn_1, cn_2)	A/V
CCCS	F···		V···	A/A

a. Time-varying signal types (SIN, PULSE, EXP, PWL, SFFM) also available.
b. AC signal types may specify phase angle as well as magnitude.

1.4. CIRCUIT LAWS

Along with the three voltage-current relationships (*1.1*) to (*1.3*), Kirchhoff's laws are sufficient to formulate the simultaneous equations necessary to solve for all currents and voltages of a network. (We use the term *network* to mean any arrangement of circuit elements.)

Kirchhoff's voltage law (KVL) states that *the algebraic sum of all voltages around any closed loop of a circuit is zero*; it is expressed mathematically as

$$\sum_{k=1}^{n} v_k = 0 \tag{1.4}$$

where n is the total number of passive- and active-element voltages around the loop under consideration.

Kirchhoff's current law (KCL) states that *the algebraic sum of all currents entering every node* (junction of elements) *must be zero*; that is

$$\sum_{k=1}^{m} i_k = 0 \tag{1.5}$$

where m is the total number of currents flowing into the node under consideration.

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1.5. STEADY-STATE CIRCUITS

At some (sufficiently long) time after a circuit containing linear elements is energized, the voltages and currents become independent of initial conditions and the time variation of circuit quantities becomes identical to that of the independent sources; the circuit is then said to be operating in the *steady state*. If all nondependent sources in a network are independent of time, the steady state of the network is referred to as the *dc steady state*. On the other hand, if the magnitude of each nondependent source can be written as $K \sin(\omega t + \phi)$, where K is a constant, then the resulting steady state is known as the *sinusoidal steady state*, and well-known frequency-domain, or phasor, methods are applicable in its analysis. In general, electronic circuit analysis is a combination of dc and sinusoidal steady-state analysis, using the principle of superposition discussed in the next section.

1.6. NETWORK THEOREMS

A *linear network* (or *linear circuit*) is formed by interconnecting the terminals of independent (that is, nondependent) sources, linear controlled sources, and linear passive elements to form one or more closed paths. The *superposition theorem* states that *in a linear network containing multiple sources, the voltage across or current through any passive element may be found as the algebraic sum of the individual voltages or currents due to each of the independent sources acting alone, with all other independent sources deactivated.*

An ideal voltage source is deactivated by replacing it with a short circuit. An ideal current source is deactivated by replacing it with an open circuit. In general, controlled sources remain active when the superposition theorem is applied.

Example 1.1. Is the network of Fig. 1-3 a linear circuit?

The definition of a linear circuit is satisfied if the controlled source is a linear controlled source; that is, if α is a constant.

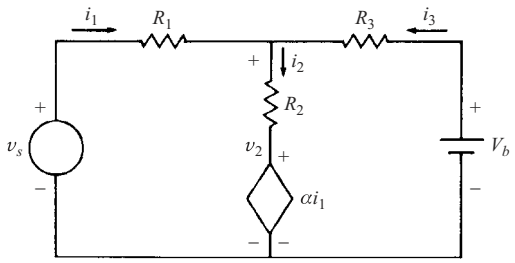


Fig. 1-3

Example 1.2. For the circuit of Fig. 1-3, $v_s = 10 \sin \omega t$ V, $V_b = 10$ V, $R_1 = R_2 = R_3 = 1\,\Omega$, and $\alpha = 0$. Find current i_2 by use of the superposition theorem.

We first deactivate V_b by shorting, and use a single prime to denote a response due to v_s alone. Using the method of node voltages with unknown v_2' and summing currents at the upper node, we have

$$\frac{v_s - v_2'}{R_1} = \frac{v_2'}{R_2} + \frac{v_2'}{R_3}$$

Substituting given values and solving for v_2', we obtain

$$v_2' = \tfrac{1}{3} v_s = \tfrac{10}{3} \sin \omega t$$

Then, by Ohm's law,

$$i_2' = \frac{v_2'}{R_2} = \tfrac{10}{3} \sin \omega t \text{ A}$$

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Now, deactivating v_s and using a double prime to denote a response due to V_b alone, we have

$$i_3'' = \frac{V_b}{R_3 + R_1 \| R_2}$$

where

$$R_1 \| R_2 \equiv \frac{R_1 R_2}{R_1 + R_2}$$

so that

$$i_3'' = \frac{10}{1 + 1/2} = \frac{20}{3} \text{ A}$$

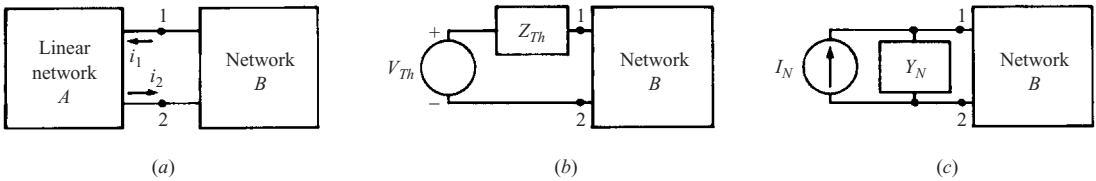
Then, by current division,

$$i_2'' = \frac{R_1}{R_1 + R_2} i_3'' = \frac{1}{2} i_3'' = \frac{1}{2}\frac{20}{3} = \frac{10}{3} \text{ A}$$

Finally, by the superposition theorem,

$$i_2 = i_2' + i_2'' = \frac{10}{3}(1 + \sin \omega t) \text{ A}$$

Terminals in a network are usually considered in pairs. A *port* is a terminal pair across which a voltage can be identified and such that the current into one terminal is the same as the current out of the other terminal. In Fig. 1-4, if $i_1 \equiv i_2$, then terminals 1 and 2 form a port. Moreover, as viewed to the left from terminals 1,2, network A is a one-port network. Likewise, viewed to the right from terminals 1,2, network B is a one-port network.



(a) (b) (c)

Fig. 1-4

Thévenin's theorem states that *an arbitrary linear, one-port network such as network A in Fig. 1-4(a) can be replaced at terminals 1,2 with an equivalent series-connected voltage source V_{Th} and impedance Z_{Th} $(= R_{Th} + jX_{Th})$ as shown in Fig. 1-4(b). V_{Th} is the open-circuit voltage of network A at terminals 1,2 and Z_{Th} is the ratio of open-circuit voltage to short-circuit current of network A determined at terminals 1,2 with network B disconnected. If network A or B contains a controlled source, its controlling variable must be in that same network.* Alternatively, Z_{Th} is the equivalent impedance looking into network A through terminals 1,2 with all independent sources deactivated. If network A contains a controlled source, Z_{Th} is found as the *driving-point impedance*. (See Example 1.4.)

Example 1.3. In the circuit of Fig. 1-5, $V_A = 4\,\text{V}$, $I_A = 2\,\text{A}$, $R_1 = 2\,\Omega$, and $R_2 = 3\,\Omega$. Find the Thévenin equivalent voltage V_{Th} and impedance Z_{Th} for the network to the left of terminals 1,2.

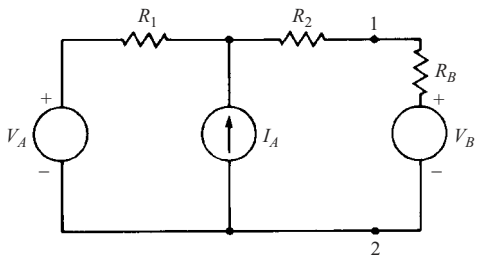


Fig. 1-5

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With terminals 1,2 open-circuited, no current flows through R_2; thus, by KVL,

$$V_{Th} = V_{12} = V_A + I_A R_1 = 4 + (2)(2) = 8\,\text{V}$$

The Thévenin impedance Z_{Th} is found as the equivalent impedance for the circuit to the left of terminals 1,2 with the independent sources deactivated (that is, with V_A replaced by a short circuit, and I_A replaced by an open circuit):

$$Z_{Th} = R_{Th} = R_1 + R_2 = 2 + 3 = 5\,\Omega$$

Example 1.4. In the circuit of Fig. 1-6(*a*), $V_A = 4\,\text{V}$, $\alpha = 0.25\,\text{A/V}$, $R_1 = 2\,\Omega$, and $R_2 = 3\,\Omega$. Find the Thévenin equivalent voltage and impedance for the network to the left of terminals 1,2.

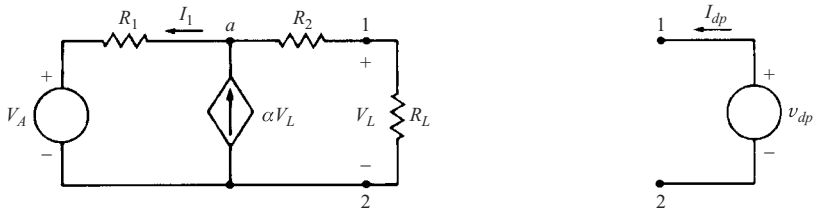


Fig. 1-6

With terminals 1,2 open-circuited, no current flows through R_2. But the control variable V_L for the voltage-controlled dependent source is still contained in the network to the left of terminals 1,2. Application of KVL yields

$$V_{Th} = V_L = V_A + \alpha V_{Th} R_1$$

so that

$$V_{Th} = \frac{V_A}{1 - \alpha R_1} = \frac{4}{1 - (0.25)(2)} = 8\,\text{V}$$

Since the network to the left of terminals 1,2 contains a controlled source, Z_{Th} is found as the driving-point impedance V_{dp}/I_{dp}, with the network to the right of terminals 1,2 in Fig. 1-6(*a*) replaced by the driving-point source of Fig. 1-6(*b*) and V_A deactivated (short-circuited). After these changes, KCL applied at node *a* gives

$$I_1 = \alpha V_{dp} + I_{dp} \tag{1.6}$$

Application of KVL around the outer loop of this circuit (with V_A still deactivated) yields

$$V_{dp} = I_{dp} R_2 + I_1 R_1 \tag{1.7}$$

Substitution of (*1.6*) into (*1.7*) allows solution for Z_{Th} as

$$Z_{Th} = \frac{V_{dp}}{I_{dp}} = \frac{R_1 + R_2}{1 - \alpha R_1} = \frac{2 + 3}{1 - (0.25)(2)} = 10\,\Omega$$

Norton's theorem states that *an arbitrary linear, one-port network such as network A in Fig. 1-4(a) can be replaced at terminals 1,2 by an equivalent parallel-connected current source I_N and admittance Y_N as shown in Fig. 1-4(c). I_N is the short-circuit current that flows from terminal 1 to terminal 2 due to network A, and Y_N is the ratio of short-circuit current to open-circuit voltage at terminals 1,2 with network B disconnected. If network A or B contains a controlled source, its controlling variable must be in that same network.* It is apparent that $Y_N \equiv 1/Z_{Th}$; thus, any method for determining Z_{Th} is equally valid for finding Y_N.

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Example 1.5. Use SPICE methods to determine the Thévenin equivalent circuit looking to the left through terminals 3,0 for the circuit of Fig. 1-7.

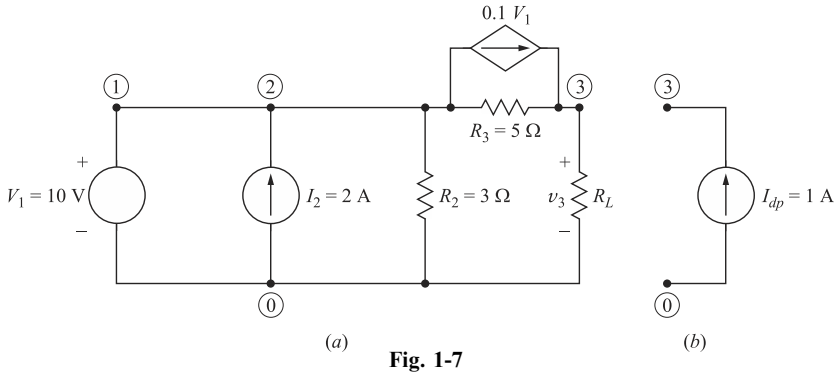


Fig. 1-7

In SPICE independent source models, an ideal voltage source of 0 V acts as a short circuit and an ideal current source of 0 A acts as an infinite impedance or open circuit. Advantage will be taken of these two features to solve the problem.

Load resistor R_L of Fig. 1-7(*a*) is replaced by the driving point current source I_{dp} of Fig. 1-7(*b*). The netlist code that follows forms a SPICE description of the resulting circuit. The code is set up with parameter-assigned values for V_1, I_2, and I_{dp}.

```
Ex1_5.CIR - Thevenin equivalent circuit
.PARAM V1value=0V I2value=0A Idpvalue=1A
V1 1 0 DC {V1value}
R1 1 2 1ohm
I2 0 2 DC {I2value}
R2 2 0 3ohm
R3 2 3 5ohm
G3 2 3 (1,0) 0.1 ; Voltage-controlled current-source
Idp 0 3 DC {Idpvalue}
.END
```

If both V_1 and I_2 are deactivated by setting V1value = I2value = 0, current $I_{dp} = 1$ A must flow through the Thévenin equivalent impedance $Z_{Th} = R_{Th}$ so that $v_3 = I_{dp}R_{Th} = R_{Th}$. Execution of <Ex1_5.CIR> by a SPICE program writes the values of the node voltages for nodes 1, 2, and 3 with respect to the universal ground node 0 in a file <Ex1_5.OUT>. Poll the output file to find $v_3 = \text{V(3)} = R_{Th} = 5.75\ \Omega$.

In order to determine V_{Th} (open-circuit voltage between terminals 3,0), edit <Ex1_5.CIR> to set V1value = 10V, I2value = 2A, and Idpvalue = 0A. Execute <Ex1_5.CIR> and poll the output file to find $V_{Th} = v_3 = \text{V(3)} = 14$ V.

Example 1.6. Find the Norton equivalent current I_N and admittance Y_N for the circuit of Fig. 1-5 with values as given in Example 1.3.

The Norton current is found as the short-circuit current from terminal 1 to terminal 2 by superposition; it is

$$I_N = I_{12} = \text{current due to } V_A + \text{current due to } I_A = \frac{V_A}{R_1 + R_2} + \frac{R_1 I_A}{R_1 + R_2}$$

$$= \frac{4}{2+3} + \frac{(2)(2)}{2+3} = 1.6\,\text{A}$$

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The Norton admittance is found from the result of Example 1.3 as

$$Y_N = \frac{1}{Z_{Th}} = \frac{1}{5} = 0.2\,\text{S}$$

We shall sometimes double-subscript voltages and currents to show the terminals that are of interest. Thus, V_{13} is the voltage across terminals 1 and 3, where terminal 1 is at a higher potential than terminal 3. Similarly, I_{13} is the current that flows *from* terminal 1 *to* terminal 3. As an example, V_L in Fig. 1-6(*a*) could be labeled V_{12} (but not V_{21}).

Note also that an active element (either independent or controlled) is restricted to its assigned, or stated, current or voltage, no matter what is involved in the rest of the circuit. Thus the controlled source in Fig. 1-6(*a*) will provide αV_L A no matter what voltage is required to do so and no matter what changes take place in other parts of the circuit.

1.7. TWO-PORT NETWORKS

The network of Fig. 1-8 is a *two-port* network if $I_1 = I_1'$ and $I_2 = I_2'$. It can be characterized by the four variables V_1, V_2, I_1, and I_2, only two of which can be independent. If V_1 and V_2 are taken as independent variables and the linear network contains no independent sources, the independent and dependent variables are related by the *open-circuit impedance parameters* (or, simply, the *z parameters*) z_{11}, z_{12}, z_{21}, and z_{22} through the equation set

$$V_1 = z_{11}I_1 + z_{12}I_2 \tag{1.8}$$

$$V_2 = z_{21}I_1 + z_{22}I_2 \tag{1.9}$$

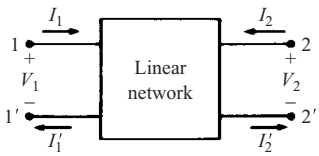


Fig. 1-8

Each of the z parameters can be evaluated by setting the proper current to zero (or, equivalently, by open-circuiting an appropriate port of the network). They are

$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} \tag{1.10}$$

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} \tag{1.11}$$

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} \tag{1.12}$$

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} \tag{1.13}$$

In a similar manner, if V_1 and I_2 are taken as the independent variables, a characterization of the two-port network via the *hybrid parameters* (or, simply, the *h-parameters*) results:

$$V_1 = h_{11}I_1 + h_{12}V_2 \tag{1.14}$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \tag{1.15}$$

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Two of the h parameters are determined by short-circuiting port 2, while the remaining two parameters are found by open-circuiting port 1:

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} \tag{1.16}$$

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} \tag{1.17}$$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} \tag{1.18}$$

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} \tag{1.19}$$

Example 1.7. Find the z parameters for the two-port network of Fig. 1-9.

With port 2 (on the right) open-circuited, $I_2 = 0$ and the use of (*1.10*) gives

$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = R_1 \| (R_2 + R_3) = \frac{R_1(R_2 + R_3)}{R_1 + R_2 + R_3}$$

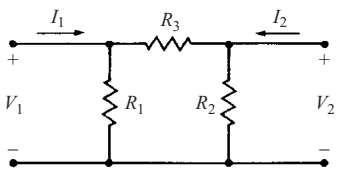


Fig. 1-9

Also, the current I_{R2} flowing downward through R_2 is, by current division,

$$I_{R2} = \frac{R_1}{R_1 + R_2 + R_3} I_1$$

But, by Ohm's law,

$$V_2 = I_{R2} R_2 = \frac{R_1 R_2}{R_1 + R_2 + R_3} I_1$$

Hence, by (*1.12*),

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} = \frac{R_1 R_2}{R_1 + R_2 + R_3}$$

Similarly, with port 1 open-circuited, $I_1 = 0$ and (*1.13*) leads to

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} = R_2 \| (R_1 + R_3) = \frac{R_2(R_1 + R_3)}{R_1 + R_2 + R_3}$$

The use of current division to find the current downward through R_1 yields

$$I_{R1} = \frac{R_2}{R_1 + R_2 + R_3} I_2$$

and Ohm's law gives

$$V_1 = R_1 I_{R1} = \frac{R_1 R_2}{R_1 + R_2 + R_3} I_2$$

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Thus, by (*1.11*),

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} = \frac{R_1 R_2}{R_1 + R_2 + R_3}$$

Example 1.8. Find the h parameters for the two-port network of Fig. 1-9.

With port 2 short-circuited, $V_2 = 0$ and, by (*1.16*),

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} = R_1 \| R_3 = \frac{R_1 R_3}{R_1 + R_3}$$

By current division,

$$I_2 = -\frac{R_1}{R_1 + R_3} I_1$$

so that, by (*1.18*),

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} = -\frac{R_1}{R_1 + R_3}$$

If port 1 is open-circuited, voltage division and (*1.17*) lead to

$$V_1 = \frac{R_1}{R_1 + R_3} V_2$$

and

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} = \frac{R_1}{R_1 + R_3}$$

Finally, h_{22} is the admittance looking into port 2, as given by (*1.19*):

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} = \frac{1}{R_2 \| (R_1 + R_3)} = \frac{R_1 + R_2 + R_3}{R_2 (R_1 + R_3)}$$

The z parameters and the h parameters can be numerically evaluated by SPICE methods. In electronics applications, the z and h parameters find application in analysis when small ac signals are impressed on circuits that exhibit limited-range linearity. Thus, in general, the test sources in the SPICE analysis should be of magnitudes comparable to the impressed signals of the anticipated application. Typically, the devices used in an electronic circuit will have one or more dc sources connected to bias or that place the device at a favorable point of operation. The input and output ports may be coupled by large capacitors that act to block the appearance of any dc voltages at the input and output ports while presenting negligible impedance to ac signals. Further, electronic circuits are usually frequency-sensitive so that any set of z or h parameters is valid for a particular frequency. Any SPICE-based evaluation of the z and h parameters should be capable of addressing the above outlined characteristics of electronic circuits.

Example 1.9. For the frequency-sensitive two-port network of Fig. 1-10(*a*), use SPICE methods to determine the z parameters suitable for use with sinusoidal excitation over a frequency range from 1 kHz to 10 kHz.

The z parameters as given by (*1.10*) to (*1.13*), when evaluated for sinusoidal steady-state conditions, are formed as the ratios of phasor voltages and currents. Consequently, the values of the z parameters are complex numbers that can be represented in polar form as $\boldsymbol{z}_{ij} = z_{ij} \angle \phi_{ij}$.

For determination of the z parameters, matching terminals of the two sinusoidal current sources of Fig. 1-10(*b*) are connected to the network under test of Fig. 1-10(*a*). The netlist code below models the resulting network with parameter-assigned values for $\bar{I}_1$ and $\bar{I}_5$. Two separate executions of < Ex1_9.CIR > are required to determine all four z parameters. The .AC statement specifies a sinusoidal steady-state solution of the circuit for 11 values of frequency over the range from 10 kHz to 100 kHz.

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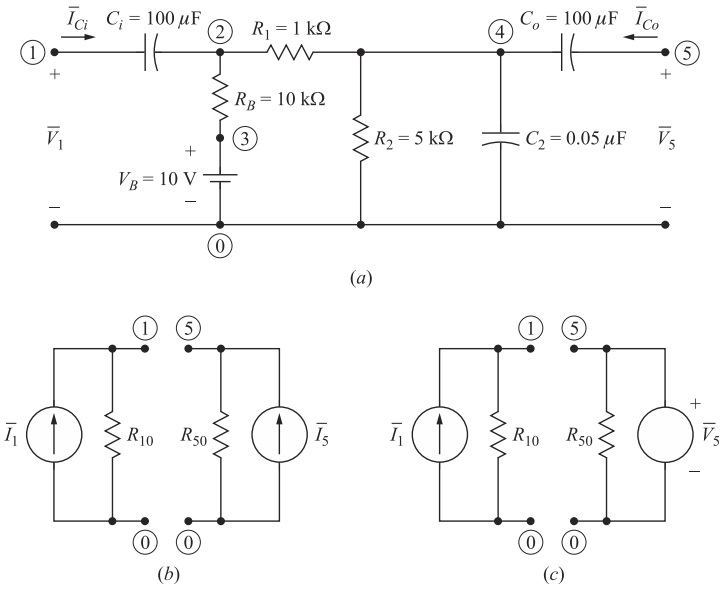


Fig. 1-10

```
Ex1_9.CIR - z-parameter evaluation
.PARAM I1value=1mA I5value=0mA
I1  0 1 AC {I1value}
R10 1 0 1Tohm ; Large resistor to avoid floating node
Ci  1 2 100uF
RB  2 3 10kohm
VB  0 3 DC 10V
R1  2 4 1kohm
R2  4 0 5kohm
C2  4 0 0.05uF
Co  5 4 100uF
I5  0 5 AC {I5value}
R50 5 0 1Tohm ; Large resistor to avoid floating node
.AC LIN 11 10kHz 100kHz
.PROBE
.END
```

The values of R10 and R50 are sufficiently large ($1 \times 10^{12}\,\Omega$) so that $\bar{I}_1 = \bar{I}_{Ci}$ and $\bar{I}_5 = \bar{I}_{Co}$. If source $\bar{I}_5$ is deactivated by setting I5value = 0 and I1value is assigned a small value (i.e., 1 mA), then z_{11} and z_{21} are determined by (*1.10*) and (*1.12*), respectively. < Ex1_9.CIR > is executed and the probe feature of PSpice is used to graphically display the magnitudes and phase angles of z_{11} and z_{21} in Fig. 1-11(*a*). Similarly, $\bar{I}_1$ is deactivated and $\bar{I}_5$ is assigned a small value (I1value = 0, I5value = 1mA) to determine the values of z_{12} and z_{22} by (*1.11*) and (*1.13*), respectively. Execution of < Ex1_9.CIR > and use of the Probe feature of PSpice results in the magnitudes and phase angles of z_{12} and z_{22} as shown by Fig. 1-11(*b*).

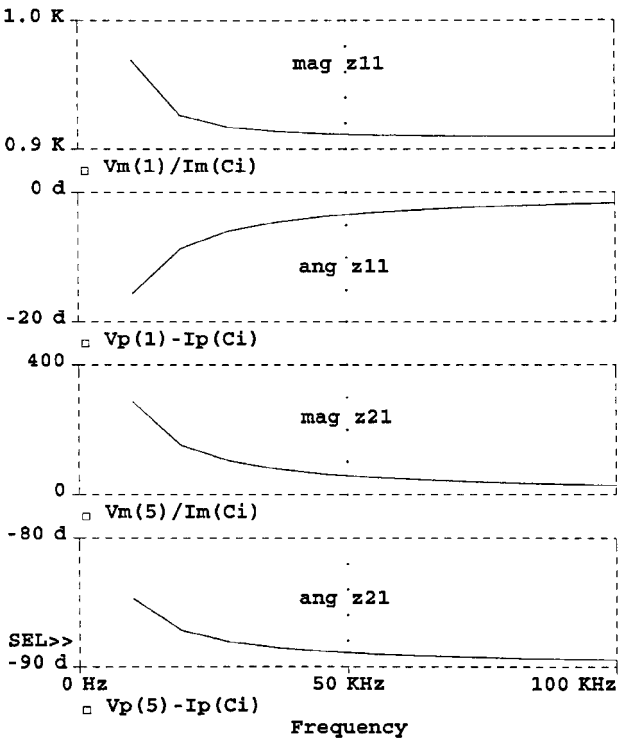
Example 1.10. Use SPICE methods to determine the *h* parameters suitable for use with sinusoidal excitation at a frequency of 10 kHz for the frequency-sensitive two-port network of Fig. 1-10(*a*).

The *h* parameters of (*1.16*) to (*1.19*) for sinusoidal steady-state excitation are ratios of phasor voltages and currents; thus the values are complex numbers expressible in polar form as $\boldsymbol{h}_{ij} = h_{ij}\angle\phi_{ij}$.

Connect the sinusoidal voltage source and current source of Fig. 1-10(*c*) to the network of Fig. 1-10(*a*). The netlist code below models the resulting network with parameter-assigned values for $\bar{I}_1$ and $\bar{V}_5$. Two separate executions of < Ex1_10.CIR > are required to produce the results needed for evaluation of all four *h* parameters.

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(*a*)



(*b*)

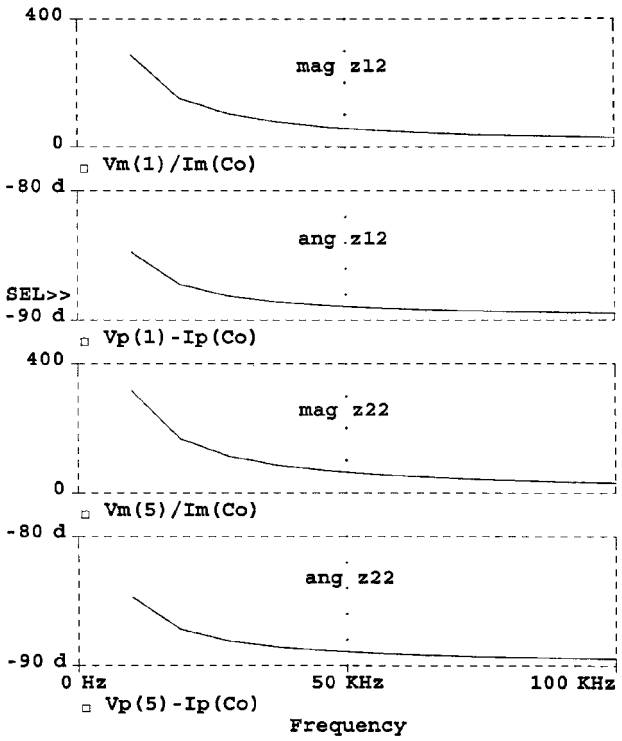


Fig. 1-11

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Through use of the .PRINT statement, both magnitudes and phase angles of $\bar{V}_1$, $\bar{V}_5$, $\bar{I}_{Ci}$, and $\bar{I}_{Co}$ are written to < Ex1_10.OUT > and can be retrieved by viewing of the file.

```
Ex1_10.CIR - h-parameter evaluation
.PARAM I1value=0mA V5value=1mV
I1  0 1 AC {I1value}
R10 1 0 1Tohm ; Large resistor to avoid floating node
Ci  1 2 100uF
RB  2 3 10kohm
VB  0 3 DC 10V
R1  2 4 1kohm
R2  4 0 5kohm
C2  4 0 0.05uF
Co  5 4 100uF
V5  5 0 AC {V5value}
.AC LIN 1 10kHz 10kHz
.PRINT AC Vm(1) Vp(1) Im(Ci) Ip(Ci) ; Mag & phase of inputs
.PRINT AC Vm(5) Vp(5) Im(Co) Ip(Co) ; Mag & phase of outputs
.END
```

Set V5value = 0 (deactivates $\bar{V}_5$) and I1value = 1mA. Execute < Ex1_10.CIR > and retrieve the necessary values of $\bar{V}_1, \bar{I}_{Ci}$, and $\bar{I}_{Co}$ to calculate $\boldsymbol{h}_{11}$ and $\boldsymbol{h}_{21}$ by use of (*1.16*) and (*1.18*).

$$\boldsymbol{h}_{11} = \frac{\text{Vm(1)}}{\text{Im(Ci)}} \angle(\text{Vp(1)} - \text{Ip(Ci)}) \cong \frac{0.9091}{0.001} \angle(-0.02^\circ + 0^\circ) = 909.1 \angle -0.02^\circ$$

$$\boldsymbol{h}_{21} = \frac{\text{Im(Co)}}{\text{Im(Ci)}} \angle(\text{Ip(Co)} - \text{Ip(Ci)}) \cong \frac{9.08 \times 10^{-4}}{1 \times 10^{-3}} \angle(-180^\circ + 0^\circ) = 0.908 \angle -180^\circ$$

Set V5value = 1mV and I1value = 0 (deactivates $\bar{I}_1$). Execute < Exl_10.CIR > and retrieve the needed values of $\bar{V}_1, \bar{V}_5$, and $\bar{I}_{Co}$ to evaluate $\boldsymbol{h}_{12}$ and $\boldsymbol{h}_{22}$ by use of (*1.17*) and (*1.19*).

$$\boldsymbol{h}_{21} = \frac{\text{Vm(1)}}{\text{Vm(5)}} \angle(\text{Vp(1)} - \text{Vp(5)}) \cong \frac{9.08 \times 10^{-4}}{1 \times 10^{-3}} \angle(0^\circ - 0^\circ) = 0.908 \angle 0^\circ$$

$$\boldsymbol{h}_{22} = \frac{\text{Im(Co)}}{\text{Vm(5)}} \angle(\text{Ip(Co)} - \text{Vp(5)}) \cong \frac{3.15 \times 10^{-6}}{1 \times 10^{-3}} \angle(84.7^\circ - 0^\circ) = 3.15 \times 10^{-3} \angle 84.7^\circ$$

1.8. INSTANTANEOUS, AVERAGE, AND RMS VALUES

The *instantaneous value* of a quantity is the value of that quantity at a specific time. Often we will be interested in the average value of a time-varying quantity. But obviously, the average value of a sinusoidal function over one period is zero. For sinusoids, then, another concept, that of the *root-mean-square* (or *rms*) value, is more useful: For any time-varying function $f(t)$ with period T, the *average* value over one period is given by

$$F_0 = \frac{1}{T} \int_{t_0}^{t_0+T} f(t)\, dt \tag{1.20}$$

and the corresponding rms value is defined as

$$F = \sqrt{\frac{1}{T} \int_{t_0}^{t_0+T} f^2(t)\, dt} \tag{1.21}$$

where, of course, F_0 and F are independent of t_0. The motive for introducing rms values can be gathered from Example 1.12.

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Example 1.11. Since the average value of a sinusoidal function of time is zero, the *half-cycle* average value, which is nonzero, is often useful. Find the half-cycle average value of the current through a resistance R connected directly across a periodic (ac) voltage source $v(t) = V_m \sin \omega t$.

By Ohm's law,

$$i(t) = \frac{v(t)}{R} = \frac{V_m}{R} \sin \omega t$$

and from (*1.20*), applied over the half cycle from $t_0 = 0$ to $T/2 = \pi$,

$$I_0 = \frac{1}{\pi} \int_0^{\pi} \frac{V_m}{R} \sin \omega t \, d(\omega t) = \frac{1}{\pi} \frac{V_m}{R} [-\cos \omega t]_{\omega t=0}^{\pi} = \frac{2}{\pi} \frac{V_m}{R} \tag{1.22}$$

Example 1.12. Consider a resistance R connected directly across a dc voltage source V_{dc}. The power absorbed by R is

$$P_{\text{dc}} = \frac{V_{\text{dc}}^2}{R} \tag{1.23}$$

Now replace V_{dc} with an ac voltage source, $v(t) = V_m \sin \omega t$. The *instantaneous power* is now given by

$$p(t) = \frac{v^2(t)}{R} = \frac{V_m^2}{R} \sin^2 \omega t \tag{1.24}$$

Hence, the *average power* over one period is, by (*1.20*),

$$P_0 = \frac{1}{2\pi} \int_0^{2\pi} \frac{V_m^2}{R} \sin^2 \omega t \, d(\omega t) = \frac{V_m^2}{2R} \tag{1.25}$$

Comparing (*1.23*) and (*1.25*), we see that, insofar as power dissipation is concerned, an ac source of amplitude V_m is equivalent to a dc source of magnitude

$$\frac{V_m}{\sqrt{2}} = \sqrt{\frac{1}{T} \int_0^T v^2(t) \, dt} \equiv V \tag{1.26}$$

For this reason, the rms value of a sinusoid, $V = V_m/\sqrt{2}$, is also called its *effective* value.

From this point on, unless an explicit statement is made to the contrary, all currents and voltages in the frequency domain (phasors) will reflect rms rather than maximum values. Thus, the time-domain voltage $v(t) = V_m \cos(\omega t + \phi)$ will be indicated in the frequency domain as $\bar{V} = V \underline{/\phi}$, where $V = V_m/\sqrt{2}$.

Example 1.13. A sinusoidal source, a dc source, and a 10 Ω resistor are connected as shown by Fig. 1-12. If $v_s = 10 \sin(\omega t - 30^\circ)$ V and $V_B = 20$ V, use SPICE methods to determine the average value of $i(I_0)$, the rms value of $i(I)$, and the average value of power (P_0) supplied to R.

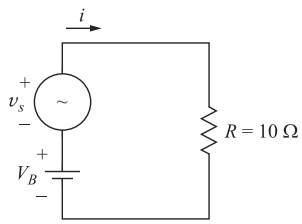


Fig. 1-12

The netlist code below describes the circuit. Notice that the two sources have been combined as a 10 V sinusoidal source with a 20-V dc bias. The frequency has been arbitrarily chosen as 100 Hz as the solution is independent of frequency.

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```
Ex1_13.CIR - Avg & rms current, avg power
vsVB 1 0 SIN(20V 10V 100Hz 0 0 -30deg)
R     1 0 10ohm
.PROBE
.TRAN 5us 10ms
.END
```

The Probe feature of PSpice is used to display the instantaneous values of $i(t)$ and $p_R(t)$. The running average and running RMS features of PSpice have been implemented as appropriate. Both features give the correct full-period values at the end of each period of the source waveform. Figure 1-13 shows the marked values as $I_0 = 2.0\,\text{A}$, $I = 2.1213\,\text{A}$, and $P_0 = 45.0\,\text{W}$.

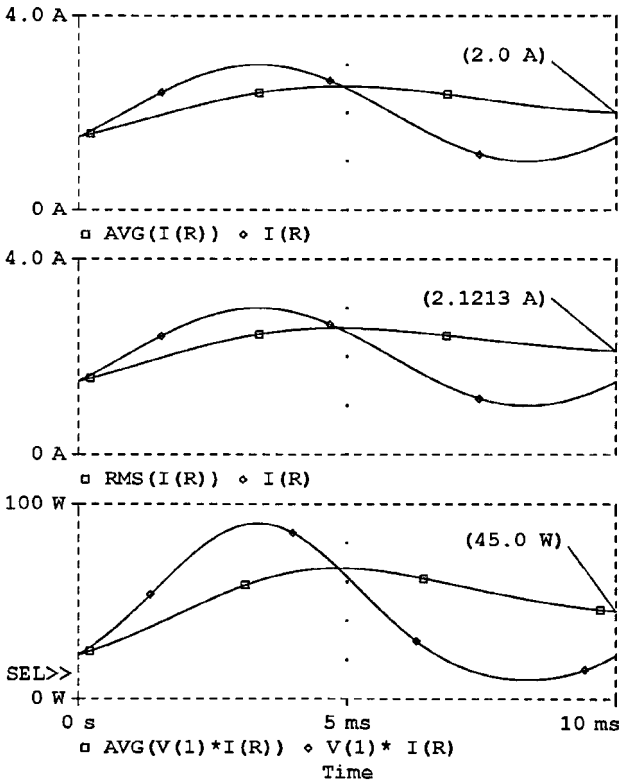


Fig. 1-13

Solved Problems

1.1 Prove that the inductor element of Fig. 1-1(*b*) is a linear element by showing that (*1.2*) satisfies the converse of the superposition theorem.

Let i_1 and i_2 be two currents that flow through the inductors. Then by (*1.2*) the voltages across the inductor for these currents are, respectively,

$$v_1 = L\frac{di_1}{dt} \qquad \text{and} \qquad v_2 = L\frac{di_2}{dt} \tag{1}$$

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Now suppose $i = k_1 i_1 + k_2 i_2$, where k_1 and k_2 are distinct arbitrary constants. Then by (*1.2*) and (*1*),

$$v = L\frac{d}{dt}(k_1 i_1 + k_2 i_2) = k_1 L\frac{di_1}{dt} + k_2 L\frac{di_2}{dt} = k_1 v_1 + k_2 v_2 \tag{2}$$

Since (*2*) holds for any pair of constants (k_1, k_2), superposition is satisfied and the element is linear.

1.2 If $R_1 = 5\,\Omega$, $R_2 = 10\,\Omega$, $V_s = 10\,\text{V}$, and $I_s = 3\,\text{A}$ in the circuit of Fig. 1-14, find the current i by using the superposition theorem.

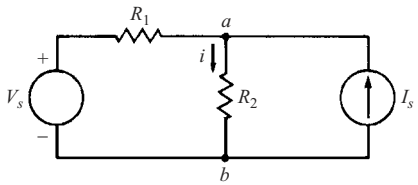


Fig. 1-14

With I_s deactivated (open-circuited), KVL and Ohm's law give the component of i due to V_s as

$$i' = \frac{V_s}{R_1 + R_2} = \frac{10}{5 + 10} = 0.667\,\text{A}$$

With V_s deactivated (short-circuited), current division determines the component of i due to I_s:

$$i'' = \frac{R_1}{R_1 + R_2} I_s = \frac{5}{5 + 10}\,3 = 1\,\text{A}$$

By superposition, the total current is

$$i = i' + i'' = 0.667 + 1 = 1.667\,\text{A}$$

1.3 In Fig. 1-14, assume all circuit values as in Problem 1.2 except that $R_2 = 0.25i\,\Omega$. Determine the current i using the method of node voltages.

By (*1.1*), the voltage-current relationship for R_2 is

$$v_{ab} = R_2 i = (0.25i)(i) = 0.25i^2$$

so that

$$i = 2\sqrt{v_{ab}} \tag{1}$$

Applying the method of node voltages at a and using (*1*), we get

$$\frac{v_{ab} - V_s}{R_1} + 2\sqrt{v_{ab}} - I_s = 0$$

Rearrangement and substitution of given values lead to

$$v_{ab} + 10\sqrt{v_{ab}} - 25 = 0$$

Letting $x^2 = v_{ab}$ and applying the quadratic formula, we obtain

$$x = \frac{-10 \pm \sqrt{(10)^2 - 4(-25)}}{2} = 2.071 \qquad \text{or} \qquad -12.071$$

The negative root is extraneous, since the resulting value of v_{ab} would not satisfy KVL; thus,

$$v_{ab} = (2.071)^2 = 4.289\,\text{V} \qquad \text{and} \qquad i = 2 \times 2.071 = 4.142\,\text{A}$$

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Notice that, because the resistance R_2 is a function of current, the circuit is not linear and the superposition theorem cannot be applied.

1.4 For the circuit of Fig. 1-15, find v_{ab} if (*a*) $k = 0$ and (*b*) $k = 0.01$. Do not use network theorems to simplify the circuit prior to solution.

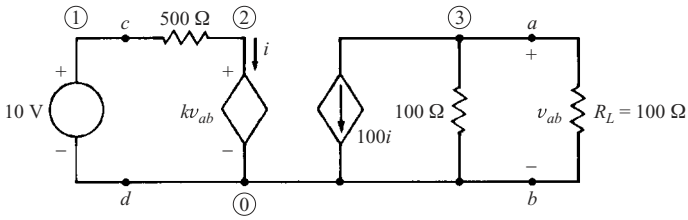


Fig. 1-15

(*a*) For $k = 0$, the current i can be determined immediately with Ohm's law:

$$i = \frac{10}{500} = 0.02\,\text{A}$$

Since the output of the controlled current source flows through the parallel combination of two 100-Ω resistors, we have

$$v_{ab} = -(100i)(100\|100) = -100 \times 0.02\,\frac{(100)(100)}{100+100} = -100\,\text{V} \tag{1}$$

(*b*) With $k \neq 0$, it is necessary to solve two simultaneous equations with unknowns i and v_{ab}. Around the left loop, KVL yields

$$0.01v_{ab} + 500i = 10 \tag{2}$$

With i unknown, (*1*) becomes

$$v_{ab} + 5000i = 0 \tag{3}$$

Solving (*2*) and (*3*) simultaneously by Cramer's rule leads to

$$v_{ab} = \frac{\begin{vmatrix} 10 & 500 \\ 0 & 5000 \end{vmatrix}}{\begin{vmatrix} 0.01 & 500 \\ 1 & 5000 \end{vmatrix}} = \frac{50{,}000}{-450} = -111.1\,\text{V}$$

1.5 For the circuit of Fig. 1-15, use SPICE methods to solve for v_{ab} if (*a*) $k = 0.001$ and (*b*) $k = 0.05$.

(*a*) The SPICE netlist code for $k = 0.001$ follows:

```
Prb.1_5.CIR
Vs 1 0 DC 10V
R1 1 2 500ohm
E  2 0 (3,0) 0.001 ; Last entry is value of k
F  0 3 Vs 100
R2 3 0 100ohm
RL 3 0 100ohm
.DC Vs 10 10 1
.PRINT DC V(3)
.END
```

Execute <Prb1_5.CIR> and poll the output file to find $v_{ab} = V(3) = -101\,\text{V}$.

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(*b*) Edit <Prb1_5.CIR> to set $k = 0.05$, execute the code, and poll the output file to find $v_{ab} = V(3) = -200\,\text{V}$.

1.6 For the circuit of Fig. 1-16, find i_L by the method of node voltages if (*a*) $\alpha = 0.9$ and (*b*) $\alpha = 0$.

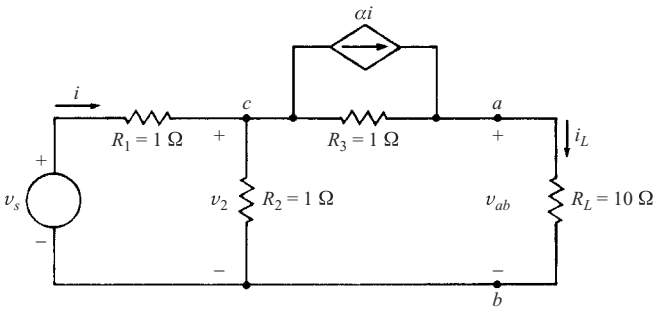


Fig. 1-16

(*a*) With v_2 and v_{ab} as unknowns and summing currents at node c, we obtain

$$\frac{v_2 - v_s}{R_1} + \frac{v_2}{R_2} + \frac{v_2 - v_{ab}}{R_3} + \alpha i = 0 \tag{1}$$

But

$$i = \frac{v_s - v_2}{R_1} \tag{2}$$

Substituting (*2*) into (*1*) and rearranging gives

$$\left(\frac{1-\alpha}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)v_2 - \frac{1}{R_3}v_{ab} = \frac{1-\alpha}{R_1}v_s \tag{3}$$

Now, summation of currents at node a gives

$$\frac{v_{ab} - v_2}{R_3} - \alpha i + \frac{v_{ab}}{R_L} = 0 \tag{4}$$

Substituting (*2*) into (*4*) and rearranging yields

$$-\left(\frac{1}{R_3} - \frac{\alpha}{R_1}\right)v_2 + \left(\frac{1}{R_3} + \frac{1}{R_L}\right)v_{ab} = \frac{\alpha}{R_1}v_s \tag{5}$$

Substitution of given values into (*3*) and (*5*) and application of Cramer's rule finally yield

$$v_{ab} = \frac{\begin{vmatrix} 2.1 & 0.1v_s \\ -0.1 & 0.9v_s \end{vmatrix}}{\begin{vmatrix} 2.1 & -1 \\ -0.1 & 1.1 \end{vmatrix}} = \frac{1.9v_s}{2.21} = 0.8597v_s$$

and by Ohm's law,

$$i_L = \frac{v_{ab}}{R_L} = \frac{0.8597v_s}{10} = 0.08597v_s \quad \text{A}$$

(*b*) With the given values (including $\alpha = 0$) substituted into (*3*) and (*5*), Cramer's rule is used to find

$$v_{ab} = \frac{\begin{vmatrix} 3 & v_s \\ -1 & 0 \end{vmatrix}}{\begin{vmatrix} 3 & -1 \\ -1 & 1.1 \end{vmatrix}} = \frac{v_s}{2.3} = 0.4348v_s$$

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Then i_L is again found with Ohm's law:

$$i_L = \frac{v_{ab}}{R_L} = \frac{0.4348 v_s}{10} = 0.04348 v_s \quad \text{A}$$

1.7 If $V_1 = 10\,\text{V}$, $V_2 = 15\,\text{V}$, $R_1 = 4\,\Omega$, and $R_2 = 6\,\Omega$ in the circuit of Fig. 1-17, find the Thévenin equivalent for the network to the left of terminals a, b.

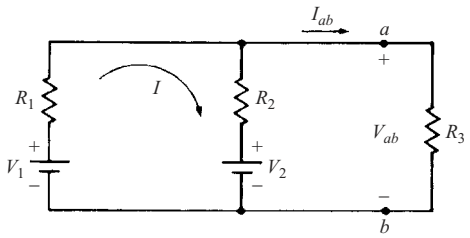


Fig. 1-17

With terminals a, b open-circuited, only loop current I flows. Then, by KVL,

$$V_1 - IR_1 = V_2 + IR_2$$

so that

$$I = \frac{V_1 - V_2}{R_1 + R_2} = \frac{10 - 15}{4 + 6} = -0.5\,\text{A}$$

The Thévenin equivalent voltage is then

$$V_{Th} = V_{ab} = V_1 - IR_1 = 10 - (-0.5)(4) = 12\,\text{V}$$

Deactivating (shorting) the independent voltage sources V_1 and V_2 gives the Thévenin impedance to the left of terminals a, b as

$$Z_{Th} = R_{Th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{(4)(6)}{4 + 6} = 2.4\,\Omega$$

V_{Th} and Z_{Th} are connected as in Fig. 1-4(b) to produce the Thévenin equivalent circuit.

1.8 For the circuit and values of Problem 1.7, find the Norton equivalent for the network to the left of terminals a, b.

With terminals a, b shorted, the component of current I_{ab} due to V_1 alone is

$$I'_{ab} = \frac{V_1}{R_1} = \frac{10}{4} = 2.5\,\text{A}$$

Similarly, the component due to V_2 alone is

$$I''_{ab} = \frac{V_2}{R_2} = \frac{15}{6} = 2.5\,\text{A}$$

Then, by superposition,

$$I_N = I_{ab} = I'_{ab} + I''_{ab} = 2.5 + 2.5 = 5\,\text{A}$$

Now, with R_{Th} as found in Problem 1.7,

$$Y_N = \frac{1}{R_{Th}} = \frac{1}{2.4} = 0.4167\,\text{A}$$

I_N and Y_N are connected as in Fig. 1-4(c) to produce the Norton equivalent circuit.

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1.9 For the circuit and values of Problems 1.7 and 1.8, find the Thévenin impedance as the ratio of open-circuit voltage to short-circuit current to illustrate the equivalence of the results.

The open-circuit voltage is V_{Th} as found in Problem 1.7, and the short-circuit current is I_N from Problem 1.8. Thus,

$$Z_{Th} = \frac{V_{Th}}{I_N} = \frac{12}{5} = 2.4\,\Omega$$

which checks with the result of Problem 1.7.

1.10 Thévenin's and Norton's theorems are applicable to other than dc steady-state circuits. For the "frequency-domain" circuit of Fig. 1-18 (where s is frequency), find (*a*) the Thévenin equivalent and (*b*) the Norton equivalent of the circuit to the right of terminals a, b.

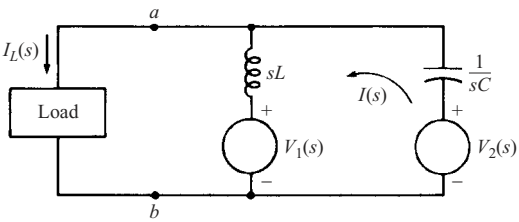


Fig. 1-18

(*a*) With terminals a, b open-circuited, only loop current $I(s)$ flows; by KVL and Ohm's law, with all currents and voltages understood to be functions of s, we have

$$I = \frac{V_2 - V_1}{sL + 1/sC}$$

Now KVL gives

$$V_{Th} = V_{ab} = V_1 + sLI = V_1 + \frac{sL(V_2 - V_1)}{sL + 1/sC} = \frac{V_1 + s^2LCV_2}{s^2LC + 1}$$

With the independent sources deactivated, the Thévenin impedance can be determined as

$$Z_{Th} = sL \| \frac{1}{sC} = \frac{sL(1/sC)}{sL + 1/sC} = \frac{sL}{s^2LC + 1}$$

(*b*) The Norton current can be found as

$$I_N = \frac{V_{Th}}{Z_{Th}} = \frac{\dfrac{V_1 + s^2LCV_2}{s^2LC + 1}}{\dfrac{sL}{s^2LC + 1}} = \frac{V_1 + s^2LCV_2}{sL}$$

and the Norton admittance as

$$Y_N = \frac{1}{Z_{Th}} = \frac{s^2LC + 1}{sL}$$

1.11 Determine the z parameters for the two-port network of Fig. 1-19.

For $I_2 = 0$, by Ohm's law,

$$I_a = \frac{V_1}{10 + 6} = \frac{V_1}{16}$$

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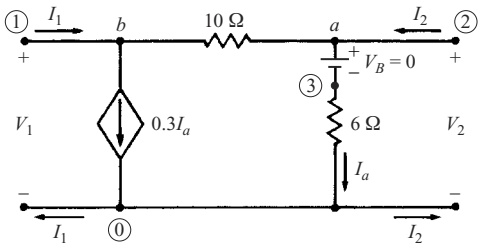


Fig. 1-19

Also, at node b, KCL gives

$$I_1 = 0.3I_a + I_a = 1.3I_a = 1.3\,\frac{V_1}{16} \tag{1}$$

Thus, by (*1.10*),

$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = \frac{16}{1.3} = 12.308\,\Omega$$

Further, again by Ohm's law,

$$I_a = \frac{V_2}{6} \tag{2}$$

Substitution of (*2*) into (*1*) yields

$$I_1 = 1.3\,\frac{V_2}{6}$$

so that, by (*1.12*),

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} = \frac{6}{1.3} = 4.615\,\Omega$$

Now with $I_1 = 0$, applying KCL at node a gives us

$$I_2 = I_a + 0.3I_a = 1.3I_a \tag{3}$$

The application of KVL then leads to

$$V_1 = V_2 - (10)(0.3I_a) = 6I_a - 3I_a = 3I_a = \frac{3I_2}{1.3}$$

so that, by (*1.11*),

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} = \frac{3}{1.3} = 2.308\,\Omega$$

Now, substitution of (*2*) in (*3*) gives

$$I_2 = 1.3I_a = 1.3\,\frac{V_2}{6}$$

Hence, from (*1.13*),

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} = \frac{6}{1.3} = 4.615\,\Omega$$

1.12 Solve Problem 1.11 using a SPICE method similar to that of Example 1.9.

The SPICE netlist code is

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```
Prb1_12.CIR z-parameter evaluation
.PARAM I1value=1mA I2value=0mA
I1 0 1 AC {I1value}
F  1 0 VB 0.3
R1 1 2 10ohm
VB 2 3 0V ; Current sense
R2 3 0 6ohm
I2 0 2 AC {I2value}
.DC I1 0 1mA 1mA I2 1mA 0 1mA ; Nested loop
.PRINT DC V(1) I(I1) V(2) I(I2)
.END
```

A nested loop is used in the .DC statement to eliminate the need for two separate executions. As a consequence, data is generated for $I1 = I2 = 1\text{mA}$ and $I1 = I2 = 0$, which is extraneous to the problem.

Execute <Prb1_12.CIR> and poll the output file to obtain data to evaluate the z parameters by use of (*1.10*) to (*1.13*).

$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = \left.\frac{V(1)}{I(I1)}\right|_{I(I2)=0} = \frac{1.231 \times 10^{-2}}{1 \times 10^{-3}} = 12.31\,\Omega$$

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} = \left.\frac{V(1)}{I(I2)}\right|_{I(I1)=0} = \frac{2.308 \times 10^{-3}}{1 \times 10^{-3}} = 2.308\,\Omega$$

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} = \left.\frac{V(2)}{I(I1)}\right|_{I(I1)=0} = \frac{4.615 \times 10^{-3}}{1 \times 10^{-3}} = 4.615\,\Omega$$

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} = \left.\frac{V(2)}{I(I2)}\right|_{I(I1)=0} = \frac{4.615 \times 10^{-3}}{1 \times 10^{-3}} = 4.615\,\Omega$$

1.13 Determine the h parameters for the two-port network of Fig. 1-19.

For $V_2 = 0$, $I_a \equiv 0$; thus, $I_1 = V_1/10$ and, by (*1.16*),

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} = 10\,\Omega$$

Further, $I_2 = -I_1$ and, by (*1.18*),

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} = -1$$

Now, $I_a = V_2/6$. With $I_1 = 0$, KVL yields

$$V_1 = V_2 - 10(0.3I_a) = V_2 - 10(0.3)\frac{V_2}{6} = \frac{1}{2}V_2$$

and, from (*1.17*),

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} = 0.5$$

Finally, applying KCL at node a gives

$$I_2 = I_a + 0.3I_a = 1.3\frac{V_2}{6}$$

so that, by (*1.19*),

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} = \frac{1.3}{6} = 0.2167\,\text{S}$$

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1.14 Use (*1.8*), (*1.9*), and (*1.16*) to (*1.19*) to find the h parameters in terms of the z parameters.

Setting $V_2 = 0$ in (*1.9*) gives

$$0 = z_{21}I_1 + z_{22}I_2 \qquad \text{or} \qquad I_2 = -\frac{z_{21}}{z_{22}}I_1 \tag{1}$$

from which we get

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} = -\frac{z_{21}}{z_{22}}$$

Back substitution of (*1*) into (*1.8*) and use of (*1.16*) give

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} = z_{11} - \frac{z_{12}z_{21}}{z_{22}}$$

Now, with $I_1 = 0$, (*1.8*) and (*1.9*) become

$$V_1 = z_{12}I_2 \qquad \text{and} \qquad V_2 = z_{22}I_2$$

so that, from (*1.17*),

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} = \frac{z_{12}}{z_{22}}$$

and, from (*1.19*),

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} = \frac{I_2}{z_{22}I_2} = \frac{1}{z_{22}}$$

1.15 The h parameters of the two-port network of Fig. 1-20 are $h_{11} = 100\,\Omega$, $h_{12} = 0.0025$, $h_{21} = 20$, and $h_{22} = 1\,\text{mS}$. Find the voltage-gain ratio V_2/V_1.

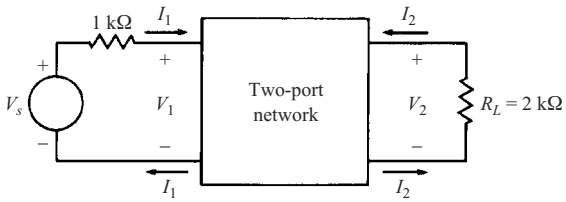


Fig. 1-20

By Ohm's law, $I_2 = -V_2/R_L$, so that (*1.15*) may be written

$$-\frac{V_2}{R_L} = I_2 = h_{21}I_1 + h_{22}V_2$$

Solving for I_1 and substitution into (*1.14*) give

$$V_1 = h_{11}I_1 + h_{12}V_2 = \frac{-(1/R_L + h_{22})}{h_{21}}V_2h_{22} + h_{12}V_2$$

which can be solved for the voltage gain ratio:

$$\frac{V_2}{V_1} = \frac{1}{h_{12} - (h_{11}/h_{21})(1/R_L + h_{22})} = \frac{1}{0.0025 - (100/20)(1/2000 + 0.001)} = -200$$

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1.16 Determine the Thévenin equivalent voltage and impedance looking right into port 1 of the circuit of Fig. 1-20.

The Thévenin voltage is V_1 of (*1.8*) with port 1 open-circuited:

$$V_{Th} = V_1|_{I_1=0} = z_{12}I_2 \tag{1}$$

Now, by Ohm's law,

$$V_2 = -R_L I_2 \tag{2}$$

But, with $I_1 = 0$, (*1.9*) reduces to

$$V_2 = z_{22}I_2 \tag{3}$$

Subtracting (*2*) from (*3*) leads to

$$(z_{22} + R_L)I_2 = 0 \tag{4}$$

Since, in general, $z_{22} + R_L \neq 0$, we conclude from (*4*) that $I_2 = 0$ and, from (*1*), $V_{Th} = 0$.

Substituting (*2*) into (*1.8*) and (*1.9*) gives

$$V_1 = z_{11}I_1 + z_{12}I_2 = z_{11}I_1 - \frac{z_{12}}{R_L}V_2 \tag{5}$$

and

$$V_2 = z_{21}I_1 + z_{22}I_2 = z_{21}I_1 - \frac{z_{22}}{R_L}V_2 \tag{6}$$

V_1 is found by solving for V_2 and substituting the result into (*5*):

$$V_1 = z_{11}I_1 - \frac{z_{12}z_{21}}{z_{22} + R_L}I_1$$

Then Z_{Th} is calculated as the driving-point impedance V_1/I_1:

$$Z_{Th} = \frac{V_{dp}}{I_{dp}} = \frac{V_1}{I_1} = z_{11} - \frac{z_{12}z_{21}}{z_{22} + R_L}$$

1.17 Find the Thévenin equivalent voltage and impedance looking into port 1 of the circuit of Fig. 1-20 if R_L is replaced with a current-controlled voltage source such that $V_2 = \beta I_1$, where β is a constant.

As in Problem 1.16,

$$V_{Th} = V_1|_{I_1=0} = z_{22}I_2$$

But if $I_1 = 0$, (*1.9*) and the defining relationship for the controlled source lead to

$$V_2 = \beta I_1 = 0 = z_{22}I_2$$

from which $I_2 = 0$ and, hence, $V_{Th} = 0$.

Now we let $V_1 = V_{dp}$, so that $I_1 = I_{dp}$, and we determine Z_{Th} as the driving-point impedance. From (*1.8*), (*1.9*), and the defining relationship for the controlled source, we have

$$V_1 = V_{dp} = z_{11}I_{dp} + z_{12}I_2 \tag{1}$$
$$V_2 = \beta I_{dp} = z_{21}I_{dp} + z_{22}I_2 \tag{2}$$

Solving (*2*) for I_2 and substituting the result into (*1*) yields

$$V_{dp} = z_{11}I_{dp} + z_{12}\frac{\beta - z_{21}}{z_{22}}I_{dp}$$

from which Thévenin impedance is found to be

$$Z_{Th} = \frac{V_{dp}}{I_{dp}} = \frac{z_{11}z_{22} + z_{12}(\beta - z_{21})}{z_{22}}$$

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1.18 The periodic current waveform of Fig. 1-21 is composed of segments of a sinusoid. Find (*a*) the average value of the current and (*b*) the rms (effective) value of the current.

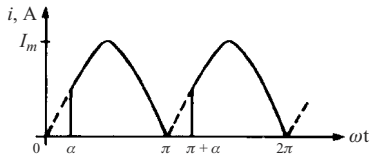


Fig. 1-21

(*a*) Because $i(t) = 0$ for $0 \le \omega t < \alpha$, the average value of the current is, according to (*1.20*),

$$I_0 = \frac{1}{\pi}\int_{\alpha}^{\pi} I_m \sin\omega t\, d(\omega t) = \frac{I_m}{\pi}\left[-\cos\omega t\right]_{\omega t=\alpha}^{\pi} = \frac{I_m}{\pi}(1+\cos\alpha)$$

(*b*) By (*1.21*) and the identity $\sin^2 x = \frac{1}{2}(1-\cos 2x)$,

$$I^2 = \frac{1}{\pi}\int_{\alpha}^{\pi} I_m^2 \sin^2(\omega t)\, d(\omega t) = \frac{I_m^2}{2\pi}\int_{\alpha}^{\pi}(1-\cos 2\omega t)\, d(\omega t)$$
$$= \frac{I_m^2}{2\pi}\left[\omega t - \frac{1}{2}\sin 2\omega t\right]_{\omega t=\alpha}^{\pi} = \frac{I_m^2}{2\pi}\left(\pi - \alpha + \frac{1}{2}\sin 2\alpha\right)$$

so that

$$I = I_m\sqrt{\frac{\pi - \alpha + \frac{1}{2}\sin 2\alpha}{2\pi}}$$

1.19 Assume that the periodic waveform of Fig. 1-22 is a current (rather than a voltage). Find (*a*) the average value of the current and (*b*) the rms value of the current.

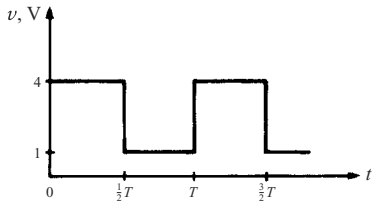


Fig. 1-22

(*a*) The integral in (*1.20*) is simply the area under the $f(t)$ curve for one period. We can, then, find the average current as

$$I_0 = \frac{1}{T}\left(4 \times \frac{T}{2} + 1 \times \frac{T}{2}\right) = 2.5\,\text{A}$$

(*b*) Similarly, the integral in (*1.21*) is no more than the area under the $f^2(t)$ curve. Hence,

$$I = \left[\frac{1}{T}\left(4^2\,\frac{T}{2} + 1^2\,\frac{T}{2}\right)\right]^{1/2} = 4.25\,\text{A}$$

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1.20 Calculate the average and rms values of the current $i(t) = 4 + 10 \sin \omega t$ A.

Since $i(t)$ has period 2π, (*1.20*) gives

$$I_0 = \frac{1}{2\pi} \int_0^{2\pi} (4 + 10 \sin \omega t)\, d(\omega t) = \frac{1}{2\pi} [4\omega t - 10 \cos \omega t]_{\omega t=0}^{2\pi} = 4 \text{ A}$$

This result was to be expected, since the average value of a sinusoid over one cycle is zero.

Equation (*1.21*) and the identity $\sin^2 x = \frac{1}{2}(1 - \cos 2x)$ provide the rms value of $i(t)$:

$$I^2 = \frac{1}{2\pi} \int_0^{2\pi} (4 + 10 \sin \omega t)^2\, d(\omega t) = \frac{1}{2\pi} \int_0^{2\pi} (16 + 80 \sin \omega t + 50 - 50 \cos 2\omega t)\, d(\omega t)$$
$$= \frac{1}{2\pi} \left[66\omega t - 80 \cos \omega t - \frac{50}{2} \sin 2\omega t \right]_{\omega t=0}^{2\pi} = 66$$

so that $I = \sqrt{66} = 8.125$ A.

1.21 Find the rms (or effective) value of a current consisting of the sum of two sinusoidally varying functions with frequencies whose ratio is an integer.

Without loss of generality, we may write

$$i(t) = I_1 \cos \omega t + I_2 \cos k\omega t$$

where k is an integer. Applying (*1.21*) and recalling that $\cos^2 x = \frac{1}{2}(1 + \cos 2x)$ and $\cos x \cos y = \frac{1}{2}[\cos(x + y) + \cos(x - y)]$, we obtain

$$I^2 = \frac{1}{2\pi} \int_0^{2\pi} (I_1 \cos \omega t + I_2 \cos k\omega t)^2\, d(\omega t)$$
$$= \frac{1}{2\pi} \int_0^{2\pi} \left\{ \frac{I_1^2}{2} (1 + \cos 2\omega t) + \frac{I_2^2}{2} (1 + \cos 2k\omega t) + I_1 I_2 [\cos(k+1)\omega t + \cos(k-1)\omega t] \right\} d(\omega t)$$

Performing the indicated integration and evaluating at the limits results in

$$I = \sqrt{\frac{I_1^2}{2} + \frac{I_2^2}{2}}$$

1.22 Find the average value of the power delivered to a one-port network with *passive sign convention* (that is, the current is directed from the positive to the negative terminal) if $v(t) = V_m \cos \omega t$ and $i(t) = I_m \cos(\omega t + \theta)$.

The instantaneous power flow into the port is given by

$$p(t) = v(t) i(t) = V_m I_m \cos \omega t \cos(\omega t + \theta)$$
$$= \tfrac{1}{2} V_m I_m [\cos(2\omega t + \theta) + \cos \theta]$$

By (*1.20*),

$$P_0 = \frac{1}{2\pi} \int_0^{2\pi} p(t)\, dt = \frac{V_m}{4\pi} I_m \int_0^{2\pi} [\cos(2\omega t + \theta) + \cos \theta]\, d(\omega t)$$

After the integration is performed and its limits evaluated, the result is

$$P_0 = \frac{V_m I_m}{2} \cos \theta = \frac{V_m}{\sqrt{2}} \frac{I_m}{\sqrt{2}} \cos \theta = VI \cos \theta$$

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Supplementary Problems

1.23 Prove that the capacitor element of Fig. 1-1(*c*) is a linear element by showing that it satisfies the converse of the superposition theorem. (*Hint*: See Problem 1.1.)

1.24 Use the superposition theorem to find the current i in Fig. 1-14 if $R_1 = 5\,\Omega$, $R_2 = 10\,\Omega$, $V_s = 10\cos 2t$ V, and $I_s = 3\cos(3t + \pi/4)$ A. *Ans.* $i = 0.667\cos 2t + \cos(3t + \pi/4)$ A

1.25 In Fig. 1-23, (*a*) find the Thévenin equivalent voltage and impedance for the network to the left of terminals a, b, and (*b*) use the Thévenin equivalent circuit to determine the current I_L.
Ans. (*a*) $V_{Th} = V_1 - I_2R_2, Z_{Th} = R_1 + R_2$; (*b*) $I_L = (V_1 - I_2R_2)/(R_1 + R_2 + R_L)$

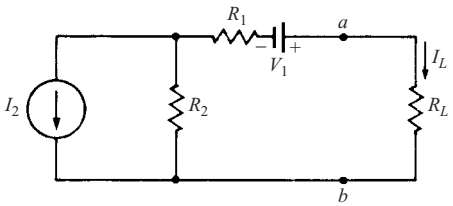


Fig. 1-23

1.26 In the circuit of Fig. 1-18, $V_1 = 10\cos 2t$ V, $V_2 = 20\cos 2t$ V, $L = 1$ H, $C = 1$ F, and the load is a 1-Ω resistor. (*a*) Determine the Thévenin equivalent for the network to the right of terminals a, b. (*b*) Use the Thévenin equivalent to find the load current $\bar{I}_L$. (*Hint*: The results of Problem 1.10 can be used here with $s = j2$.) *Ans.* (*a*) $\bar{V}_{Th} = 23.333\angle 0^\circ$ V, $Z_{Th} = -j0.667\,\Omega$; (*b*) $\bar{I}_L = 19.4\angle 33.69^\circ$ A.

1.27 In Fig. 1-24, find the Thévenin equivalent for the bridge circuit as seen through the load resistor R_L.
Ans. $V_{Th} = V_b(R_2R_3 - R_1R_4)/(R_1 + R_2)(R_3 + R_4), Z_{Th} = R_1R_2/(R_1 + R_3) + R_2R_4/(R_2 + R_4)$

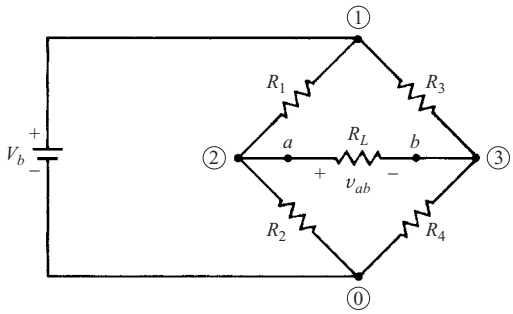


Fig. 1-24

1.28 Suppose the bridge circuit in Fig. 1-24 is balanced by letting $R_1 = R_2 = R_3 = R_4 = R$. Find the elements of the Norton equivalent circuit. *Ans.* $I_N = 0, Y_N = 1/R$

1.29 Use SPICE methods to determine voltage v_{ab} for the circuit of Fig. 1-24 if $V_b = 20$ V, $R_L = 10\,\Omega$, $R_1 = 1\,\Omega$, $R_2 = 2\,\Omega$, $R_3 = 3\,\Omega$, and $R_4 = 4\,\Omega$. (*Netlist code available at author download site.*)
Ans. $v_{ab} = V(2, 3) = 1.538$ V

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1.30 For the circuit of Fig. 1-25, (*a*) determine the Thévenin equivalent of the circuit to the left of terminals *a*, *b*, and (*b*) use the Thévenin equivalent to find the load current i_L.
Ans. (*a*) $V_{Th} = 120\,\text{V}, Z_{Th} = 20\,\Omega$; (*b*) $i_L = 4\,\text{A}$

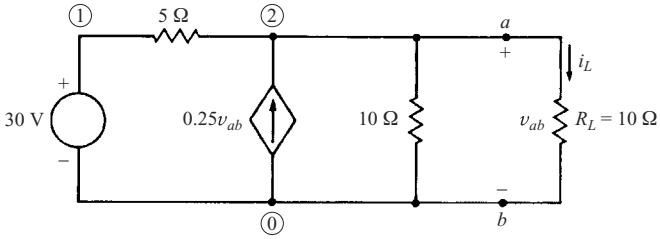


Fig. 1-25

1.31 Apply SPICE methods to determine load current i_L for the circuit of Fig. 1-25 if (*a*) the element values are as shown and (*b*) the VCCS has a value of $0.5v_{ab}$ with all else unchanged. (*Netlist code available at author download site.*) *Ans.* (*a*) $i_L = 4\,\text{A}$; (*b*) $i_L = -6\,\text{A}$

1.32 In the circuit of Fig. 1-26, let $R_1 = R_2 = R_C = 1\,\Omega$ and find the Thévenin equivalent for the circuit to the right of terminals *a*, *b* (*a*) if $v_C = 0.5i_1$ and (*b*) if $v_C = 0.5i_2$.
Ans. (*a*) $V_{Th} = 0, Z_{Th} = R_{Th} = 1.75\,\Omega$; (*b*) $V_{Th} = 0, Z_{Th} = R_{Th} = 1.667\,\Omega$

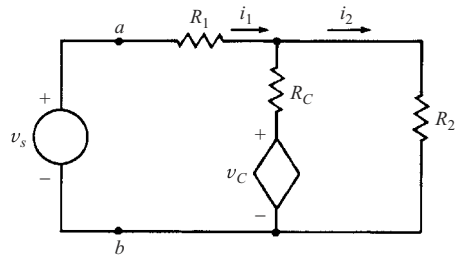


Fig. 1-26

1.33 Find the Thévenin equivalent for the network to the left of terminals *a*, *b* in Fig. 1-15 (*a*) if $k = 0$, and (*b*) if $k = 0.1$. Use the Thévenin equivalent to verify the results of Problem 1.4.
Ans. (*a*) $V_{Th} = -200\,\text{V}, Z_{Th} = R_{Th} = 100\,\Omega$; (*b*) $V_{Th} = -250\,\text{V}, Z_{Th} = R_{Th} = 125\,\Omega$

1.34 Find the Thévenin equivalent for the circuit to the left of terminals *a*, *b* in Fig. 1-16, and use it to verify the results of Problem 1.6. *Ans.* $V_{Th} = \frac{1}{2}(1+\alpha)v_s, Z_{Th} = R_{Th} = \frac{1}{2}(3-\alpha)\,\Omega$

1.35 An alternative solution for Problem 1.3 involves finding a Thévenin equivalent circuit which, when connected across the nonlinear $R_2 = 0.25i$, allows a quadratic equation in current i to be written via KVL. Find the elements of the Thévenin circuit and the resulting current.
Ans. $V_{Th} = 25\,\text{V}, Z_{Th} = R_{Th} = 5\,\Omega, i = 4.142\,\text{A}$

1.36 Use (*1.10*) to (*1.15*) to find expressions for the *z* parameters in terms of the *h* parameters.
Ans. $z_{11} = h_{11} - h_{12}h_{21}/h_{22}, z_{12} = h_{12}/h_{22}, z_{21} = -h_{21}/h_{22}, z_{22} = 1/h_{22}$

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1.37 For the two-port network of Fig. 1-20, (*a*) find the voltage-gain ratio V_2/V_1 in terms of the z parameters, and then (*b*) evaluate the ratio, using the h-parameter values given in Problem 1.15 and the results of Problem 1.36. *Ans.* (*a*) $z_{21}R_L/(z_{11}R_L + z_{11}z_{22} - z_{12}z_{21})$; (*b*) -200

1.38 Find the current-gain ratio I_2/I_1 for the two-port network of Fig. 1-20 in terms of the h parameters.
Ans. $h_{21}/(1 + h_{22}R_L)$

1.39 Find the current-gain ratio I_2/I_1 for the two-port network of Fig. 1-20 in terms of the z parameters.
Ans. $-z_{21}/(z_{22} + R_L)$

1.40 Determine the Thévenin equivalent voltage and impedance, in terms of the z parameters, looking right into port 1 of the two-port network of Fig. 1-20 if R_L is replaced with an independent dc voltage source V_d, connected such that $V_2 = V_d$. *Ans.* $V_{Th} = z_{12}V_d/z_{22}$, $Z_{Th} = (z_{11}z_{22} - z_{12}z_{21})/z_{22}$

1.41 Find the Thévenin equivalent voltage and impedance, in terms of the h parameters, looking right into port 1 of the network of Fig. 1-20 if R_L is replaced with a voltage-controlled current source such that $I_2 = -\alpha V_1$, where $\alpha > 0$ and the h parameters are understood to be positive.
Ans. $V_{Th} = 0$, $Z_{Th} = (h_{11}h_{22} - h_{12}h_{21})/(h_{22} + \alpha h_{12})$

1.42 Determine the driving-point impedance (the input impedance with all independent sources deactivated) of the two-port network of Fig. 1-20. *Ans.* $(z_{11}R_L + z_{11}z_{22} - z_{12}z_{21})/(z_{22} + R_L)$

1.43 Evaluate the z parameters of the network of Fig. 1-16.
Ans. $z_{11} = 2\,\Omega$, $z_{12} = 1\,\Omega$, $z_{21} = \alpha + 1\,\Omega$, $z_{22} = 2\,\Omega$

1.44 Find the current i_1 in Fig. 1-3 if $\alpha = 2$, $R_1 = R_2 = R_3 = 1\,\Omega$, $V_b = 10\,\text{V}$, and $v_s = 10 \sin \omega t\,\text{V}$.
Ans. $-2\,\text{A}$

1.45 For a one-port network with passive sign convention (see Problem 1.22), $v = V_m \cos \omega t\,\text{V}$ and $i = I_1 + I_2 \cos(\omega t + \theta)\,\text{A}$. Find (*a*) the instantaneous power flowing to the network and (*b*) the average power to the network. *Ans.* (*a*) $V_m I_1 \cos \omega t + \frac{1}{2} V_m I_2[\cos(2\omega t + \theta) + \cos \theta]$; (*b*) $\frac{1}{2} V_m I_2 \cos \theta$

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CHAPTER 2

Semiconductor Diodes

2.1. INTRODUCTION

Diodes are among the oldest and most widely used of electronic devices. A *diode* may be defined as a near-unidirectional conductor whose state of conductivity is determined by the polarity of its terminal voltage. The subject of this chapter is the *semiconductor diode*, formed by the metallurgical junction of *p*-type and *n*-type materials. (A *p*-type material is a group-IV element *doped* with a small quantity of a group-V material; *n*-type material is a group-IV base element doped with a group-III material.)

2.2. THE IDEAL DIODE

The symbol for the *common*, or *rectifier*, *diode* is shown in Fig. 2-1(*a*). The device has two terminals, labeled *anode* (*p*-type) and *cathode* (*n*-type), which makes understandable the choice of *diode* as its name. When the terminal voltage is nonnegative ($v_D \geq 0$), the diode is said to be *forward-biased* or "on"; the positive current that flows ($i_D \geq 0$) is called *forward current*. When $v_D < 0$, the diode is said to be *reverse-biased* or "off," and the corresponding small negative current is referred to as *reverse current*.

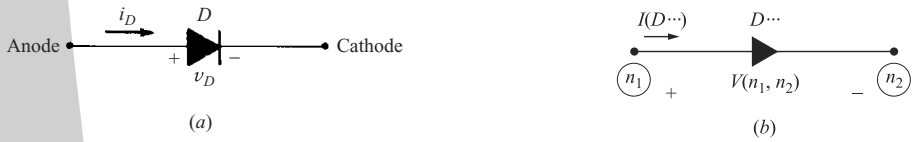


Fig. 2-1

The ideal diode is a perfect two-state device that exhibits zero impedance when forward-biased and infinite impedance when reverse-biased (Fig. 2-2). Note that since either current or voltage is zero at any instant, no power is dissipated by an ideal diode. In many circuit applications, diode forward voltage drops and reverse currents are small compared to other circuit variables; then, sufficiently accurate results are obtained if the actual diode is modeled as ideal.

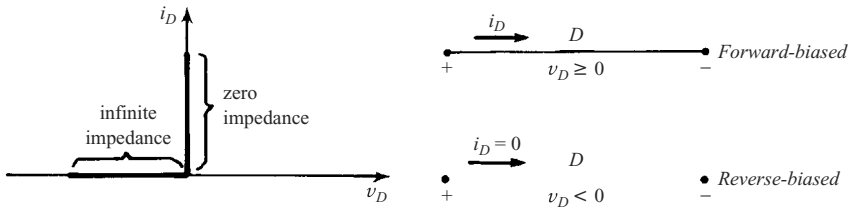
The *ideal diode analysis procedure* is as follows:

Step 1: Assume forward bias, and replace the ideal diode with a short circuit.

Step 2: Evaluate the diode current i_D, using any linear circuit-analysis technique.

Step 3: If $i_D \geq 0$, the diode is actually forward-biased, the analysis is valid, and step 4 is to be omitted.

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(*a*) Terminal characteristics (*b*) Circuit models

Fig. 2-2 Ideal diode

Step 4: If $i_D < 0$, the analysis so far is invalid. Replace the diode with an open circuit, forcing $i_D = 0$, and solve for the desired circuit quantities using any method of circuit analysis. Voltage v_D must be found to have a negative value.

Example 2.1. Find voltage v_L in the circuit of Fig. 2-3(*a*), where D is an ideal diode.

The analysis is simplified if a Thévenin equivalent is found for the circuit to the left of terminals a, b; the result is

$$v_{Th} = \frac{R_1}{R_1 + R_S} v_s \qquad \text{and} \qquad Z_{Th} = R_{Th} = R_1 \| R_S = \frac{R_1 R_S}{R_1 + R_S}$$

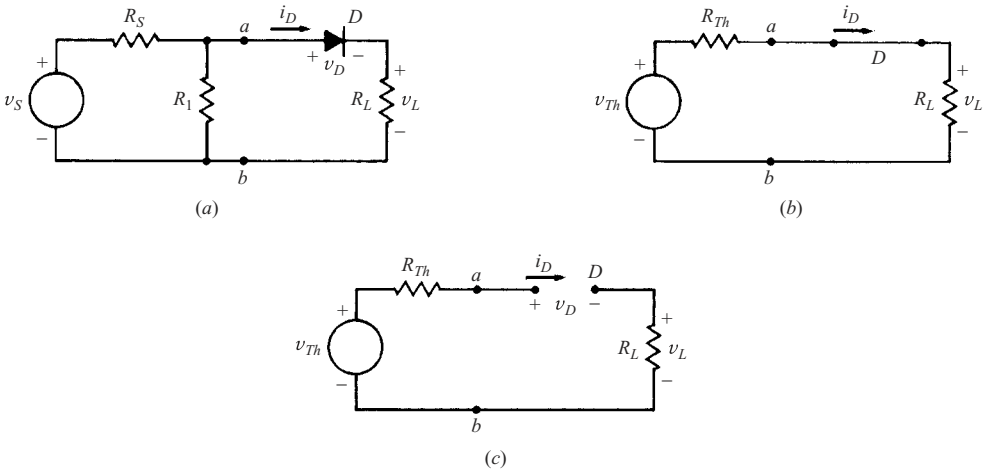


Fig. 2-3

Step 1: After replacing the network to the left of terminals a, b with the Thévenin equivalent, assume forward bias and replace diode D with a short circuit, as in Fig. 2-3(*b*).

Step 2: By Ohm's law,

$$i_D = \frac{v_{Th}}{R_{Th} + R_L}$$

Step 3: If $v_S \geq 0$, then $i_D \geq 0$ and

$$v_L = i_D R_L = \frac{R_L}{R_L + R_{Th}} v_{Th}$$

Step 4: If $v_S < 0$, then $i_D < 0$ and the result of step 3 is invalid. Diode D must be replaced by an open circuit as illustrated in Fig. 2-3(*c*), and the analysis performed again. Since now $i_D = 0$, $v_L = i_D R_L = 0$. Since $v_D = v_S < 0$, the reverse bias of the diode is verified.

(See Problem 2.4 for an extension of this procedure to a multidiode circuit.)

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2.3. DIODE TERMINAL CHARACTERISTICS

Use of the Fermi-Dirac probability function to predict charge neutralization gives the *static* (non-time-varying) equation for diode junction current:

$$i_D = I_o(e^{v_D/\eta V_T} - 1) \quad \text{A} \tag{2.1}$$

where $V_T \equiv kT/q$, V
$v_D \equiv$ diode terminal voltage, V
$I_o \equiv$ temperature-dependent saturation current, A
$T \equiv$ absolute temperature of p-n junction, K
$k \equiv$ Boltzmann's constant (1.38×10^{-23} J/K)
$q \equiv$ electron charge (1.6×10^{-19} C)
$\eta \equiv$ empirical constant, 1 for Ge and 2 for Si

Example 2.2. Find the value of V_T in (*2.1*) at 20°C.

Recalling that absolute zero is −273°C, we write

$$V_T = \frac{kT}{q} = \frac{(1.38 \times 10^{-23})(273 + 20)}{1.6 \times 10^{-19}} = 25.27\,\text{mV}$$

While (*2.1*) serves as a useful model of the junction diode insofar as dynamic resistance is concerned, Fig. 2-4 shows it to have regions of inaccuracy:

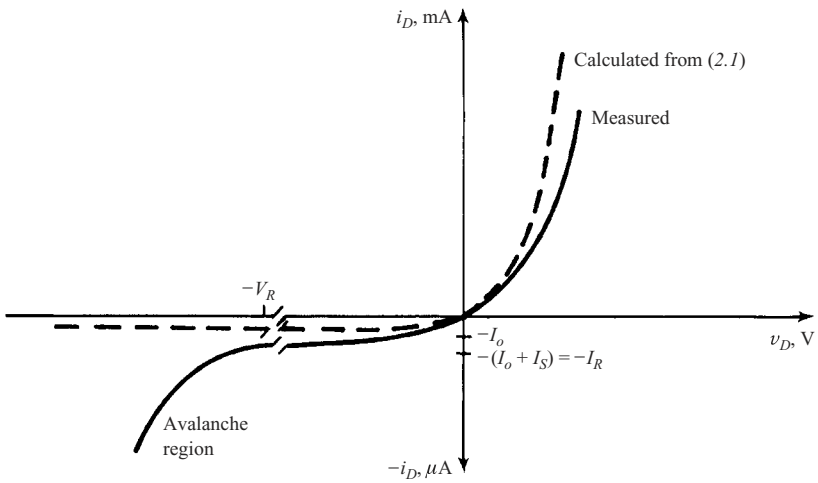


Fig. 2-4

1. The actual (measured) forward voltage drop is greater than that predicted by (*2.1*) (due to ohmic resistance of metal contacts and semiconductor material).
2. The actual reverse current for $-V_R \le v_D < 0$ is greater than predicted (due to leakage current I_S along the surface of the semiconductor material).
3. The actual reverse current increases to significantly larger values than predicted for $v_D < -V_R$ (due to a complex phenomenon called *avalanche breakdown*).

In commercially available diodes, proper doping (impurity addition) of the base material results in distinct static terminal characteristics. A comparison of Ge- and Si-base diode characteristics is shown in Fig. 2-5. If $-V_R < v_D < -0.1$ V, both diode types exhibit a near-constant reverse current I_R. Typically, $1\,\mu\text{A} < I_R < 500\,\mu\text{A}$

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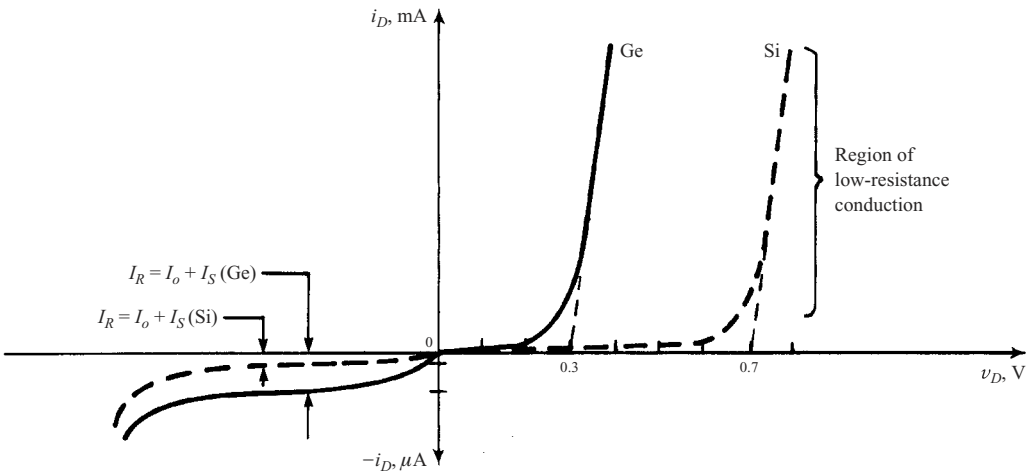


Fig. 2-5

for Ge, while $10^{-3}\ \mu\text{A} < I_R < 1\ \mu\text{A}$ for Si, for signal-level diodes (forward current ratings of less than 1 A). For a forward bias, the onset of low-resistance conduction is between 0.2 and 0.3 V for Ge, and between 0.6 and 0.7 V for Si.

For both Si and Ge diodes, the saturation current I_o doubles for an increase in temperature of 10°C; in other words, the ratio of saturation current at temperature T_2 to that at temperature T_1 is

$$\frac{(I_o)_2}{(I_o)_1} = 2^{(T_2 - T_1)/10} \tag{2.2}$$

Example 2.3. Find the percentage increase in the reverse saturation current of a diode if the temperature is increased from 25°C to 50°C.

By (*2.2*),

$$\frac{(I_o)_2}{(I_o)_1} = 2^{(50-25)/10} \times 100\% = 565.7\%$$

Static terminal characteristics are generally adequate for describing diode operation at low frequency. However, if high-frequency analysis (above 100 kHz) or switching analysis is to be performed, it may be necessary to account for the small *depletion capacitance* (typically several picofarads) associated with a reverse-biased *p-n* junction; for a forward-biased *p-n* junction, a somewhat larger *diffusion capacitance* (typically several hundred picofarads) that is directly proportional to the forward current should be included in the model. (See Problem 2.25.)

2.4. THE DIODE SPICE MODEL

The element specification statement for a diode must explicitly name a model even if the default model parameters are intended for use. The general form of the diode specification statement is as follows, where the *model name* is arbitrarily chosen:

$$\text{D}\cdots n_1 n_2 \quad \textit{model name}$$

Node n_1 is the anode and node n_2 is the cathode of the diode. Positive current and voltage directions are clarified by Fig. 2-1(*b*).

In addition, the .MODEL control statement must be added to the netlist code even if the default parameters are acceptable. This control statement is

$$\text{.MODEL } \textit{model name } \text{D } (\textit{parameters})$$

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If the parameters field is left blank, default values are assigned. Otherwise, the parameters field contains the number of desired specifications in the format *parameter name* = *value*. Specific parameters that are of concern in this book are documented by Table 2-1.

Table 2-1

Parameter	Description	Reference	Default	Units
Is	saturation current	I_o of (2.1)	1×10^{-14}	A
n	emission coefficient	η of (2.1)	1	
BV	reverse breakdown voltage	V_R of Fig. 2-4	∞	V
IBV	reverse breakdown current	I_R of Fig. 2-4	1×10^{-10}	A
Rs	ohmic resistance	Section 2.3	0	Ω

Example 2.4. The circuit of Fig. 2-6(*a*) can be used to determine the static characteristic of diode D provided that the ramp of source v_s spans sufficient time so that any dynamic effects are negligible. Let source v_s ramp from -5 V to 5 V over a span of 2 s. Use SPICE methods to plot the silicon diode static characteristic (*a*) if the diode is nonideal with a voltage rating of $V_R = 4$ V and (*b*) if the diode is ideal.

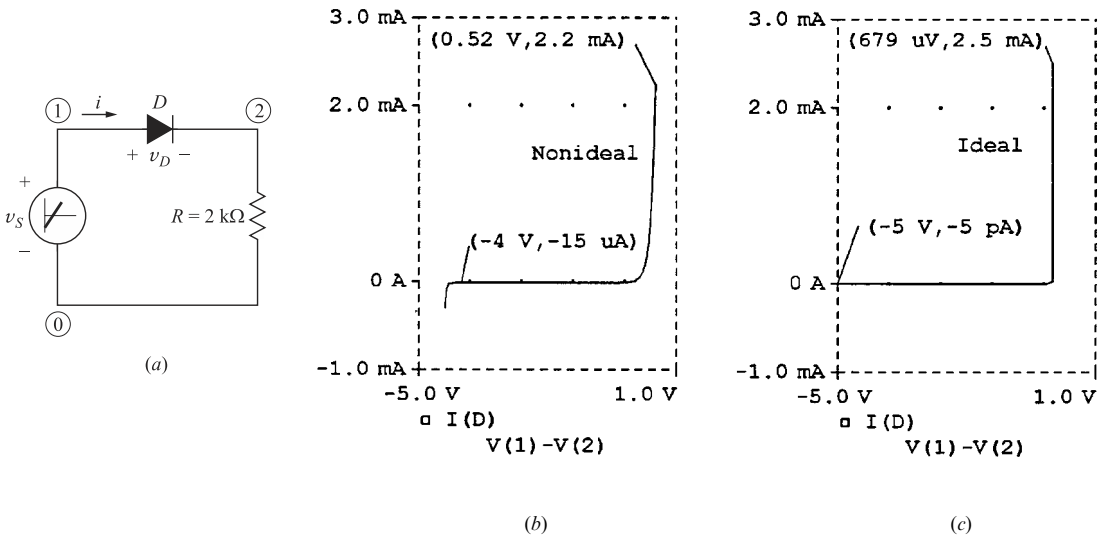


Fig. 2-6

(*a*) The SPICE netlist code below describes the nonideal diode for a typical saturation current $I_s = 15\,\mu$A. An emission coefficient $n = 4 > 2$ has been used to yield a typical forward voltage drop for a silicon diode.

```
Ex2_4.CIR - Diode static characteristic
vs 1 0 PWL (0s -5V 2s 5V)
D  1 2 DMOD
R  2 0 2kohms
.MODEL DMOD D(n=4 Is=15uA BV=4) ; Nonideal
*.MODEL DMOD D(n=0.0001) ; Ideal
.TRAN .1us 2s
.PROBE
.END
```

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After executing < Ex2_4.CIR >, I(D) is plotted with the x-axis variable changed from time to $v_D = \text{V}(1) - \text{V}(2) = \text{V}(1, 2)$ giving the static diode characteristic of Fig. 2-6(*b*).

(*b*) Edit < Ex2_4.CIR > to move the asterisk preceding the second .MODEL statement to the first .MODEL statement, thereby preparing for the ideal diode analysis. Setting the emission coefficient parameter (n) to a small value ensures a negligibly small forward voltage drop. Execute < Ex2_5.CIR > and plot the result as in part (*a*) to give the static characteristic of Fig. 2-6(*c*). Inspection of the marked points on the curve shows that the diode is approaching the ideal case of negligible reverse current and negligible forward voltage drop.

2.5. GRAPHICAL ANALYSIS

A graphical solution necessarily assumes that the diode is resistive and therefore instantaneously characterized by its static i_D-versus-v_D curve. The balance of the network under study must be linear so that a Thévenin equivalent exists for it (Fig. 2-7). Then the two simultaneous equations to be solved graphically for i_D and v_D are the diode characteristic

$$i_D = f_1(v_D) \tag{2.3}$$

and the *load line*

$$i_D = f_2(v_D) = -\frac{1}{R_{Th}} v_D + \frac{v_{Th}}{R_{Th}} \tag{2.4}$$

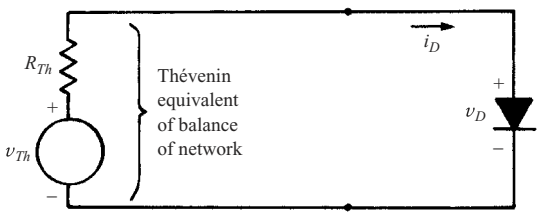


Fig. 2-7

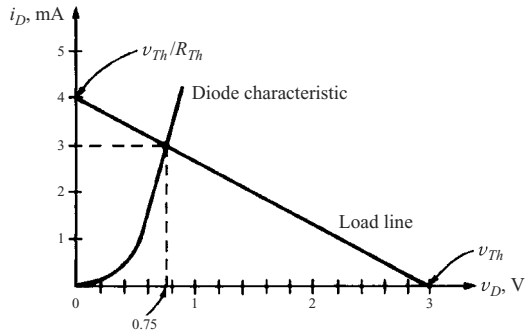


Fig. 2-8

Example 2.5. In the circuit of Fig. 2-3(*a*), $v_s = 6\,\text{V}$ and $R_1 = R_S = R_L = 500\,\Omega$. Determine i_D and v_D graphically, using the diode characteristic in Fig. 2-8.

The circuit may be reduced to that of Fig. 2-7, with

$$v_{Th} = \frac{R_1}{R_1 + R_S} v_S = \frac{500}{500 + 500} 6 = 3\,\text{V}$$

and

$$R_{Th} = R_1 \| R_S + R_L = \frac{(500)(500)}{500 + 500} + 500 = 750\,\Omega$$

Then, with these values the load line (*2.4*) must be superimposed on the diode characteristic, as in Fig. 2-8. The desired solution, $i_D = 3\,\text{mA}$ and $v_D = 0.75\,\text{V}$, is given by the point of intersection of the two plots.

Example 2.6. If all sources in the original linear portion of a network vary with time, then v_{Th} is also a time-varying source. In reduced form [Fig. 2-9(*a*)], one such network has a Thévenin voltage that is a triangular wave with a 2-V peak. Find i_D and v_D for this network.

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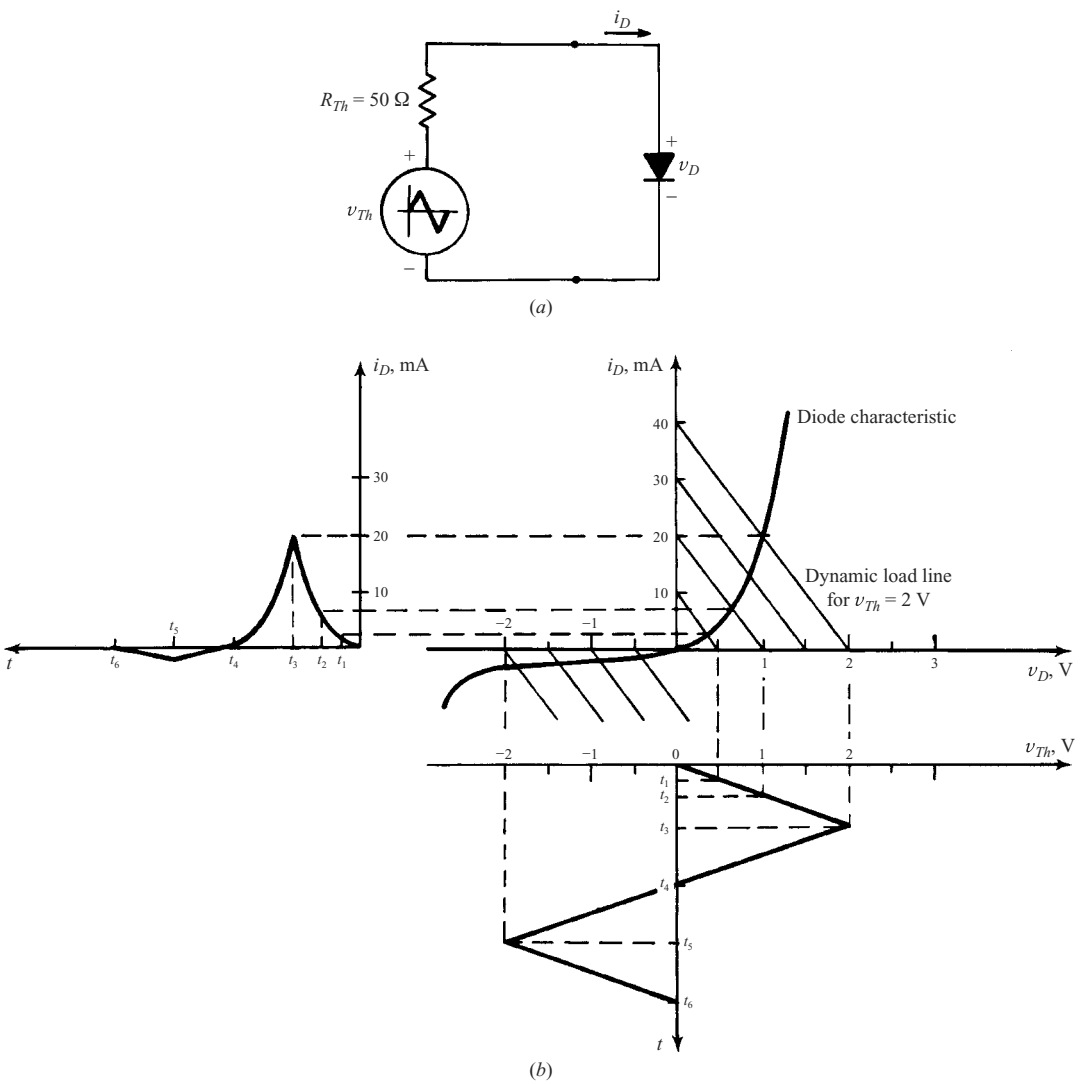


Fig. 2-9

In this case there is no unique value of i_D that satisfies the simultaneous equations (*2.3*) and (*2.4*); rather, there exists a value of i_D corresponding to each value that v_{Th} takes on. An acceptable solution for i_D may be found by considering a finite number of values of v_{Th}. Since v_{Th} is repetitive, i_D will be repetitive (with the same period), so only one cycle need be considered.

As in Fig. 2-9(*b*), we begin by laying out a scaled plot of v_{Th} versus time, with the v_{Th} axis parallel to the v_D axis of the diode characteristic. We then select a point on the v_{Th} plot, such as $v_{Th} = 0.5\,\text{V}$ at $t = t_1$. Considering time to be stopped at $t = t_1$, we construct a load line for this value on the diode characteristic plot; it intersects the v_D axis at $v_{Th} = 0.5\,\text{V}$, and the i_D axis at $v_{Th}/R_{Th} = 0.5/50 = 10\,\text{mA}$. We determine the value of i_D at which this load line intersects the characteristic, and plot the point (t_1, i_D) on a time-versus-i_D coordinate system constructed to the left of the diode characteristic curve. We then let time progress to some new value, $t = t_2$, and repeat the entire process. And we continue until one cycle of v_{Th} is completed. Since the load line is continually changing, it is referred to as a *dynamic load line*. The solution, a plot of i_D, differs drastically in form from the plot of v_{Th} because of the nonlinearity of the diode.

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Example 2.7. If both dc and time-varying sources are present in the original linear portion of a network, then v_{Th} is a series combination of a dc and a time-varying source. Suppose that the Thévenin source for a particular network combines a 0.7-V battery and a 0.1-V-peak sinusoidal source, as in Fig. 2-10(*a*). Find i_D and v_D for the network.

We lay out a scaled plot of v_{Th}, with the v_{Th} axis parallel to the v_D axis of the diode characteristic curve. We then consider v_{Th}, the ac component of v_{Th}, to be momentarily at zero ($t = 0$), and we plot a load line for this instant

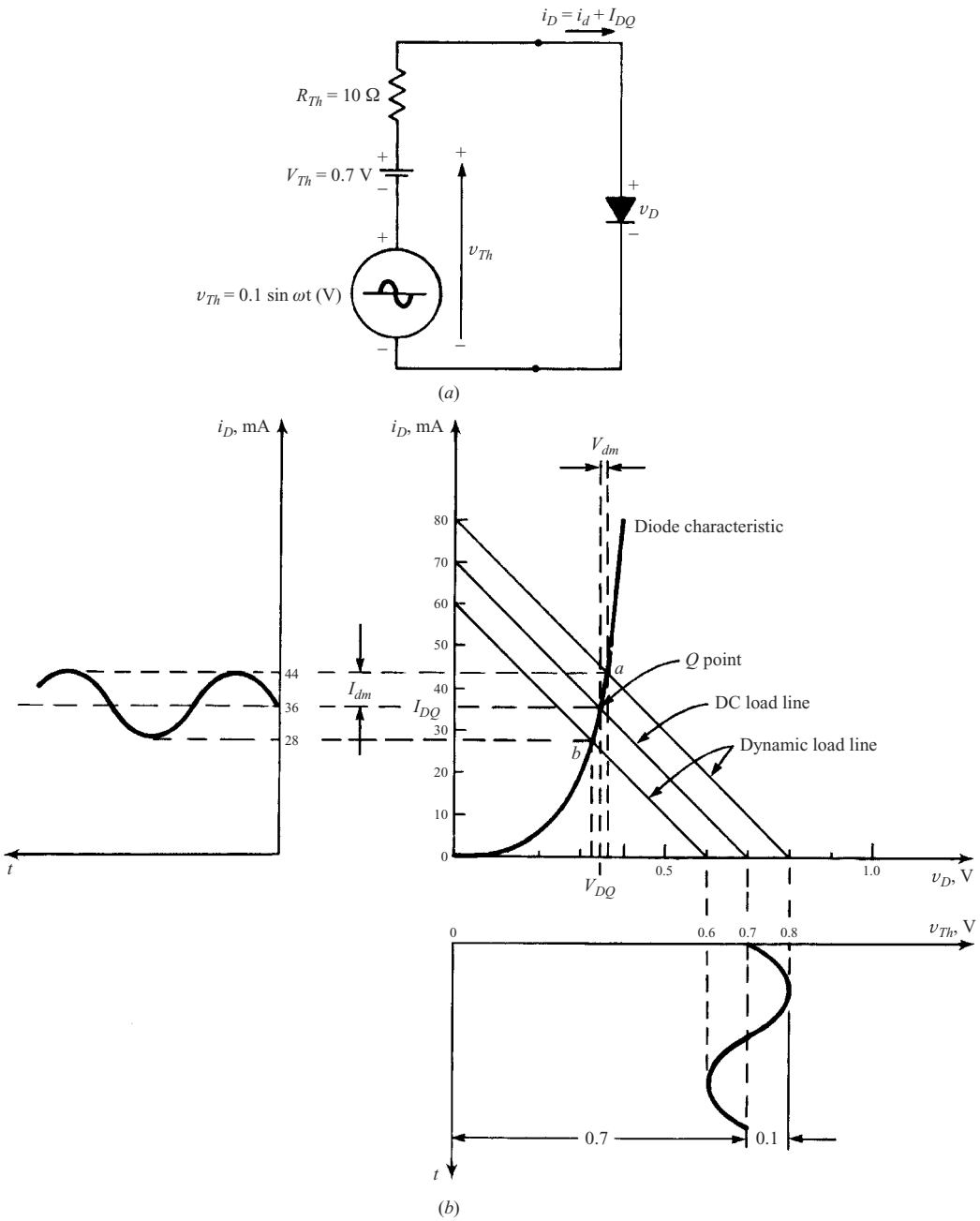


Fig. 2-10

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on the diode characteristic. This particular load line is called the *dc load line*, and its intersection with the diode characteristic curve is called the *quiescent point* or *Q point*. The values of i_D and v_D at the Q point are labeled I_{DQ} and V_{DQ}, respectively, in Fig. 2-10(*b*).

In general, a number of dynamic load lines are needed to complete the analysis of i_D over a cycle of v_{Th}. However, for the network under study, only dynamic load lines for the maximum and minimum values of v_{Th} are required. The reason is that the diode characteristic is almost a straight line near the Q point [from *a* to *b* in Fig. 2-10(*b*)], so that negligible distortion of i_d, the ac component of i_D, will occur. Thus, i_d will be of the same form as v_{Th} (i.e., sinusoidal), and it can easily be sketched once the extremes of variation have been determined. The solution for i_D is thus

$$i_D = I_{DQ} + i_d = I_{DQ} + I_{dm} \sin \omega t = 36 + 8 \sin \omega t \quad \text{mA}$$

where I_{dm} is the amplitude of the sinusoidal term.

2.6. EQUIVALENT-CIRCUIT ANALYSIS

Piecewise-Linear Techniques

In piecewise-linear analysis, the diode characteristic curve is approximated with straight-line segments. Here we shall use only the three approximations shown in Fig. 2-11, in which combinations of ideal diodes, resistors, and batteries replace the actual diode. The simplest model, in Fig. 2-11(*a*), treats the actual diode as an infinite resistance for $v_D < V_F$, and as an ideal battery if v_D tends to be greater than V_F. V_F is usually selected as 0.6 to 0.7 V for a Si diode and 0.2 to 0.3 V for a Ge diode.

If greater accuracy in the range of forward conduction is dictated by the application, a resistor R_F is introduced, as in Fig. 2-11(*b*). If the diode reverse current ($i_D < 0$) cannot be neglected, the additional refinement (R_R plus an ideal diode) of Fig. 2-11(*c*) is introduced.

Small-Signal Techniques

Small-signal analysis can be applied to the diode circuit of Fig. 2-10 if the amplitude of the ac signal v_{Th} is small enough so that the curvature of the diode characteristic over the range of operation (from *b* to *a*) may be neglected. Then the diode voltage and current may each be written as the sum of a dc signal and an *undistorted* ac signal. Furthermore, the ratio of the diode ac voltage v_d to the diode ac current i_d will be constant and equal to

$$\frac{v_d}{i_d} = \frac{2V_{dm}}{2I_{dm}} = \frac{v_D|_a - v_D|_b}{i_D|_a - i_D|_b} = \left.\frac{\Delta v_D}{\Delta i_D}\right|_Q = \left.\frac{dv_D}{di_D}\right|_Q \equiv r_d \tag{2.5}$$

where r_d is known as the *dynamic resistance* of the diode. It follows (from a linear circuit argument) that the ac signal components may be determined by analysis of the "small-signal" circuit of Fig. 2-12; if the frequency of the ac signal is large, a capacitor can be placed in parallel with r_d to model the depletion or diffusion capacitance as discussed in Section 2.3. The dc or quiescent signal components must generally be determined by graphical methods since, overall, the diode characteristic is nonlinear.

Example 2.8. For the circuit of Fig. 2-10, determine i_D.

The Q-point current I_{DQ} has been determined as 36 mA (see Example 2.7). The dynamic resistance of the diode at the Q point can be evaluated graphically:

$$r_d = \frac{\Delta v_D}{\Delta i_D} = \frac{0.37 - 0.33}{0.044 - 0.028} = 2.5\,\Omega$$

Now the small-signal circuit of Fig. 2.12 can be analyzed to find i_d:

$$i_d = \frac{v_{Th}}{R_{Th} + r_d} = \frac{0.1 \sin \omega t}{10 + 2.5} = 0.008 \sin \omega t \quad \text{A}$$

The total diode current is obtained by superposition and checks well with that found in Example 2.7:

$$i_D = I_{DQ} + i_d = 36 + 8 \sin \omega t \quad \text{mA}$$

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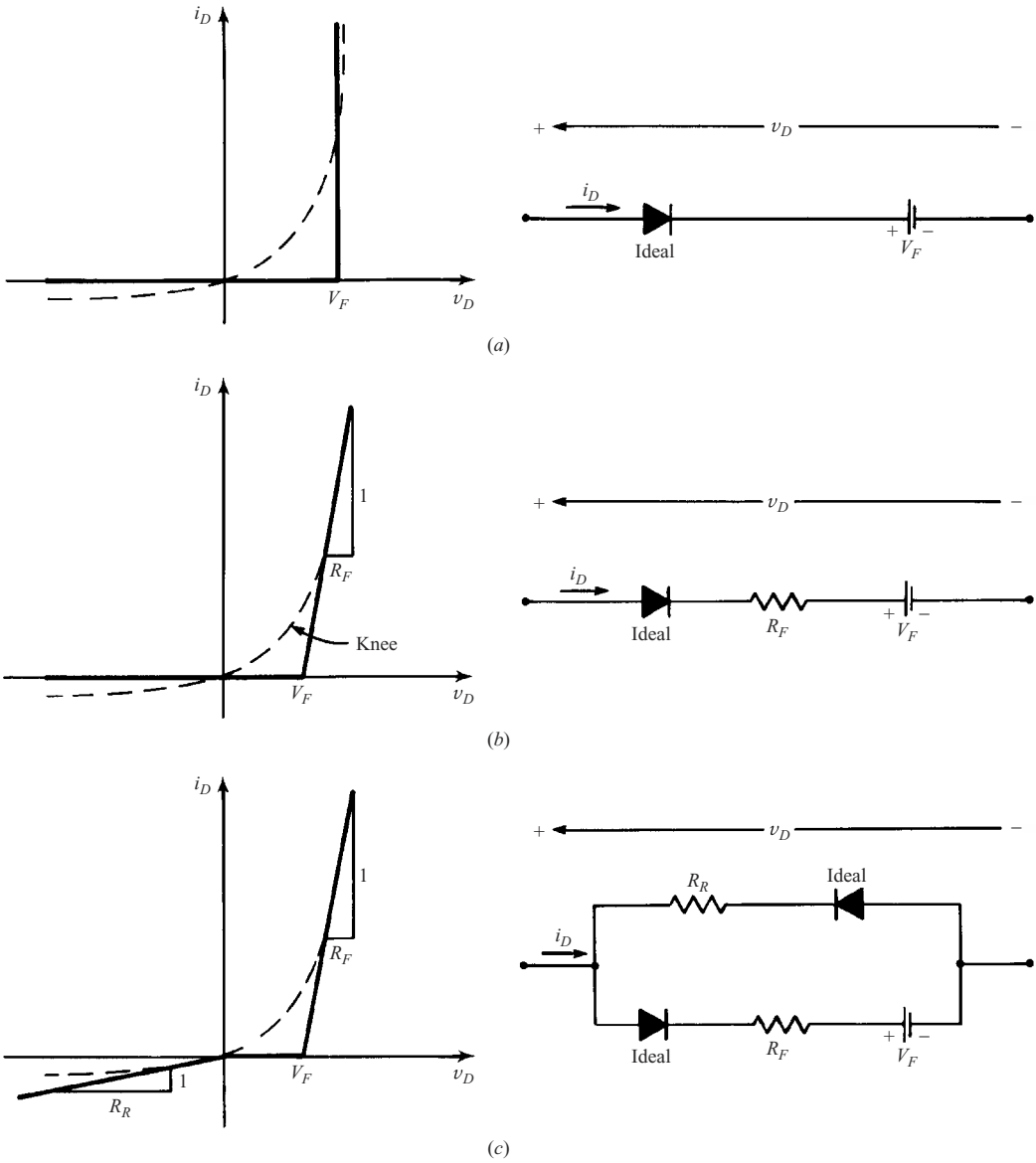


Fig. 2-11

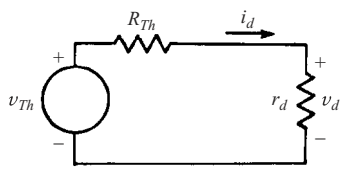


Fig. 2-12

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Example 2.9. For the circuit of Fig. 2-10, determine i_D if $\omega = 10^8$ rad/s and the diffusion capacitance is known to be 5000 pF.

From Example 2.8, $r_d = 2.5\,\Omega$. The diffusion capacitance C_d acts in parallel with r_d to give the following equivalent impedance for the diode, as seen by the ac signal:

$$Z_d = r_d \| jx_d = r_d \| \left(-j\,\frac{1}{\omega C_d}\right) = \frac{r_d}{1 + j\omega C_d r_d} = \frac{2.5}{1 + j(10^8)(5000 \times 10^{-12})(2.5)}$$
$$= 1.56\underline{|-51.34^\circ} = 0.974 - j1.218$$

In the frequency domain, the small-signal circuit (Fig. 2-12) yields

$$\bar{I}_d = \frac{\bar{V}_{Th}}{R_{Th} + Z_d} = \frac{0.1\underline{|-90^\circ}}{10 + 0.974 - j1.218} = \frac{0.1\underline{|-90^\circ}}{11.041\underline{|-6.33^\circ}} = 0.0091\underline{|-83.67^\circ} \quad \text{A}$$

In the time domain, with I_{DQ} as found in Example 2.7, we have

$$i_D = I_{DQ} + i_d = 36 + 9.1\cos(10^8 t - 83.67^\circ) \quad \text{mA}$$

2.7. RECTIFIER APPLICATIONS

Rectifier circuits are two-port networks that capitalize on the nearly one-way conduction of the diode: An ac voltage is impressed upon the input port, and a dc voltage appears at the output port.

The simplest rectifier circuit (Fig. 2-13) contains a single diode. It is commonly called a *half-wave rectifier* because the diode conducts over either the positive or the negative halves of the input-voltage waveform.

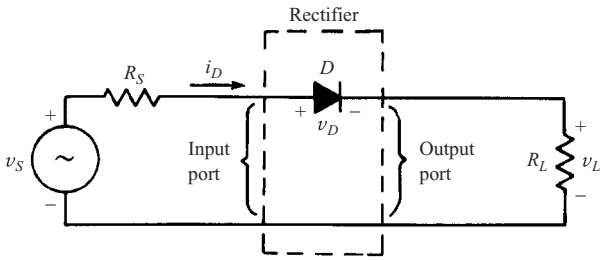


Fig. 2-13

Example 2.10. In Fig. 2-13, $v_S = V_m \sin \omega t$ and the diode is ideal. Calculate the average value of v_L.

Only one cycle of v_S need be considered. For the positive half-cycle, $i_D > 0$ and, by voltage division,

$$v_L = \frac{R_L}{R_L + R_S}(V_m \sin \omega t) \equiv V_{Lm} \sin \omega t$$

For the negative half-cycle, the diode is reverse-biased, $i_D = 0$, and $v_L = 0$. Hence,

$$V_{L0} = \frac{1}{2\pi}\int_0^{2\pi} v_L(\omega t)\, d(\omega t) = \frac{1}{2\pi}\int_0^{\pi} V_{Lm} \sin \omega t\, d(\omega t) = \frac{V_{Lm}}{\pi}$$

Although the half-wave rectifier gives a dc output, current flows through R_L only half the time, and the average value of the output voltage is only $1/\pi = 0.318$ times the peak value of the sinusoidal input voltage. The output voltage can be improved by use of a *full-wave rectifier* (see Problems 2.28 and 2.50).

When rectifiers are used as dc power supplies, it is desirable that the average value of the output voltage remain nearly constant as the load varies. The degree of constancy is measured as the *voltage regulation*,

$$\text{Reg} \equiv \frac{(\text{no-load } V_{L0}) - (\text{full-load } V_{L0})}{\text{full-load } V_{L0}} \tag{2.6}$$

which is usually expressed as a percentage. Note that 0 percent regulation implies a constant output voltage.

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Example 2.11. Find the voltage regulation of the half-wave rectifier of Fig. 2-13.

From Example 2.10, we know that

$$\text{Full-load } V_{L0} = \frac{V_{Lm}}{\pi} = \frac{R_L}{\pi(R_L + R_s)} V_m \tag{2.7}$$

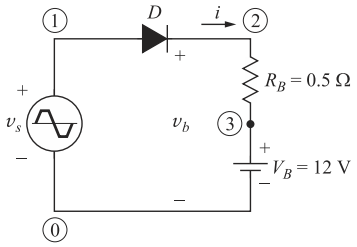
Realizing that $R_L \to \infty$ for no load, we may write

$$\text{No-load } V_{L0} = \lim_{R_L \to \infty} \left| \frac{R_L}{\pi(R_L + R_S)} V_m \right| = \frac{V_m}{\pi}$$

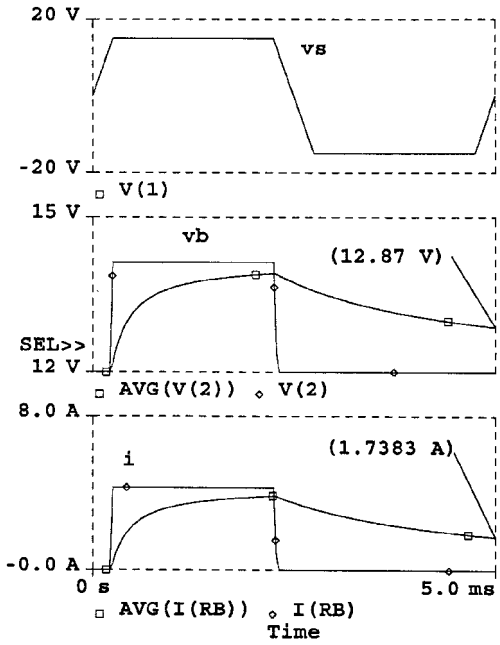
Thus, the voltage regulation is

$$\text{Reg} = \frac{\dfrac{V_m}{\pi} - \dfrac{R_L}{\pi(R_L + R_S)} V_m}{\dfrac{R_L}{\pi(R_L + R_S)} V_m} = \frac{R_S}{R_L} = \frac{100 R_S}{R_L}\,\%$$

Example 2.12. The half-wave rectifier circuit of Fig. 2-14(*a*) forms a battery charger where the battery terminal voltage (v_b) appears across the battery ideal voltage (V_B) and the battery internal resistance (R_B). The source is a 15-V, 200-Hz trapezoidal waveform with equal rise and fall times of 0.5 ms. Use SPICE methods to determine the average value of the voltage appearing at the battery terminals (V_{b0}) and the average value of current (I_0) supplied to the battery.



(*a*)



(*b*)

Fig. 2-14

The netlist code that follows describes the circuit.

```
Ex2_12.CIR - Half-wave rectifier
vs 1 0 PULSE ( -15V 15V -0.25ms 0.5ms 0.5ms 2ms 5ms )
D  1 2 DMOD
RB 2 3 0.5ohm
VB 3 0 12V
.MODEL DMOD D() ; Default diode
.TRAN 1us 5ms
.PROBE
.END
```

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After execution of < Ex2_12.CIR >, the Probe feature of PSpice is used to plot the instantaneous values of v_s, v_b, and i on the common time-axis of Fig. 2-14(b) for reference. The Running Average feature of PSpice (gives the correct full-period average value at the end of each waveform period) is invoked to find $V_{b0} = 12.87\,\text{V}$ and $I_0 = 1.7383\,\text{A}$, as marked on Fig. 2-14(b).

2.8. WAVEFORM FILTERING

The output of a rectifier alone does not usually suffice as a power supply, due to its variation in time. The situation is improved by placing a *filter* between the rectifier and the load. The filter acts to suppress the harmonics from the rectified waveform and to preserve the dc component. A measure of goodness for rectified waveforms, both filtered and unfiltered, is the *ripple factor*,

$$F_r \equiv \frac{\text{maximum variation in output voltage}}{\text{average value of output voltage}} = \frac{\Delta v_L}{V_{L0}} \tag{2.8}$$

A small value, say $F_r \leq 0.05$, is usually attainable and practical.

Example 2.13. Calculate the ripple factor for the half-wave rectifier of Example 2.10 (a) without a filter and (b) with a shunt capacitor filter as in Fig. 2-15(a).

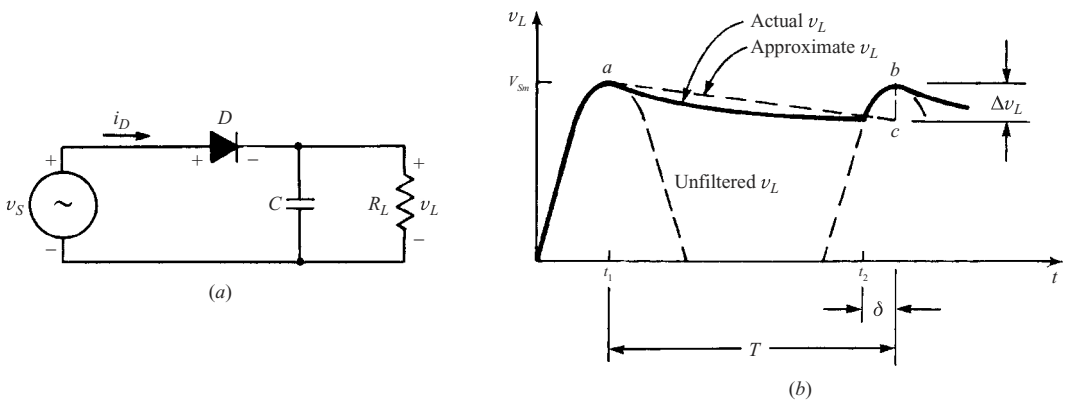


Fig. 2-15

(a) For the circuit of Example 2.10,

$$F_r = \frac{\Delta v_L}{V_{L0}} = \frac{V_{Lm}}{V_{Lm}/\pi} = \pi \approx 3.14$$

(b) The capacitor in Fig. 2-15(a) stores energy while the diode allows current to flow, and delivers energy to the load when current flow is blocked. The actual load voltage v_L that results with the filter inserted is sketched in Fig. 2-15(b), for which we assume that $v_S = V_{Sm} \sin \omega t$ and D is an ideal diode. For $0 < t \leq t_1$, D is forward-biased and capacitor C charges to the value V_{Sm}. For $t_1 < t \leq t_2$, v_S is less than v_L, reverse-biasing D and causing it to act as an open circuit. During this interval the capacitor is discharging through the load R_L, giving

$$v_L = V_{Sm}\, e^{-(t-t_1)/R_L C} \qquad (t_1 < t \leq t_2) \tag{2.9}$$

Over the interval $t_2 < t \leq t_2 + \delta$, v_S forward-biases diode D and again charges the capacitor to V_{Sm}. Then v_S falls below the value of v_L and another discharge cycle identical to the first occurs.

Obviously, if the time constant $R_L C$ is large enough compared to T to result in a decay like that indicated in Fig. 2-15(b), a major reduction in Δv_L and a major increase in V_{L0} will have been achieved, relative to the unfiltered rectifier. The introduction of two quite reasonable approximations leads to simple formulas for Δv_L and V_{L0}, and hence for F_r, that are sufficiently accurate for design and analysis work:

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1. If Δv_L is to be small, then $\delta \to 0$ in Fig. 2-15(b) and $t_2 - t_1 \approx T$.
2. If Δv_L is small enough, then (*2.9*) can be represented over the interval $t_1 < t \le t_2$ by a straight line with a slope of magnitude $V_{Sm}/R_L C$.

The dashed line labeled "Approximate v_L" in Fig. 2-15(b) implements these two approximations. From right triangle abc,

$$\frac{\Delta v_L}{T} = \frac{V_{Sm}}{R_L C} \qquad \text{or} \qquad \Delta v_L = \frac{V_{Sm}}{f R_L C}$$

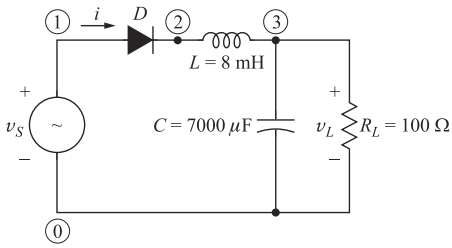
where f is the frequency of v_S. Since, under this approximation,

$$V_{L0} = V_{Sm} - \tfrac{1}{2}\Delta v_L$$

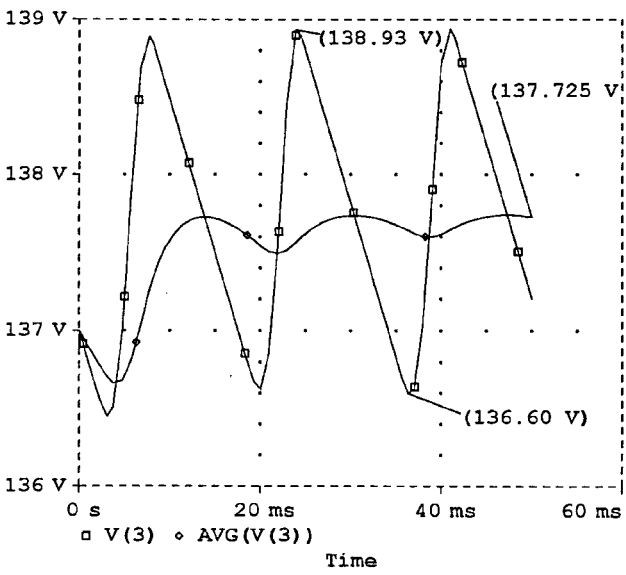
and $R_L C/T = f R_L C$ is presumed large,

$$F_r = \frac{\Delta v_L}{V_{L0}} = \frac{2}{2 f R_L C - 1} \approx \frac{1}{f R_L C} \tag{2.10}$$

Example 2.14. The half-wave rectifier of Fig. 2-16(a) is similar to that of Fig. 2-15 except an inductor that acts to reduce harmonics has been added. If source v_s is a 120-V (rms) sinusoidal source, use SPICE methods to determine the ripple factor F_r.



(a)



(b)

Fig. 2-16

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A set of netlist code for analysis of the circuit is shown below where an initial condition voltage (IC = 137 V) has been placed on the capacitor to eliminate transient conditions.

```
Ex2_14.CIR - HW rectifier with L-C filter
vs 1 0 SIN ( 0V {sqrt(2) *120V} 60Hz)
D  1 2 DMOD
L  2 3 8mH
C  3 0 700uF IC=137V ; Set initial condition
RL 3 0 100ohm
.MODEL DMOD D() ; Default diode
.TRAN 1us 50ms UIC
.PROBE
.END
```

Execution of < Ex2_14.CIR > and use of the Probe feature of PSpice leads to the plot of output voltage $v_L = \text{V}(3)$, shown by Fig. 2-16(*b*). The maximum and minimum values have been marked. Hence, the ripple voltage is

$$\Delta v_L = 138.93 - 136.60 = 2.33\,\text{V}$$

The running average of Fig. 2-16(*b*) has the full-period average value of v_L marked at the end of three source cycles giving $V_{L0} = 137.725\,\text{V}$. By (*2.8*),

$$F_r = \frac{\Delta v_L}{V_{L0}} = \frac{2.33}{137.725} = 0.017$$

2.9. CLIPPING AND CLAMPING OPERATIONS

Diode *clipping circuits* separate an input signal at a particular dc level and pass to the output, without distortion, the desired upper or lower portion of the original waveform. They are used to eliminate amplitude noise or to fabricate new waveforms from an existing signal.

Example 2.15. Figure 2-17(*a*) shows a *positive* clipping circuit, which removes any portion of the input signal v_i that is greater than V_b and passes as the output signal v_o any portion of v_i that is less than V_b. As you can see, v_D is negative when $v_i < V_b$, causing the ideal diode to act as an open circuit. With no path for current to flow through R, the value of v_i appears at the output terminals as v_o. However, when $v_i \geq V_b$, the diode conducts, acting as a short circuit and forcing $v_o = V_b$. Figure 2-17(*b*), the *transfer graph* or *transfer characteristic* for the circuit, shows the relationship between the input voltage, here taken as $v_i = 2V_b \sin \omega t$, and the output voltage.

Clamping is a process of setting the positive or negative peaks of an input ac waveform to a specific dc level, regardless of any variation in those peaks.

Example 2.16. An ideal clamping circuit is shown in Fig. 2-18(*b*), and a triangular ac input waveform in Fig. 2-18(*a*). If the capacitor C is initially uncharged and $V_b = 0$, the ideal diode D is forward-biased for $0 < t \leq T/4$, and it acts as a short circuit while the capacitor charges to $v_C = V_p$. At $t = T/4$, D open-circuits, breaking the only possible discharge path for the capacitor. Thus, the value $v_C = V_p$ is preserved; since v_i can never exceed V_p, D remains reverse-biased for all $t > T/4$, giving $v_o = v_D = v_i - V_p$. The function v_o is sketched in Fig. 2-18(*c*); all positive peaks are clamped at zero, and the average value is shifted from 0 to $-V_p$.

Example 2.17. For the clamping circuit of Fig. 2-18(*b*), let $v_i = 10\sin(2000\pi t)\,\text{V}$, $V_B = 5\,\text{V}$, and $C = 10\,\mu\text{F}$. Assume an ideal diode and use SPICE methods to determine output voltage v_o.

The netlist code describing the circuit is shown below. Since the capacitor will charge so that $v_C = V_B = 5\,\text{V}$, this value is set as an initial condition (IC = 5 V) to circumvent the transient response.

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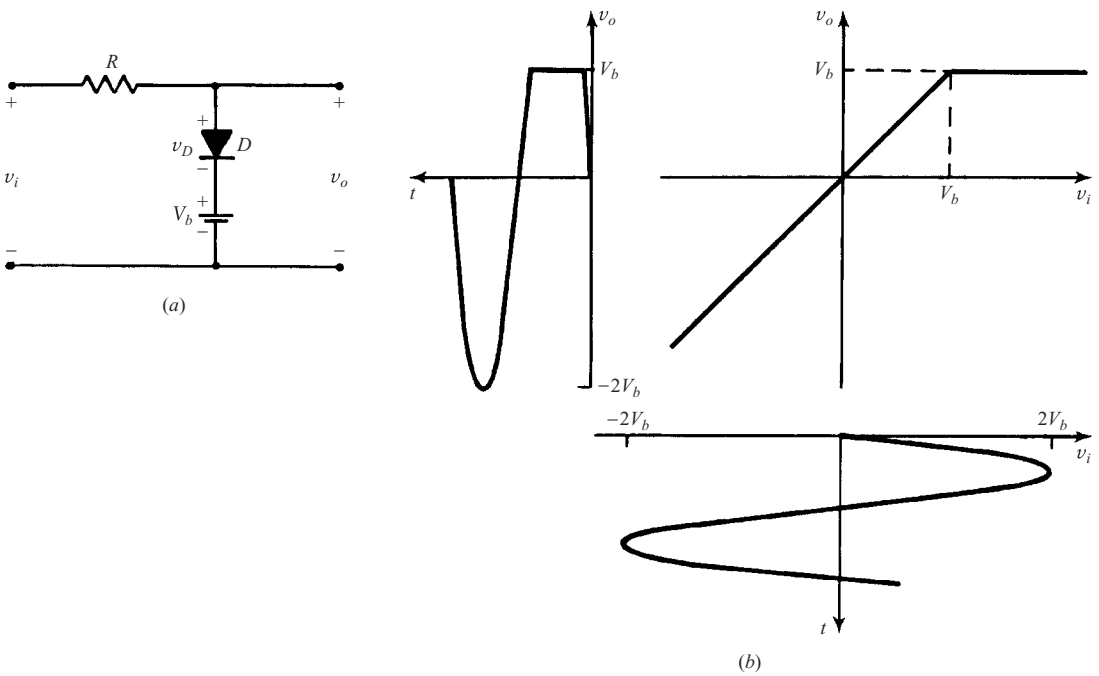


Fig. 2-17

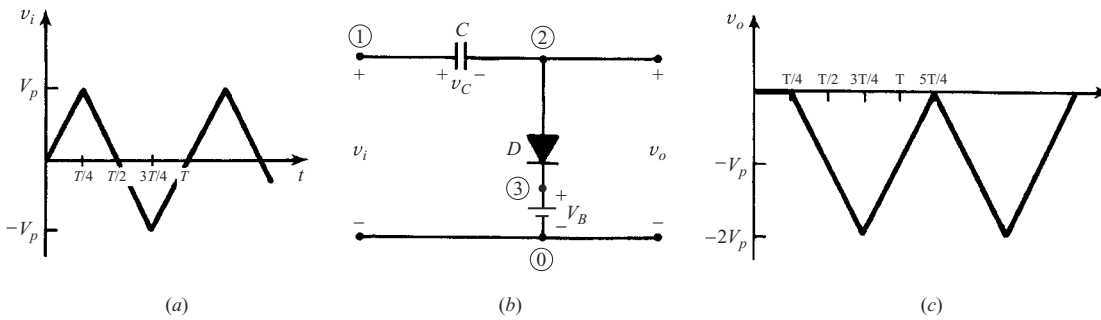
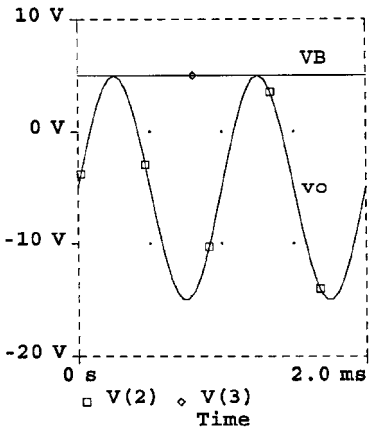


Fig. 2-18

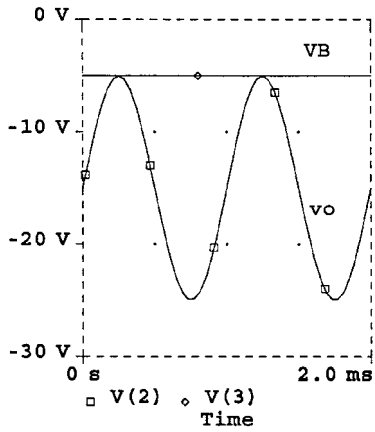
```
Ex2_17.CIR - Clamping circuit
vi 1 0 SIN ( 0V 10V 1kHz )
C  1 2 10uF IC=5V ; Set initial condition
D  2 3 DMOD
VB 3 0 5V
.MODEL DMOD D(n=0.0001) ; Ideal diode
.TRAN 1us 2ms UIC
.PROBE
.END
```

Execute < Ex2_17.CIR > and use the Probe feature of PSpice to plot the resulting output voltage $v_o = \text{V}(2)$ as shown by Fig. 2-19(*a*) where it is seen that the output voltage is simply v_i clamped so that the maximum value is equal to $V_B = 5\,\text{V}$.

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(*a*)



(*b*)

Fig. 2-19

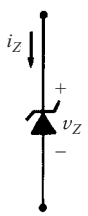
Example 2.18. The positive clamping circuit of Fig. 2-18(*b*) can be changed to a negative clamping circuit by inverting battery V_B. Make this change ($V_B = -5$ V) and use SPICE methods to determine the output voltage v_o for the circuit if v_i and C have the values of Example 2.17.

The netlist code of Example 2.17 can be modified to describe the reversal of V_B by simply assigning a value of -5 V (VB 3 0 $-$5V) or by reversing the order of the node listing (VB 0 3 5V). Since the capacitor will charge so that $v_C = 15$ V, set IC = 15 V to yield an immediate steady-state solution.

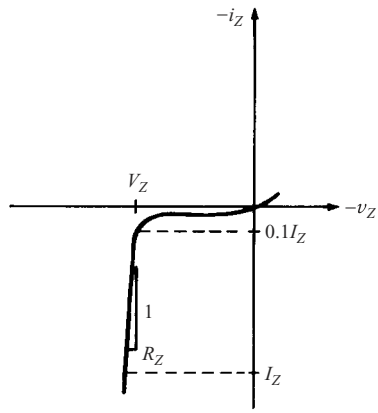
Execution of the modified netlist code (available at the author website as < Ex2_18.CIR >) and use of the Probe feature of PSpice leads to the plot of Fig. 2-19(*b*) where it is seen that the output voltage v_o = V(2) is v_i clamped to the maximum value of $V_B = -5$ V.

2.10. THE ZENER DIODE

The *Zener diode* or *reference diode*, whose symbol is shown in Fig. 2-20(*a*), finds primary usage as a voltage regulator or reference. The forward conduction characteristic of a Zener diode is much the same as that of a rectifier diode; however, it usually operates with a reverse bias, for which its characteristic is radically different. Note, in Fig. 2-20(*b*), that:



(*a*)



(*b*)

Fig. 2-20

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1. The reverse voltage breakdown is rather sharp. The breakdown voltage can be controlled through the manufacturing process so it has a reasonably predictable value.
2. When a Zener diode is in reverse breakdown, its voltage remains extremely close to the breakdown value while the current varies from rated current (I_Z) to 10 percent or less of rated current.

A Zener regulator should be designed so that $i_Z \geq 0.1I_Z$ to ensure the constancy of v_Z.

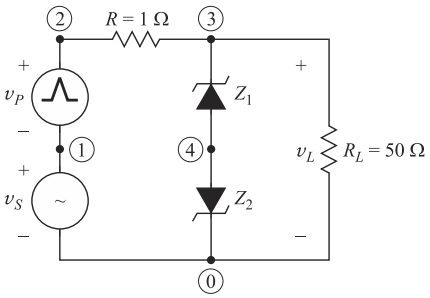
Example 2.19. Find the voltage v_Z across the Zener diode of Fig. 2-20(a) if $i_Z = 10\,\text{mA}$ and it is known that $V_Z = 5.6\,\text{V}$, $I_Z = 25\,\text{mA}$, and $R_Z = 10\,\Omega$.

Since $0.1I_Z \leq i_Z \leq I_Z$, operation is along the safe and predictable region of Zener operation. Consequently,

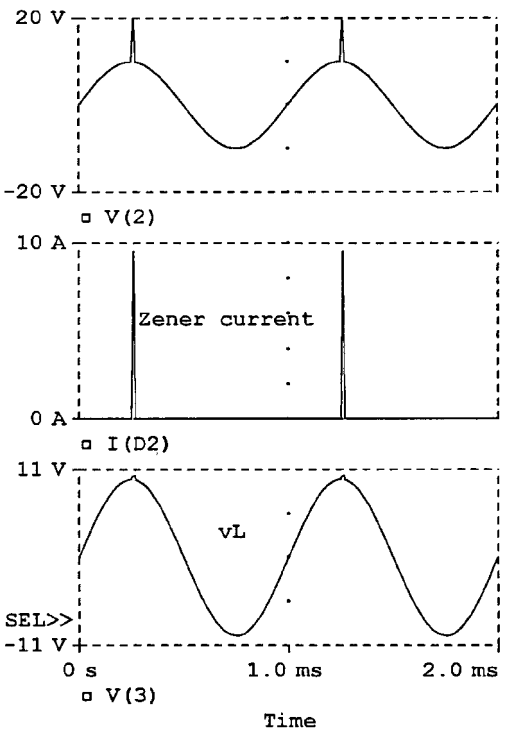
$$v_Z \approx V_Z + i_Z R_Z = 5.6 + (10 \times 10^{-3})(10) = 5.7\,\text{V}$$

R_Z is frequently neglected in the design of Zener regulators. Problem 2.31 illustrates the design technique.

Example 2.20. Back-to-back Zener diodes, as shown between 3,0 of Fig. 2-21(a), are frequently used to clip or remove voltage spikes. SPICE-based analysis programs generally do not offer a specific model for the Zener diode, but rather the model is implemented by model parameter specification of the reverse breakdown voltage (BV) and the associated reverse breakdown current (IBV). For the circuit of Fig. 2-21(a), let $v_s = 10\sin(2000\pi t)\,\text{V}$ and source v_p model a disturbance that results in a 10 V spike appearing at the positive crest of v_s. Set values for the reverse breakdown voltage of the Zener diodes and assess the effectiveness of the circuit in clipping the disturbance spike.



(a)



(b)

Fig. 2-21

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The netlist code describing the circuit follows:

```
Ex2_20.CIR - Zener diode spike clipper
.PARAM f=1kHz T={1/f}
vs 1 0 SIN ( 0V 10V {f} )
* Set 10V spike at positive peak of vs
vp 2 1 PULSE ( 0V 10V {T/4} {T/100} {T/100} 1us {T} )
R  2 3 1ohm
D1 4 3 DMOD ; Zener diode Z1
D2 4 0 DMOD ; Zener diode Z2
RL 3 0 50ohm
.MODEL DMOD D( BV=9.3V IBV=1A )
.TRAN 1 us 2ms
.PROBE
.END
```

The final values of BV and IBV shown in the code were determined by trial and error to give acceptable results, knowing that severe avalanche is approximately 1 V beyond the value of BV. Parameter IBV strongly influences the slope of the diode characteristic in the avalanche region.

The plot of Fig. 2-21(*b*) shows both the voltage $(v_s + v_p)$ impressed on the circuit and the resulting Zener current as the spike is clipped. Examination of the output voltage v_L shows that the spike is clipped so that only a 0.42 V remnant of the original 10 V spike appears across the load resistor R_L.

Solved Problems

2.1 At a junction temperature of 25°C, over what range of forward voltage drop v_D can (*2.1*) be approximated as $i_D \approx I_o e^{v_D/V_T}$ with less than 1 percent error for a Ge diode?

From (*2.1*) with $\eta = 1$, the error will be less than 1 percent if $e^{v_D/V_T} > 101$. In that range,

$$v_D > V_T \ln 101 = \frac{kT}{q} \ln 101 = \frac{(1.38 \times 10^{-23})(25 + 273)}{1.6 \times 10^{-19}} 4.6151 = 0.1186\,\text{V}$$

2.2 A Ge diode described by (*2.1*) is operated at a junction temperature of 27°C. For a forward current of 10 mA, v_D is found to be 0.3 V. (*a*) If $v_D = 0.4$ V, find the forward current. (*b*) Find the reverse saturation current.

(*a*) We form the ratio

$$\frac{i_{D2}}{i_{D1}} = \frac{I_o(e^{v_{D2}/V_T} - 1)}{I_o(e^{v_{D1}/V_T} - 1)} = \frac{e^{0.4/0.02587} - 1}{e^{0.3/0.02587} - 1} = 47.73$$

Then $i_{D2} = (47.73)(10\,\text{mA}) = 477.3\,\text{mA}$

(*b*) By (*2.1*),

$$I_o = \frac{i_{D1}}{e^{v_{D1}/V_T} - 1} = \frac{10 \times 10^{-3}}{e^{0.3/0.02587} - 1} = 91\,\text{nA}$$

2.3 For the circuit of Fig. 2-22(*a*), sketch the waveforms of v_L and v_D if the source voltage v_S is as given in Fig. 2-22(*b*). The diode is ideal, and $R_L = 100\,\Omega$.

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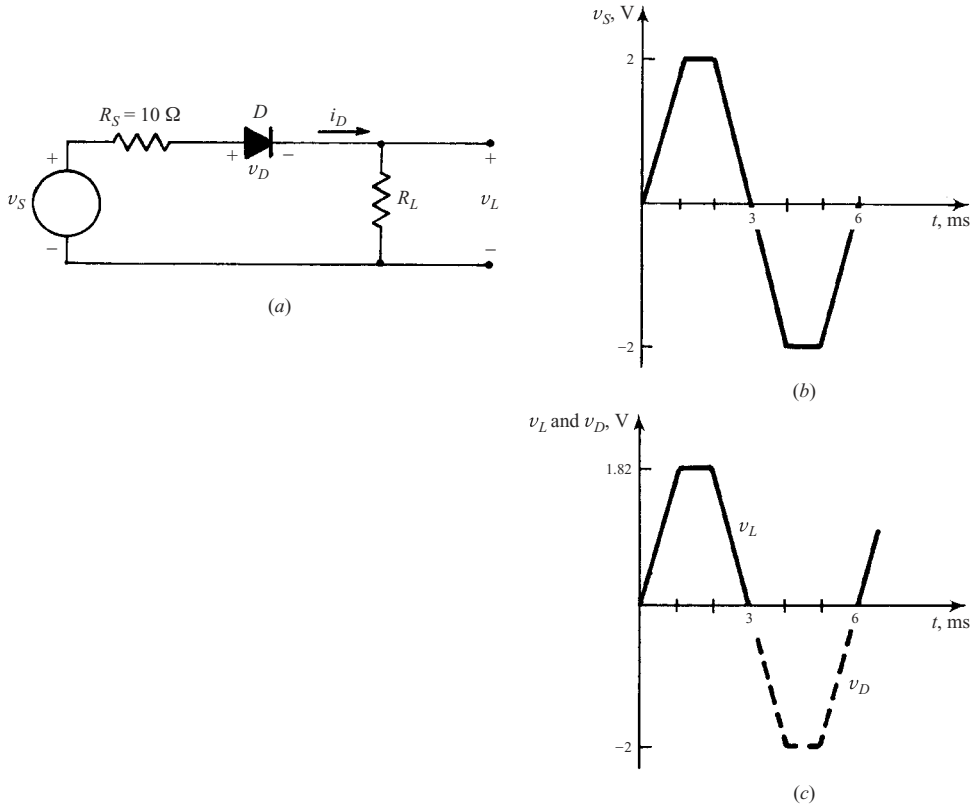


Fig. 2-22

If $v_S \geq 0$, D conducts, so that $v_D = 0$ and

$$v_L = \frac{R_L}{R_L + R_S} v_S = \frac{100}{100 + 10} v_S = 0.909 v_S$$

If $v_S < 0$, D blocks, so that $v_D = v_S$ and $v_L = 0$. Sketches of v_D and v_L are shown in Fig. 2-22(*c*).

2.4 Extend the ideal diode analysis procedure of Section 2.2 to the case of multiple diodes by solving for the current i_L in the circuit of Fig. 2-23(*a*). Assume D_1 and D_2 are ideal. $R_2 = R_L = 100\,\Omega$, and v_S is a 10-V square wave of period 1 ms.

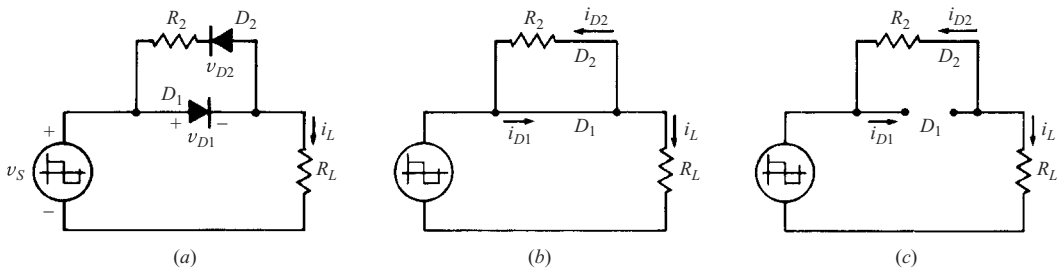


Fig. 2-23

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Step 1: Assume both diodes are forward-biased, and replace each with a short circuit as shown in Fig. 2-23(*b*).

Step 2: Since D_1 is "on," or in the zero-impedance state, current division requires that

$$i_{D2} = -\frac{0}{R_2 + 0} i_L = 0 \tag{1}$$

Hence, by Ohm's law,

$$i_L = i_{D1} = \frac{v_S}{R_L} \tag{2}$$

Step 3: Observe that when $v_S = 10 > 0$, we have, by (*2*), $i_{D1} = 10/100 = 0.1\,\text{A} > 0$. Also, by (*1*), $i_{D2} = 0$. Thus all diode currents are greater than or equal to zero, and the analysis is valid. *However*, when $v_S = -10 < 0$, we have, by (*2*), $i_{D1} = -10/100 = -0.1\,\text{A} < 0$, and the analysis is no longer valid.

Step 4: Replace D_1 with an open circuit as illustrated in Fig. 2-23(*c*). Now obviously $i_{D1} = 0$ and, by Ohm's law,

$$i_L = -i_{D2} = \frac{v_S}{R_2 + R_L} = \frac{-10}{100 + 100} = -0.05\,\text{A}$$

Further, voltage division requires that

$$v_{D1} = \frac{R_2}{R_2 + R_L} v_S$$

so that $v_{D1} < 0$ if $v_S < 0$, verifying that D_1 is actually reverse-biased. Note that if D_2 had been replaced with an open circuit, we would have found that $v_{D2} = -v_S = 10\,\text{V} > 0$, so D_2 would not actually have been reverse-biased.

2.5 In the circuit of Fig. 2-24, D_1 and D_2 are ideal diodes. Find i_{D1} and i_{D2}.

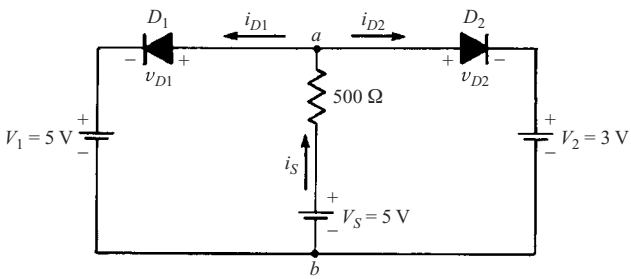


Fig. 2-24

Because of the polarities of D_1 and D_2, it is necessary that $i_S \geq 0$. Thus, $v_{ab} \leq V_S = V_1$. But $v_{D1} = v_{ab} - V_1$; therefore, $v_D \leq 0$ and so $i_{D1} \equiv 0$, regardless of conditions in the right-hand loop. It follows that $i_{D2} = i_S$. Now using the analysis procedure of Section 2.2, we assume D_2 is forward-biased and replace it with a short circuit. By KVL,

$$i_{D2} = \frac{V_S - V_2}{500} = \frac{5 - 3}{500} = 4\,\text{mA}$$

Since $i_{D2} \geq 0$, D_2 is in fact forward-biased and the analysis is valid.

2.6 The logic OR gate can be utilized to fabricate composite waveforms. Sketch the output v_o of the gate of Fig. 2-25(*a*) if the three signals of Fig. 2-25(*b*) are impressed on the input terminals. Assume that diodes are ideal.

For this circuit, KVL gives

$$v_1 - v_2 = v_{D1} - v_{D2} \qquad v_1 - v_3 = v_{D1} - v_{D3}$$

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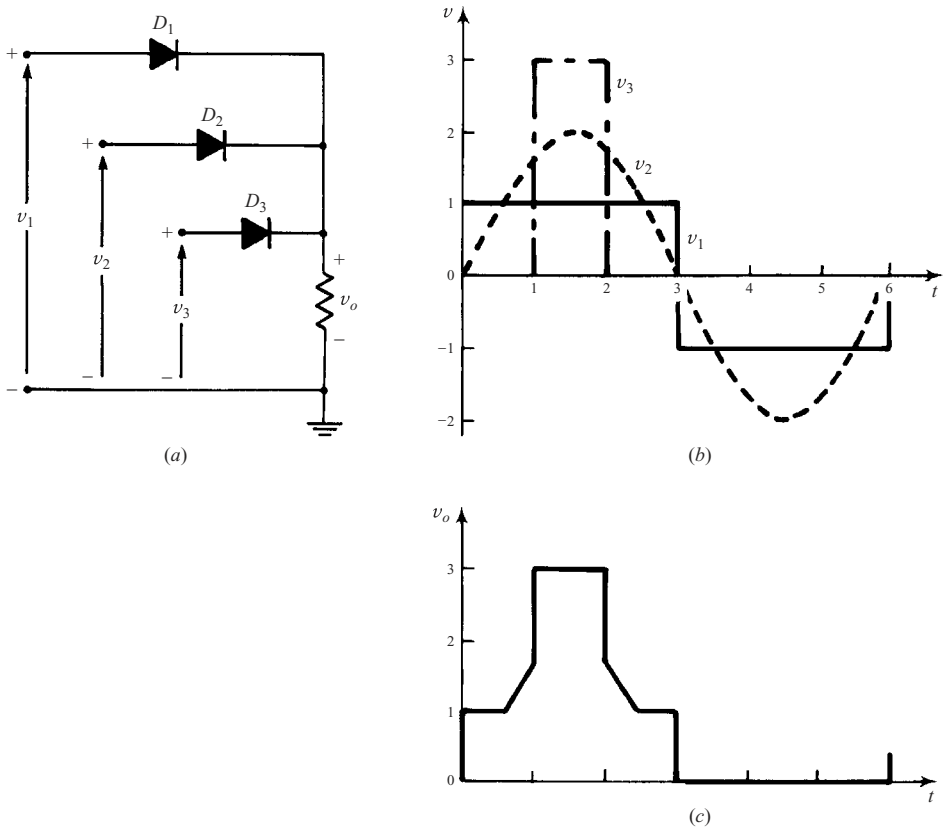


Fig. 2-25

i.e., the diode voltages have the same ordering as the input voltages. Suppose that v_1 is positive and exceeds v_2 and v_3. Then D_1 must be forward-biased, with $v_{D1} = 0$ and, consequently, $v_{D2} < 0$ and $v_{D3} < 0$. Hence, D_2 and D_3 block, while v_1 is passed as v_o. This is so in general: The logic of the OR gate is that the largest positive input signal is passed as v_o, while the remainder of the input signals are blocked. If all input signals are negative, $v_o = 0$. Application of this logic gives the sketch of v_o in Fig. 2-25(*c*).

2.7 The diode in the circuit of Fig. 2-26(*a*) has the nonlinear terminal characteristic of Fig. 2-26(*b*). Find i_D and v_D analytically, given $v_S = 0.1 \cos \omega t$ V and $V_b = 2$ V.

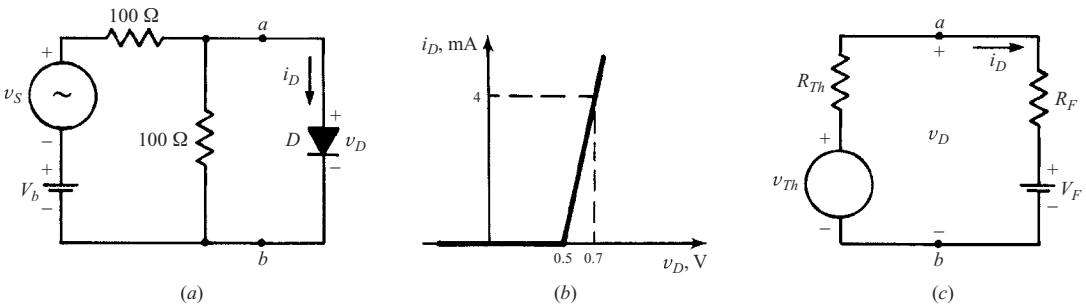


Fig. 2-26

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The Thévenin equivalent circuit for the network to the left of terminals a, b in Fig. 2-26(a) has

$$V_{Th} = \frac{100}{200}(2 + 0.1\cos\omega t) = 1 + 0.05\cos\omega t \quad \text{V}$$
$$R_{Th} = \frac{(100)^2}{200} = 50\,\Omega$$

The diode can be modeled as in Fig. 2-11(b), with $V_F = 0.5\,\text{V}$ and

$$R_F = \frac{0.7 - 0.5}{0.004} = 50\,\Omega$$

Together, the Thévenin equivalent circuit and the diode model form the circuit in Fig. 2-26(c). Now by Ohm's law,

$$i_D = \frac{V_{Th} - V_F}{R_{Th} + R_F} = \frac{(1 + 0.05\cos\omega t) - 0.5}{50 + 50} = 5 + 0.5\cos\omega t \quad \text{mA}$$
$$v_D = V_F + R_F i_D = 0.5 + 50(0.005 + 0.0005\cos\omega t) = 0.75 + 0.025\cos\omega t \quad \text{V}$$

2.8 Solve Problem 2.7 graphically for i_D.

The Thévenin equivalent circuit has already been determined in Problem 2.7. By (*2.4*), the dc load line is given by

$$i_D = \frac{V_{Th}}{R_{Th}} - \frac{v_D}{R_{Th}} = \frac{1}{50} - \frac{v_D}{50} = 20 - 20v_D \quad \text{mA} \tag{1}$$

In Fig. 2-27, (*1*) has been superimposed on the diode characteristic, replotted from Fig. 2-26(b). As in Example 2.7, equivalent time scales for v_{Th} and i_D are laid out adjacent to the characteristic curve. Since the diode characteristic is linear about the Q point over the range of operation, only dynamic load lines corresponding to the maximum and minimum of v_{Th} need be drawn. Once these two dynamic load lines are constructed parallel to the dc load line, i_D can be sketched.

2.9 Use the small-signal technique of Section 2.6 to find i_D and v_D in Problem 2.7.

The Thévenin equivalent circuit of Problem 2.7 is valid here. Moreover, the intersection of the dc load line and the diode characteristic in Fig. 2-27 gives $I_{DQ} = 5\,\text{mA}$ and $V_{DQ} = 0.75\,\text{V}$. The dynamic resistance is, then, by (*2.5*),

$$r_d = \frac{\Delta v_D}{\Delta i_D} = \frac{0.7 - 0.5}{0.004} = 50\,\Omega$$

We now have all the values needed for analysis using the small-signal circuit of Fig. 2-12. By Ohm's law,

$$i_d = \frac{v_{th}}{R_{Th} + r_d} = \frac{0.05\cos\omega t}{50 + 50} = 0.5\cos\omega t \quad \text{mA}$$
$$v_d = r_d i_d = 50(0.0005\cos\omega t) = 0.025\cos\omega t \quad \text{V}$$
$$i_D = I_{DQ} + i_d = 5 + 0.5\cos\omega t \quad \text{mA}$$
$$v_D = V_{DQ} + v_d = 0.75 + 0.025\cos\omega t \quad \text{V}$$

2.10 A voltage source, $v_S = 0.4 + 0.2\sin\omega t\,\text{V}$, is placed directly across a diode characterized by Fig. 2-26(b). The source has no internal impedance and is of proper polarity to forward-bias the diode. (a) Sketch the resulting diode current i_D. (b) Determine the value of the quiescent current I_{DQ}.

(a) A scaled plot of v_S has been laid out adjacent to the v_D axis of the diode characteristic in Fig. 2-28. With zero resistance between the ideal voltage source and the diode, the dc load line has infinite slope and $v_D = v_S$. Thus, i_D is found by a point-by-point projection of v_S onto the diode characteristic,

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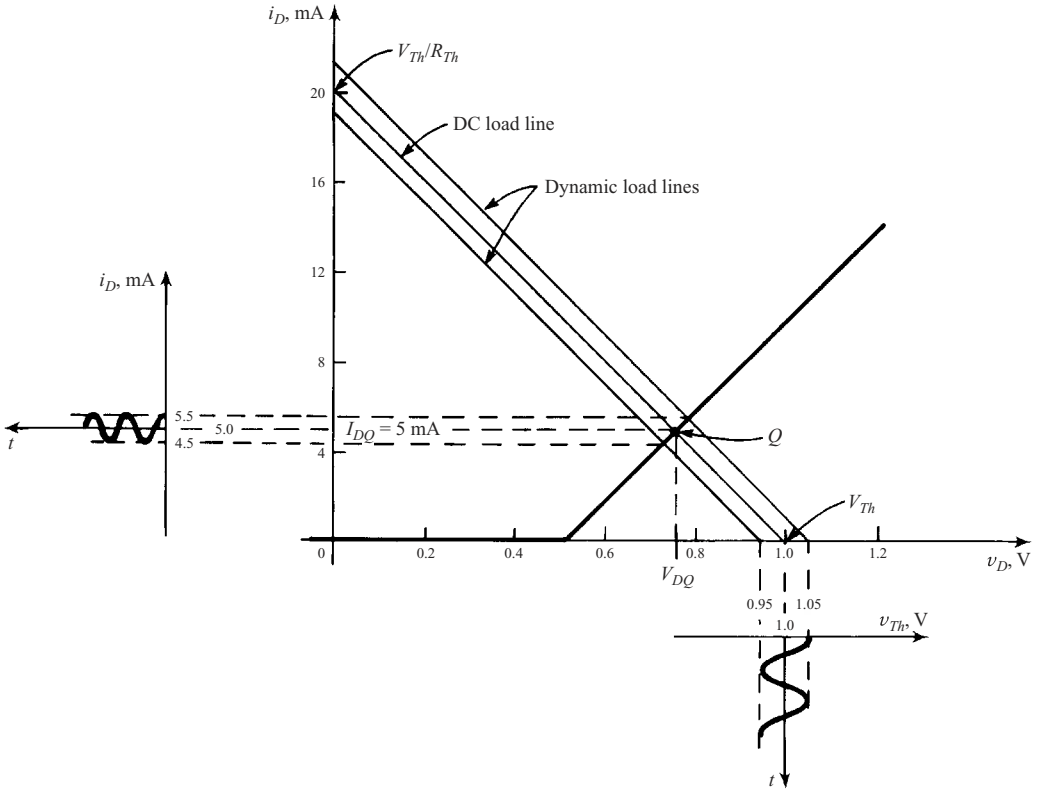


Fig. 2-27

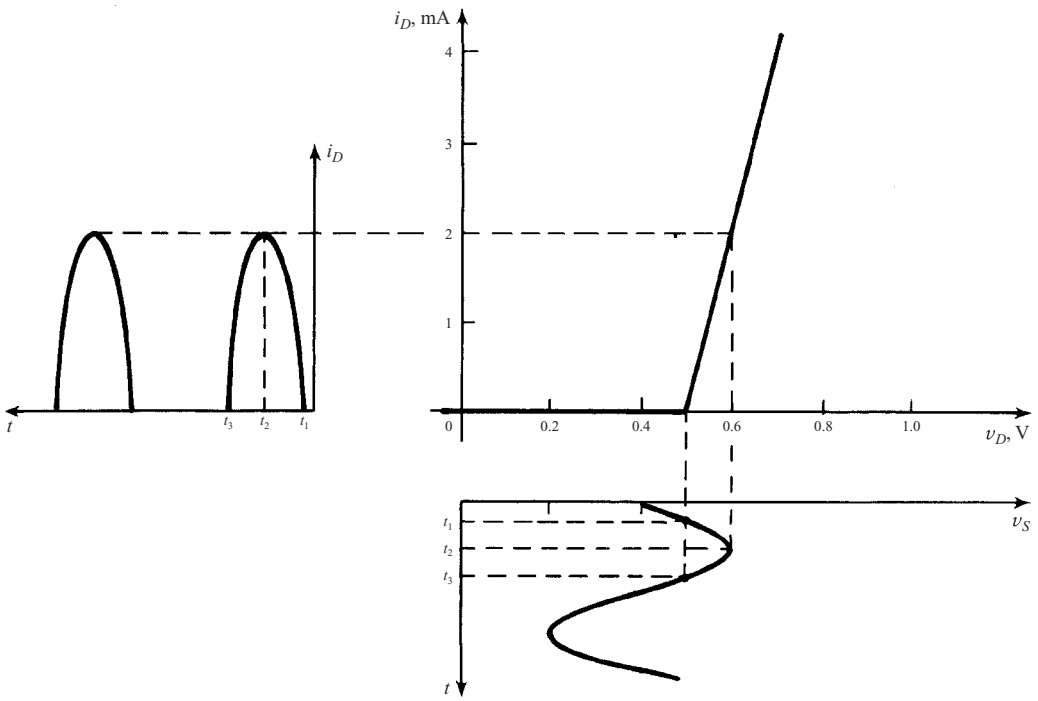


Fig. 2-28

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followed by reflection through the i_D axis. Notice that i_D is extremely distorted, bearing little resemblance to v_S.

(*b*) Quiescent conditions obtain when the ac signal is zero. In this case, when $v_S = 0.4\,\text{V}$, $i_D = I_{DQ} = 0$.

2.11 In the circuit of Fig. 2-3(*a*), assume $R_S = R_1 = 200\,\Omega$, $R_L = 50\,\text{k}\Omega$, and $v_S = 400 \sin \omega t\,\text{V}$. The diode is ideal, with reverse saturation current $I_o = 2\,\mu\text{A}$ and a peak inverse voltage (PIV) rating of $V_R = 100\,\text{V}$. (*a*) Will the diode fail in avalanche breakdown? (*b*) If the diode will fail, is there a value of R_L for which failure will not occur?

(*a*) From Example 2.1,

$$v_{Th} = \frac{R_1}{R_1 + R_S} v_S = \frac{200}{200 + 200} (400 \sin \omega t) = 200 \sin \omega t \quad \text{V}$$

$$R_{Th} = \frac{R_1 R_S}{R_1 + R_S} = \frac{(200)(200)}{200 + 200} = 100\,\Omega$$

The circuit to be analyzed is that of Fig. 2-3(*c*); the instants of concern are when $\omega t = (2n + 1)\pi/2$ for $n = 1, 2, 3, \ldots$, at which times $v_{Th} = -200\,\text{V}$ and thus v_D is at its most negative value. An application of KVL yields

$$v_D = v_{Th} - i_D(R_{Th} + R_L) = -200 - (-2 \times 10^{-6})(100 + 50 \times 10^3) = -199.9\,\text{V} \qquad (1)$$

Since $v_D < -V_R = -100\,\text{V}$, avalanche failure occurs.

(*b*) From (*1*), it is apparent that $v_D \geq -100\,\text{V}$ if

$$R_L \geq \frac{v_{Th} - v_D}{i_D} - R_{Th} = \frac{-200 - (-100)}{-2 \times 10^{-6}} - 100 = 50\,\text{M}\Omega$$

2.12 In the circuit of Fig. 2-29, v_S is a 10-V square wave of period 4 ms, $R = 100\,\Omega$, and $C = 20\,\mu\text{F}$. Sketch v_C for the first two cycles of v_S if the capacitor is initially uncharged and the diode is ideal.

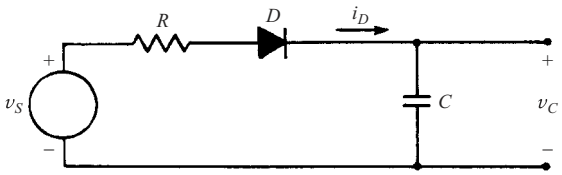


Fig. 2-29

In the interval $0 \leq t < 2\,\text{ms}$,

$$v_C(t) = v_S(1 - e^{-t/RC}) = 10(1 - e^{-500t}) \quad \text{V}$$

For $2 \leq t < 4\,\text{ms}$, D blocks and the capacitor voltage remains at

$$v_C(2\,\text{ms}) = 10(1 - e^{-500(0.002)}) = 6.32\,\text{V}$$

For $4 \leq t < 6\,\text{ms}$,

$$v_C(t) = v_S - (v_S - 6.32)e^{-(t-0.004)/RC} = 10 - (10 - 6.32)e^{-500(t-0.004)} \quad \text{V}$$

And for $6 \leq t < 8\,\text{ms}$, D again blocks and the capacitor voltage remains at

$$v_C(6\,\text{ms}) = 10 - (10 - 6.32)e^{-500(0.002)} = 8.654\,\text{V}$$

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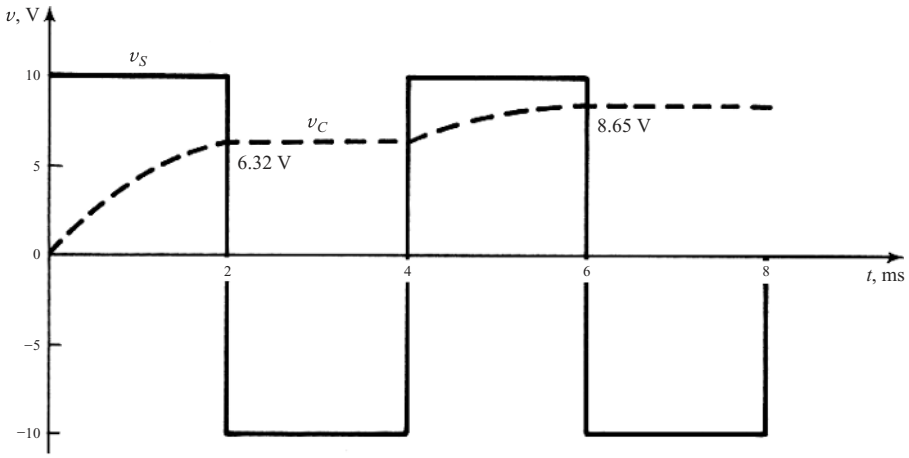
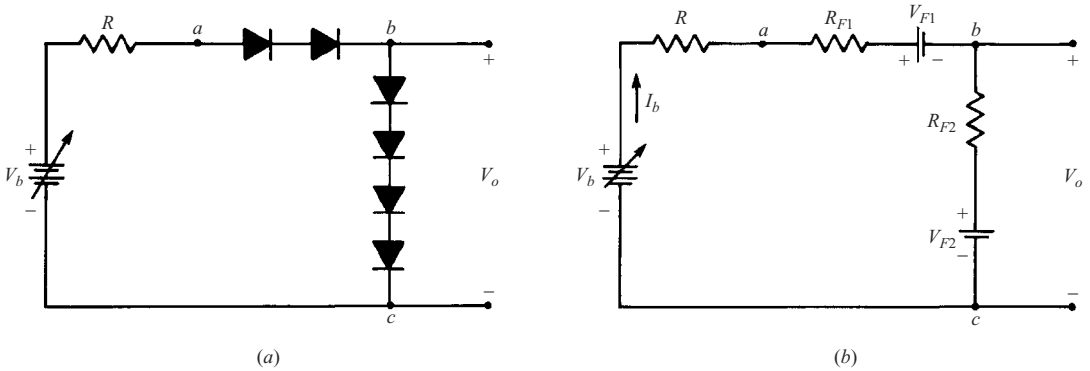


Fig. 2-30

The waveforms of v_S and v_C are sketched in Fig. 2-30.

2.13 The circuit of Fig. 2-31(*a*) is an "inexpensive" voltage regulator; all the diodes are identical and have the characteristic of Fig. 2-26(*b*). Find the regulation of v_o when V_b increases from its nominal value of 4 V to the value 6 V. Take $R = 2\,\text{k}\Omega$.



(*a*) (*b*)

Fig. 2-31

We determined in Problem 2.7 that each diode can be modeled as a battery, $V_F = 0.5\,\text{V}$, and a resistor, $R_F = 500\,\Omega$, in series. Combining the diode strings between points *a* and *b* and between points *b* and *c* gives the circuit of Fig. 2-31(*b*), where

$$V_{F1} = 2V_F = 1\,\text{V} \qquad V_{F2} = 4V_F = 2\,\text{V} \qquad R_{F1} = 2R_F = 100\,\Omega \qquad R_{F2} = 4R_F = 200\,\Omega$$

By KVL,
$$I_b = \frac{V_b - V_{F1} - V_{F2}}{R + R_{F1} + R_{F2}}$$

whence
$$V_o = V_{F2} + I_b R_{F2} = V_{F2} + \frac{(V_b - V_{F1} - V_{F2})R_{F2}}{R + R_{F1} + R_{F2}}$$

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For $V_{b1} = 4\,\text{V}$ and $V_{b2} = 6\,\text{V}$,

$$V_{o1} = 2 + \frac{(4-1-2)(200)}{2000+100+200} = 2.09\,\text{V} \qquad V_{o2} = 2 + \frac{(6-1-2)(200)}{2000+100+200} = 2.26\,\text{V}$$

and (*2.6*) gives

$$\text{Reg} = \frac{V_{o2} - V_{o1}}{V_{o1}}\,(100\%) = 8.1\%$$

2.14 The circuit of Fig. 2-22(*a*) is to be used as a dc power supply for a load R_L that varies from $10\,\Omega$ to $1\,\text{k}\Omega$; v_S is a 10-V square wave. Find the percentage change in the average value of v_L over the range of load variation, and comment on the quality of regulation exhibited by this circuit.

Let T denote the period of v_S. For $R_L = 10\,\Omega$,

$$v_L = \begin{cases} \dfrac{R_L}{R_L + R_S}\,v_S = \dfrac{10}{10+10}\,10 = 5\,\text{V} & 0 \le t < T/2 \\ 0 \text{ (diode blocks)} & T/2 \le t < T \end{cases}$$

and so $$V_{L0} = \frac{5(T/2) + 0(T/2)}{T} = 2.5\,\text{V}$$

For $R_L = 1\,\text{k}\Omega$,

$$v_L = \begin{cases} \dfrac{R_L}{R_L + R_S}\,v_S = \dfrac{1000}{1010}\,10 = 9.9\,\text{V} & 0 \le t < T/2 \\ 0 \text{ (diode blocks)} & T/2 \le t < T \end{cases}$$

and so $$V_{L0} = \frac{9.9(T/2) + 0}{T} = 4.95\,\text{V}$$

Then, by (*2.6*) and using $R_L = 10\,\Omega$ as full load, we have

$$\text{Reg} = \frac{4.95 - 2.5}{2.5}\,(100\%) = 98\%$$

This large value of regulation is prohibitive for most applications. Either another circuit or a filter network would be necessary to make this power supply useful.

2.15 The circuit of Fig. 2-32 adds a dc level (a bias voltage) to a signal whose average value is zero. If v_S is a 10-V square wave of period T, $R_L = R_1 = 10\,\Omega$, and the diode is ideal, find the average value of v_L.

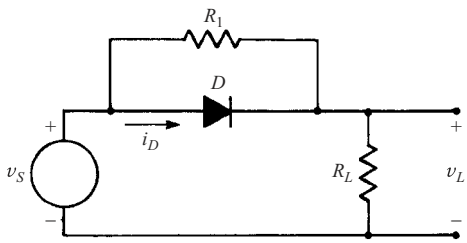


Fig. 2-32

For $v_L > 0$, D is forward-biased and $v_L = v_S = 10\,\text{V}$. For $v_L < 0$, D is reverse-biased and

$$v_L = \frac{R_L}{R_L + R_1}\,v_S = \frac{10}{10+10}\,(-10) = -5\,\text{V}$$

Thus, $$V_{L0} = \frac{10(T/2) + (-5)(T/2)}{T} = 2.5\,\text{V}$$

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For some symmetrical input signals, this type of circuit could destroy the symmetry of the input.

2.16 Size the filter capacitor in the rectifier circuit of Fig. 2-15(*a*) so that the ripple voltage is approximately 5 percent of the average value of the output voltage. The diode is ideal, $R_L = 1\,\text{k}\Omega$, and $v_S = 90 \sin 2000t\,\text{V}$. Calculate the average value of v_L for this filter.

With $F_r = 0.05$, (*2.10*) gives

$$C \approx \frac{1}{fR_L(0.05)} = \frac{1}{(2000/2\pi)(1 \times 10^3)(0.05)} = 62.83\,\mu\text{F}$$

Then, using the approximations that led to (*2.10*), we have

$$V_{L0} = V_{Sm} - \frac{1}{2}\Delta v_L = V_{Sm} - \frac{V_{Sm}}{2fR_LC} \approx V_{Sm}\left(1 - \frac{0.05}{2}\right) = (90)(0.975) = 87.75\,\text{V}$$

2.17 In the positive clipping circuit of Fig. 2-17(*a*), the diode is ideal and v_i is a 10-V triangular wave with period T. Sketch one cycle of the output voltage v_o if $V_b = 6\,\text{V}$.

The diode blocks (acts as an open circuit) for $v_i < 6\,\text{V}$, giving $v_o = v_i$. For $v_i \geq 6\,\text{V}$, the diode is in forward conduction, clipping v_i to effect $v_o = 6\,\text{V}$. The resulting output voltage waveform is sketched in Fig. 2-33.

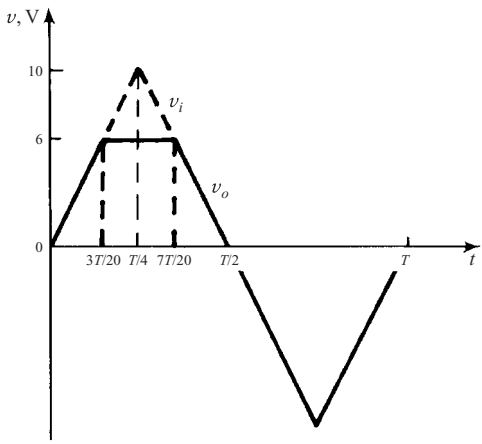


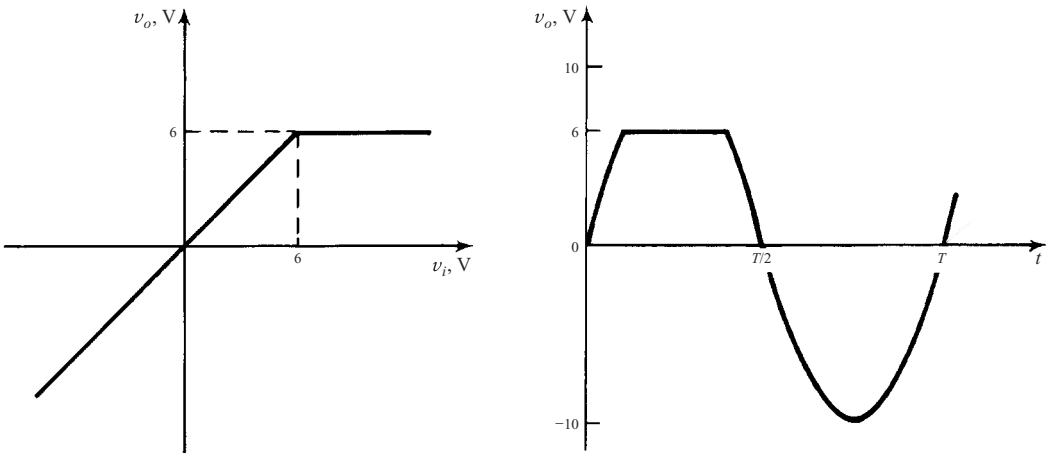
Fig. 2-33

2.18 Draw a transfer characteristic relating v_o to v_i for the positive clipping network of Problem 2.17. Also, sketch one cycle of the output waveform if $v_i = 10 \sin \omega t\,\text{V}$.

The diode blocks for $v_i < 6\,\text{V}$ and conducts for $v_i \geq 6\,\text{V}$. Thus, $v_o = v_i$ for $v_i < 6\,\text{V}$, and $v_o = 6\,\text{V}$ for $v_i \geq 6\,\text{V}$. The transfer characteristic is displayed in Fig. 2-34(*a*). For the given input signal, the output is a sine wave with the positive peak clipped at 6 V, as shown in Fig. 2-34(*b*).

2.19 Reverse the diode in Fig. 2-17(*a*) to create a negative clipping network. (*a*) Let $V_b = 6\,\text{V}$, and draw the network transfer characteristic. (*b*) Sketch one cycle of the output waveform if $v_S = 10 \sin \omega t\,\text{V}$.

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(*a*) (*b*)

Fig. 2-34

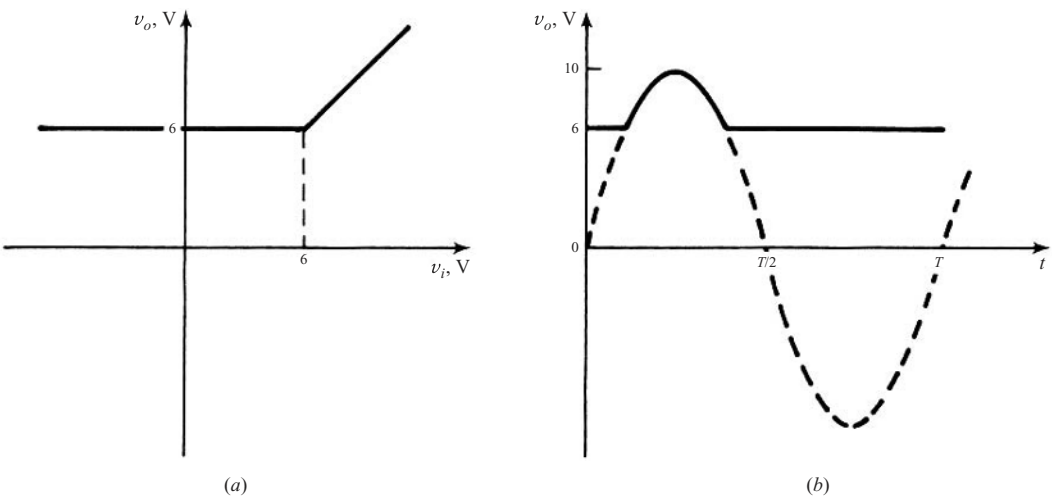
(*a*) The diode conducts for $v_i \leq 6\,\text{V}$ and blocks for $v_i > 6\,\text{V}$. Consequently, $v_o = v_i$ for $v_i > 6\,\text{V}$, and $v_o = 6\,\text{V}$ for $v_i \leq 6\,\text{V}$. The transfer characteristic is drawn in Fig. 2-35(*a*).

(*b*) With negative clipping, the output is made up of the positive peaks of $10 \sin \omega t$ above 6 V and is 6 V otherwise. Figure 2-35(*b*) displays the output waveform.

2.20 The signal, $v_i = 10 \sin \omega t\,\text{V}$, is applied to the negative clamping circuit of Fig. 2-18(*b*). Treating the diode as ideal, sketch the output waveform for $1\frac{1}{2}$ cycles of v_i. The capacitor is initially uncharged.

For $0 \leq t \leq T/4$, the diode is forward-biased, giving $v_o = 0$ as the capacitor charges to $v_C = +10\,\text{V}$. For $t > T/4$, $v_o \leq 0$, and thus the diode remains in the blocking mode, resulting in

$$v_o = -v_C + v_i = -10 + v_i = -10(1 - \sin \omega t) \quad \text{V}$$



(*a*) (*b*)

Fig. 2-35

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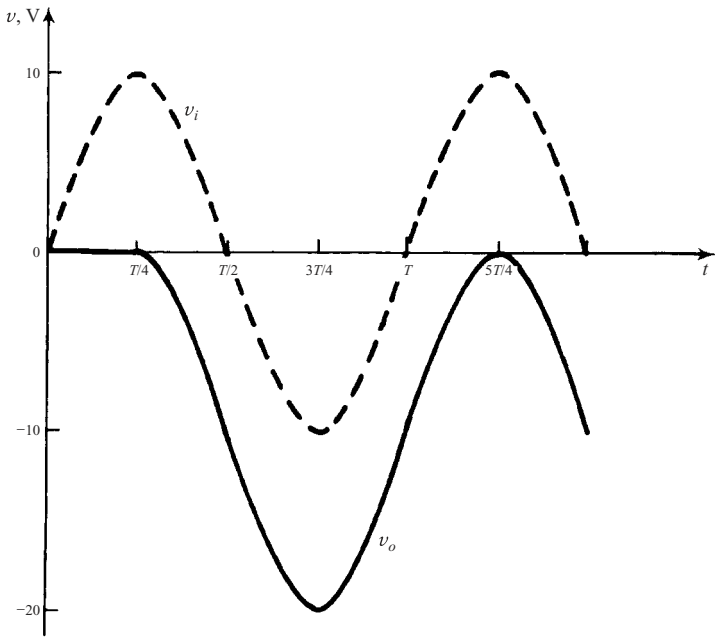


Fig. 2-36

The output waveform is sketched in Fig. 2-36.

2.21 The diodes in the circuit of Fig. 2-37 are ideal. Sketch the transfer characteristic for $-20\,\text{V} \le V_1 \le 20\,\text{V}$.

Inspection of the circuit shows that I_2 can have no component due to the 10-V battery because of the one-way conduction property of D_2. Therefore, D_1 is "off" for $V_1 < 0$; then $v_{D2} = -10\,\text{V}$ and $V_2 = 0$.

Now D_1 is "on" if $V_1 \ge 0$; however, D_2 is "off" for $V_2 < 10$. The onset of conduction for D_2 occurs when $V_{ab} = 10$ V with $I_2 = 0$, or when, by voltage division,

$$V_{ab} = V_2 = 10 = \frac{R_2}{R_1 + R_2} V_1$$

Hence,

$$V_1 = \frac{R_1 + R_2}{R_2} 10 = \frac{5 + 10}{10} 10 = 15\,\text{V} \qquad (1)$$

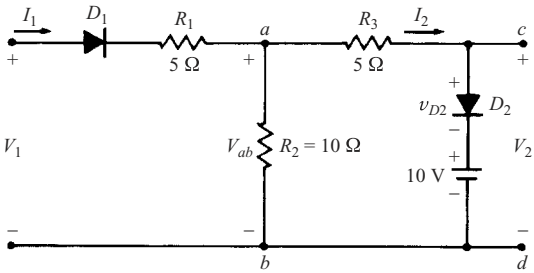


Fig. 2-37

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Thus, if $V_1 \geq 15\,\text{V}$, D_2 is "on" and $V_2 = 10\,\text{V}$. But, for $0 \leq V_1 < 15\,\text{V}$, D_2 is "off," $I_2 = 0$, and V_2 is given as a function of V_1 by (*1*). Figure 2-38 shows the composite result.

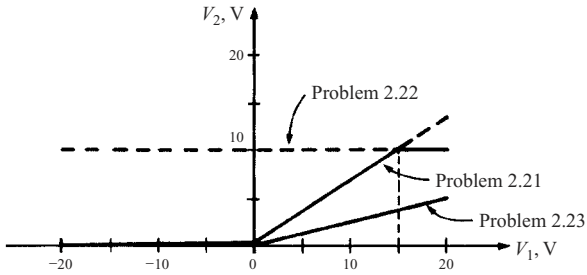


Fig. 2-38

2.22 Suppose diode D_2 is reversed in the circuit of Fig. 2-37. Sketch the resulting transfer characteristic for $-20 \leq V_1 \leq 20\,\text{V}$.

Diode D_2 is now "on" and $V_2 = 10\,\text{V}$ until V_1 increases enough so that $V_{ab} = 10\,\text{V}$, at which point $I_2 = 0$. That is, $V_2 = 10\,\text{V}$ until

$$V_2 = V_{ab} = 10 = \frac{R_2}{R_1 + R_2} V_1 = \frac{10}{5 + 10} V_1 = \frac{2}{3} V_1 \qquad (1)$$

or until

$$V_1 = \tfrac{3}{2} V_2 = 15\,\text{V}$$

For $V_1 > 15\,\text{V}$, $I_2 = 0$ and (*1*) remains valid. The resulting transfer characteristic is shown dashed in Fig. 2-38.

2.23 Suppose a resistor $R_4 = 5\,\Omega$ is added across terminals c, d of the circuit of Fig. 2-37. Describe the changes that result in the transfer characteristic of Problem 2.21.

There is no change in the transfer characteristic for $V_1 \leq 0$. However, D_2 remains "off" until $V_1 > 0$ increases to where $V_2 = 10\,\text{V}$. At the onset of conduction for D_2, the current through D_2 is zero; thus,

$$I_1 = \frac{V_1}{R_1 + R_2 \| (R_3 + R_4)} = \frac{V_1}{10} \qquad \text{and} \qquad I_2 = \frac{R_2}{R_2 + R_3 + R_4} I_1 = \frac{I_1}{2}$$

Hence, by Ohm's law,

$$V_2 = I_2 R_4 = \frac{I_1 R_4}{2} = \frac{V_1 R_4}{20} = \frac{V_1}{4}$$

Thus, $V_1 = 40\,\text{V}$ when $V_2 = 10\,\text{V}$, and it is apparent that the breakpoint of Problem 2.21 at $V_1 = 15\,\text{V}$ has moved to $V_1 = 40\,\text{V}$. The transfer characteristic for $-20 \leq V_1 \leq 20$ is sketched in Fig. 2-38.

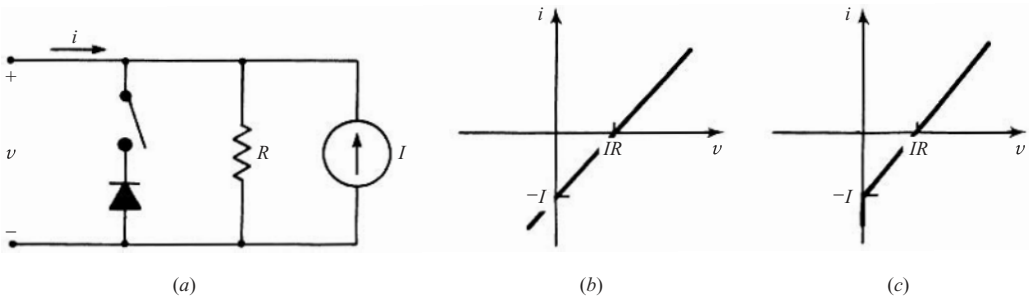
2.24 Sketch the i-v input characteristic of the network of Fig. 2-39(*a*) when (*a*) the switch is open and (*b*) the switch is closed.

The solution is more easily found if the current source and resistor are replaced with the Thévenin equivalents $V_{Th} = IR$ and $R_{Th} = R$.

(*a*) KVL gives $v = iR_{Th} + IR$, which is the equation of a straight line intersecting the i axis at $-I$ and the v axis at IR. The slope of the line is $1/R$. The characteristic is sketched in Fig. 2-39(*b*).

(*b*) The diode is reverse-biased and acts as an open circuit when $v > 0$. It follows that the i-v characteristic here is identical to that with the switch open if $v > 0$. But if $v \leq 0$, the diode is forward-biased, acting

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(*a*) (*b*) (*c*)

Fig. 2-39

as a short circuit. Consequently, v can never reach the negative values, and the current i can increase negatively without limit. The corresponding i-v plot is sketched in Fig. 2-39(*c*).

2.25 In the small-signal circuit of Fig. 2-40, the capacitor models the diode diffusion capacitance, so that $C = C_d = 0.02\,\mu\text{F}$, and v_{th} is known to be of frequency $\omega = 10^7$ rad/s. Also, $r_d = 2.5\,\Omega$ and $Z_{Th} = R_{Th} = 10\,\Omega$. Find the phase angle (*a*) between i_d and v_d and (*b*) between v_d and v_{th}.

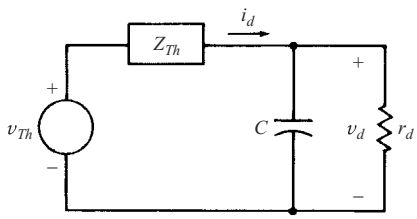


Fig. 2-40

(*a*) The diffusion capacitance produces a reactance

$$x_d = \frac{1}{\omega C_d} = \frac{1}{(10^7)(0.02 \times 10^{-6})} = 5\,\Omega$$

so that

$$Z_d = r_d \| (-jx_d) = \frac{(2.5)(5\underline{|-90^\circ})}{2.5 - j5} = 2.236\underline{|-26.57^\circ} = 2 - j1\,\Omega$$

Thus, i_d leads v_d by a phase angle of 26.57°.

(*b*) Let Z_{eq} be the impedance looking to the right from v_{th}; then

$$Z_{eq} = Z_{Th} + Z_d = 10 + (2 - j1) = 12 - j1 = 12.04\underline{|-4.76^\circ}\,\Omega$$

Hence, v_{th} leads v_d by an angle of $26.57^\circ - 4.76^\circ = 21.81^\circ$.

2.26 Using ideal diodes, resistors, and batteries, synthesize a function-generator circuit that will yield the i-v characteristic of Fig. 2-41(*a*).

Since the i-v characteristic has two breakpoints, two diodes are required. Both diodes must be oriented so that no current flows for $v < -5\,\text{V}$. Further, one diode must move into forward bias at the first breakpoint, $v = -5\,\text{V}$, and the second diode must begin conduction at $v = +10\,\text{V}$. Note also that the slope of the i-v plot is the reciprocal of the Thévenin equivalent resistance of the active portion of the network.

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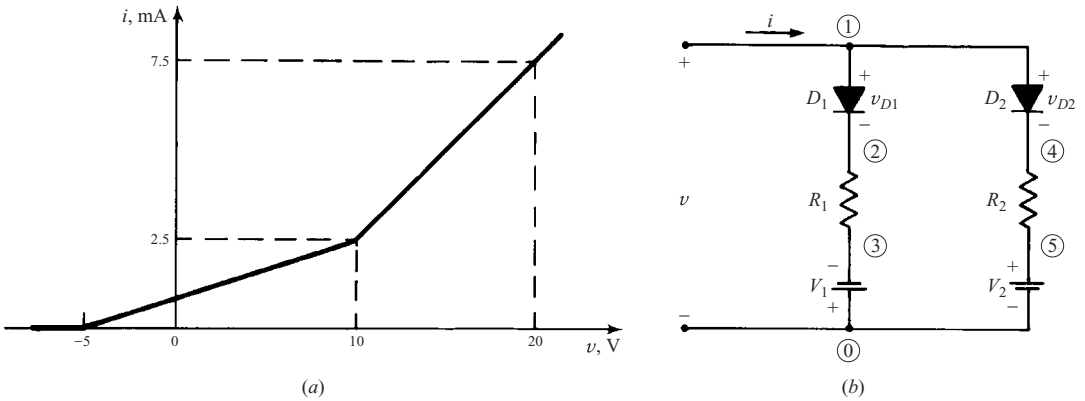


Fig. 2-41

The circuit of Fig. 2-41(*b*) will produce the given *i*-*v* plot if $R_1 = 6\,\text{k}\Omega$, $R_2 = 3\,\text{k}\Omega$, $V_1 = 5\,\text{V}$, and $V_2 = 10\,\text{V}$. These values are arrived at as follows:

1. If $v < -5\,\text{V}$, both v_{D1} and v_{D2} are negative, both diodes block, and no current flows.
2. If $-5 \le v < 10\,\text{V}$, D_1 is forward-biased and acts as a short circuit, whereas v_{D2} is negative, causing D_2 to act as an open circuit. R_1 is found as the reciprocal of the slope in that range:

$$R_1 = \frac{10 - (-5)}{0.0025} = 6\,\text{k}\Omega$$

3. If $v \ge 10\,\text{V}$, both diodes are forward-biased,

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{\Delta v}{\Delta i} = \frac{20 - 10}{(7.5 - 2.5) \times 10^{-3}} = 2\,\text{k}\Omega$$

and

$$R_2 = \frac{R_1 R_{Th}}{R_1 - R_{Th}} = \frac{(6 \times 10^3)(2 \times 10^3)}{4 \times 10^3} = 3\,\text{k}\Omega$$

2.27 For the resistor and battery values of Problem 2.26, use SPICE methods to simulate the function generator circuit of Fig. 2-41(*b*). Implement using default diode parameters. Determine the values of input voltage v for which the two break points occur.

The describing netlist code appears below:

```
Prb2_27.CIR
v  1 0 DC 0V
D1 1 2 DMOD
R1 2 3 6kohm
V1 0 3 DC 5V
D2 1 4 DMOD
R2 4 5 3kohm
V2 5 0 DC 10V
.DC v -10V 25V 0.25V
.MODEL DMOD D ( )
.PROBE
.END
```

After executing <Prb2_27.CIR>, the Probe feature is used to plot the resulting *i*-*v* characteristic of Fig. 2-42, where it is seen that the nonideal diodes have resulted in shifts of the $-5\,\text{V}$ and $-10\,\text{V}$ break points of Fig. 2-41(*a*) to $-4.54\,\text{V}$ and $10.61\,\text{V}$, respectively.

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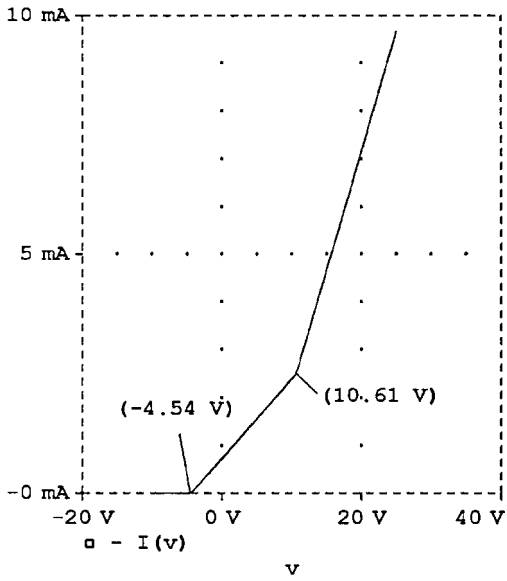
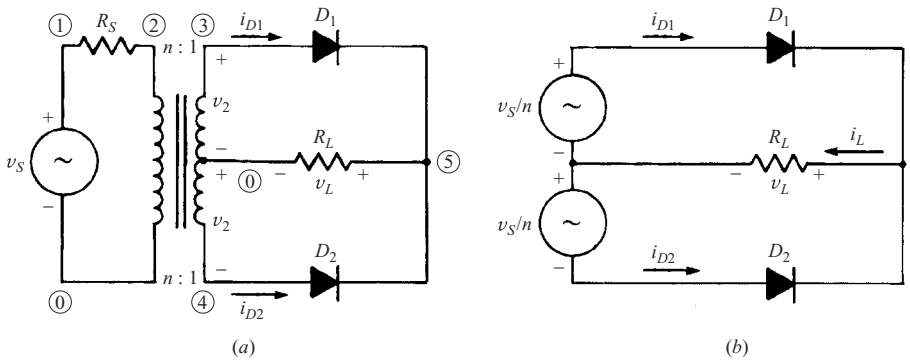


Fig. 2-42

2.28 Find v_L for the full-wave rectifier circuit of Fig. 2-43(a), treating the transformer and diodes as ideal. Assume $R_S = 0$.



(a) (b)

Fig. 2-43

The two voltages labeled v_2 in Fig. 2-43(a) are identical in magnitude and phase. The ideal transformer and the voltage source v_S can therefore be replaced with two identical voltage sources, as in Fig. 2-43(b), without altering the electrical performance of the balance of the network. When v_S/n is positive, D_1 is forward-biased and conducts but D_2 is reverse-biased and blocks. Conversely, when v_S/n is negative, D_2 conducts and D_1 blocks. In short,

$$i_{D1} = \begin{cases} \dfrac{v_S/n}{R_L} & \dfrac{v_S}{n} \geq 0 \\ 0 & \dfrac{v_s}{n} < 0 \end{cases} \qquad \text{and} \qquad i_{D2} = \begin{cases} 0 & \dfrac{v_S}{n} > 0 \\ -\dfrac{v_S/n}{R_L} & \dfrac{v_S}{n} \leq 0 \end{cases}$$

By KCL,
$$i_L = i_{D1} + i_{D2} = \frac{|v_S/n|}{R_L}$$

and so $v_L = R_L i_L = |v_S/n|$.

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2.29 For the full-wave rectifier circuit of Fig. 2-43(*a*), let $v_S = 120\sqrt{2}\sin(120\pi t)$ V, $R_S = 0.001\,\Omega$, $R_L = 5\,\Omega$, and the ideal transformer has a turns ratio of 10:1. Using SPICE methods and assuming ideal diodes, plot the output voltage v_L and diode currents i_{D1} and i_{D2}. Compare the results with predicted values based on the solution of Problem 2.28.

The netlist code for analysis of the circuit is

```
Prb2_29.CIR - FW rectifier
vs 1 0 SIN( 0V {sqrt(2)*120V} 60Hz )
Rs 1 2 0.0010ohm
* Ideal transformer, 10:1 ratio
L1 2 0 1H IC=-0.39A
L2 3 0 10mH
L3 0 4 10mH
kall L1 L2 L3 1
D1 3 5 DMOD
D2 4 5 DMOD
RL 5 0 5ohm
.MODEL DMOD D(n=0.0001) ; Ideal diode
.TRAN 1us 16.667ms 0s 1e-6s UIC
.PROBE
.END
```

Execution of <Prb2_29.CIR> and use of the Probe feature of PSpice result in the plots of Fig. 2-44 where the peak values of v_L and i_{D1} have been marked.

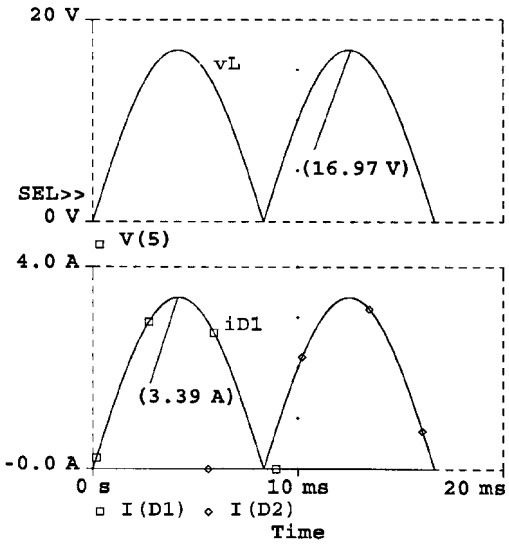


Fig. 2-44

Based on the results of Problem 2.28, the predicted peak values of v_L and i_{D1} are given by

$$i_{D1\,\max} = \frac{v_{S\,\max}/n}{R_L} = \frac{120\sqrt{2}/10}{5} = 3.39\,\text{A}$$

$$v_{L\,\max} = \frac{v_{S\,\max}}{n} = \frac{120\sqrt{2}}{10} = 16.97\,\text{V}$$

The predicted values and the SPICE results are in agreement.

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2.30 The Zener diode in the voltage-regulator circuit of Fig. 2-45 has a constant reverse breakdown voltage $V_Z = 8.2\,\text{V}$, for $75\,\text{mA} \le i_Z \le 1\,\text{A}$. If $R_L = 9\,\Omega$, size R_S so that $v_L = V_Z$ is regulated to (maintained at) 8.2 V while V_b varies by ±10 percent from its nominal value of 12 V.

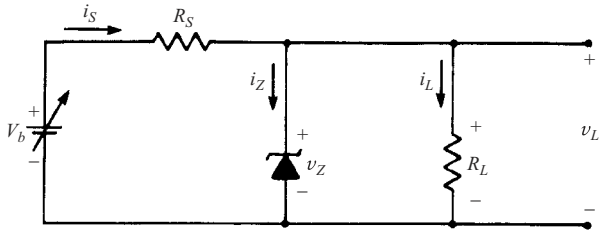


Fig. 2-45

By Ohm's law

$$i_L = \frac{v_L}{R_L} = \frac{V_Z}{R_L} = \frac{8.2}{9} = 0.911\,\text{A}$$

Now an application of KVL gives

$$R_S = \frac{V_b - V_Z}{i_Z + i_L} \tag{1}$$

and we use (*1*) to size R_S for maximum Zener current I_Z at the largest value of V_b:

$$R_S = \frac{(1.1)(12) - 8.2}{1 + 0.911} = 2.62\,\Omega$$

Now we check to see if $i_Z \ge 75\,\text{mA}$ at the lowest value of V_b:

$$i_Z = \frac{V_b - v_Z}{R_S} - i_L = \frac{(0.9)(12) - 8.2}{2.62} - 0.911 = 81.3\,\text{mA}$$

Since $i_Z > 75\,\text{mA}$, $v_Z = V_Z = 8.2\,\text{V}$ and regulation is preserved.

2.31 A Zener diode has the specifications $V_Z = 5.2\,\text{V}$ and $P_{D\max} = 260\,\text{mW}$. Assume $R_Z = 0$. (*a*) Find the maximum allowable current i_Z when the Zener diode is acting as a regulator. (*b*) If a single-loop circuit consists of an ideal 15-V dc source V_S, a variable resistor R, and the described Zener diode, find the range of values of R for which the Zener diode remains in constant reverse breakdown with no danger of failure.

(*a*)
$$i_{Z\max} = I_Z = \frac{P_{D\max}}{V_Z} + \frac{260 \times 10^{-3}}{5.2} = 50\,\text{mA}$$

(*b*) By KVL,

$$V_S = Ri_Z + V_Z \qquad \text{so that} \qquad R = \frac{V_s - V_Z}{i_Z}$$

From Section 2.10, we know that regulation is preserved if

$$R \le \frac{V_S - V_Z}{0.1 I_{Z\max}} = \frac{15 - 5.2}{(0.1)(50 \times 10^{-3})} = 1.96\,\text{k}\Omega$$

Overcurrent failure is avoided if

$$R \ge \frac{V_S - V_Z}{I_{Z\max}} = \frac{15 - 5.2}{50 \times 10^{-3}} = 196\,\Omega$$

Thus, we need $196\,\Omega \le R \le 196\,\text{k}\Omega$.

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2.32 A *light-emitting diode* (LED) has a greater forward voltage drop than does a common signal diode. A typical LED can be modeled as a constant forward voltage drop $v_D = 1.6\,\text{V}$. Its *luminous intensity* I_v varies directly with forward current and is described by

$$I_v = 40 i_D \approx \text{millicandela (mcd)}$$

A series circuit consists of such an LED, a current-limiting resistor R, and a 5-V dc source V_S. Find the value of R such that the luminous intensity is 1 mcd.

By (*1*), we must have

$$i_D = \frac{I_v}{40} = \frac{1}{40} = 25\,\text{mA}$$

From KVL, we have

$$V_S = R i_D + 1.6$$

so that

$$R = \frac{V_S - 1.6}{i_D} = \frac{5 - 1.6}{25 \times 10^{-3}} = 136\,\Omega$$

2.33 The reverse breakdown voltage V_R of the LED of Problem 2.32 is guaranteed by the manufacturer to be no lower than 3 V. Knowing that the 5-V dc source may be inadvertently applied so as to reverse-bias the LED, we wish to add a Zener diode to ensure that reverse breakdown of the LED can never occur. A Zener diode is available with $V_Z = 4.2\,\text{V}$, $I_Z = 30\,\text{mA}$, and a forward drop of 0.6 V. Describe the proper connection of the Zener in the circuit to protect the LED, and find the value of the luminous intensity that will result if R is unchanged from Problem 2.32.

The Zener diode and LED should be connected in series to that the anode of one device connects to the cathode of the other. Then, even if the 5-V source is connected in reverse, the reverse voltage across the LED will be less than $5 - 4.2 = 0.8\,\text{V} < 3\,\text{V}$. When the dc source is connected to forward-bias the LED, we will have

$$i_D = \frac{V_S - V_{F\text{LED}} - V_{FZ}}{R} = \frac{5 - 1.6 - 0.6}{136} = 20.6\,\text{mA}$$

so that

$$I_v = 40 i_D = (40)(20.6 \times 10^{-3}) = 0.824\,\text{mcd}$$

Supplementary Problems

2.34 A Si diode has a saturation currrent $I_o = 10\,\text{nA}$ at $T = 300^\circ\text{K}$. (*a*) Find the forward current i_D if the forward drop v_D is 0.5 V. (*b*) This diode is rated for a maximum current of 5 A. What is its junction temperature at rated current if the forward drop is 0.7 V. *Ans.* (*a*) 2.47 A; (*b*) 405.4°K

2.35 Solve Problem 2.1 for a Si diode. *Ans.* $v_D > .0.2372\,\text{V}$

2.36 Laboratory data for a Si diode described by (*2.1*) show that $i_D = 2\,\text{mA}$ when $v_D = 0.6\,\text{V}$, and $i_D = 10\,\text{mA}$ for $v_D = 0.7\,\text{V}$. Find (*a*) the temperature for which the data were taken, and (*b*) the reverse saturation current. *Ans.* (*a*) 87.19°C; (*b*) $2.397\,\mu\text{A}$

2.37 For what voltage v_D will the reverse current of a Ge diode that is described by (*2.1*) reach 99 percent of its saturation value at a temperature of 300°K? *Ans.* $v_D = -0.1191\,\text{V}$

2.38 Find the increase in temperature ΔT necessary to increase the reverse saturation current of a diode by a factor of 100. *Ans.* 66.4°C

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2.39 The diode of Problem 2.34 is operating in a circuit where it has dynamic resistance $r_d = 100\,\Omega$. What must be the quiescent conditions? *Ans.* $V_{DQ} = 0.263\,\text{V}$, $I_{DQ} = 0.259\,\text{mA}$

2.40 The diode of Problem 2.34 has a forward current $i_D = 2 + 0.004 \sin \omega t\,\text{mA}$. Find the total voltage, $v_D = V_{DQ} + v_d$, across the diode. *Ans.* $v_D = 339.5 + 0.0207 \sin \omega t\,\text{mV}$

2.41 Find the power dissipated in the load resistor $R_L = 100\,\Omega$ of the circuit of Fig. 2-22(*a*) if the diode is ideal and $v_S = 10 \sin \omega t\,\text{V}$. *Ans.* 206.6 mW

2.42 The logic AND gate of Fig. 2-46(*a*) has trains of input pulses arriving at the gate inputs, as indicated by Fig. 2-47(*b*). Signal v_2 is erratic, dropping below nominal logic level on occasion. Determine v_o. *Ans.* 10 V for $1 \le t \le 2\,\text{ms}$, 5 V for $4 \le t \le 5\,\text{ms}$, zero otherwise.

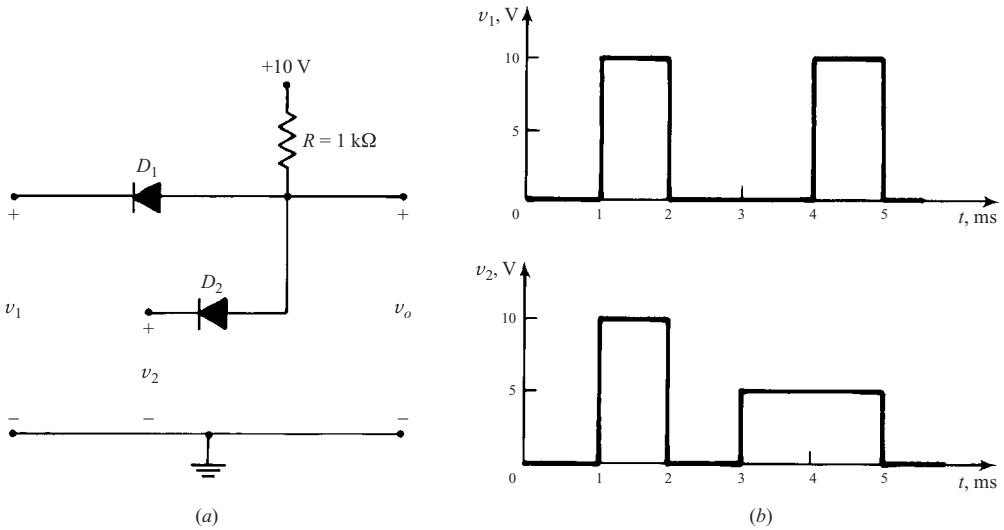


Fig. 2-46

2.43 The logic AND gate of Fig. 2-46(*a*) is to be used to generate a crude pulse train by letting $v_1 = 10 \sin \omega t\,\text{V}$ and $v_2 = 5\,\text{V}$. Determine (*a*) the amplitude and (*b*) the period of the pulse train appearing as v_o. *Ans.* (*a*) 5 V; (*b*) $2\pi/\omega$

2.44 In the circuit of Fig. 2-29, v_S is a 10-V square wave with a 4-ms period. The diode is nonideal, with the characteristic of Fig. 2-26(*b*). If the capacitor is initially uncharged, determine v_C for the first cycle of v_s. *Ans.* $9.5(1 - e^{-333.3t})\,\text{V}$ for $0 \le t < 2\,\text{ms}$ and 4.62 V for $2 \le t < 4\,\text{ms}$

2.45 The forward voltage across the diode of Problem 2.35 is $v_D = 0.3 + 0.060 \cos t\,\text{V}$. Find the ac component of the diode current i_d. *Ans.* $2.52 \cos t\,\text{mA}$

2.46 The circuit of Fig. 2-47(*a*) is a voltage-doubler circuit, sometimes used as a low-level power supply when the load R_L is reasonably constant. It is called a "doubler" because the steady-state peak value of v_L is twice the peak value of the sinusoidal source voltage. Figure 2-47(*b*) is a sketch of the steady-state output voltage for $v_s = 10 \cos \omega t\,\text{V}$. Assume ideal diodes, $\omega = 120\pi\,\text{rad/s}$, $C_1 = 20\,\mu\text{F}$, $C_2 = 100\,\mu\text{F}$, and $R_L = 20\,\text{k}\Omega$. (*a*) Solve by SPICE methods for the decay time t_d. (*b*) From the SPICE results, determine the peak-to-peak value of the ripple voltage. (*Netlist code available from author website.*)
Ans. (*a*) 15.52 ms; (*b*) 0.75 V

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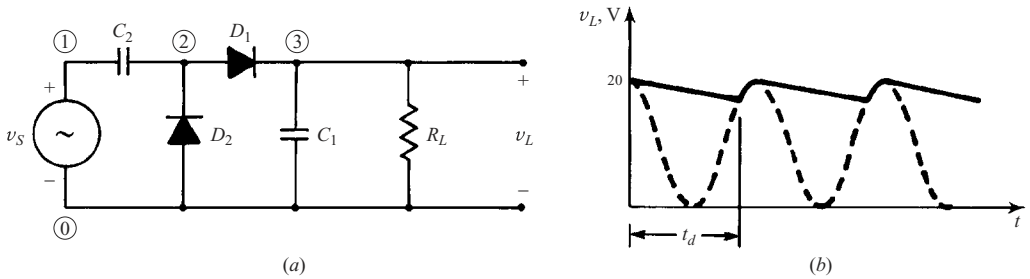


Fig. 2-47

2.47 Find the diode current during one capacitor-charging cycle in the rectifier circuit of Fig. 2-15(*a*) if $C = 47\,\mu\text{F}$, $R_L = 1\,\text{k}\Omega$, and $v_S = 90\cos 2000t\,\text{V}$. (*Hint*: The approximate ripple formula cannot be used, as it implicitly assumes zero capacitor charging time. Instead, solve for capacitor current and load current, and add.) *Ans.* $i_D = -8.49\sin(2000t - 0.6^\circ)\,\text{A}$ for $2.966\,\text{ms} \le t < 3.142\,\text{ms}$

2.48 In the circuit of Fig. 2-32, $R_1 = R_L = 10\,\Omega$. If the diode is ideal and $v_S = 10\sin\omega t\,\text{V}$, find the average value of the load voltage v_L. *Ans.* 3.18 V

2.49 Rework Problem 2.20 with the diode of Fig. 2-18(*b*) reversed and all else unchanged. (The circuit is now a positive clamping circuit.)
Ans. $v_o = 10\sin\omega t\,\text{V}$ for $0 \le t < T/2$, 0 for $T/2 \le t < 3T/4$, and $10(1 - \sin\omega t)\,\text{V}$ for $t \ge 3T/4$

2.50 Four diodes are utilized for the full-wave bridge of Fig. 2-48. Assuming that the diodes are ideal and that $v_S = V_m\sin\omega t$, (*a*) find the output voltage v_L and (*b*) find the average value of v_L.
Ans. (*a*) $v_L = V_m|\sin\omega t|\,\text{V}$; (*b*) $V_{L0} = 2V_m/\pi$

2.51 A shunt filter capacitor (see Example 2.13) is added to the full-wave rectifier of Problem 2.50. Show that the ripple factor is given by $F_r = 2/(4fR_LC - 1) \approx 1/2fR_LC$.

2.52 Add a $470\,\mu\text{F}$ filter capacitor across points *a*, *b* in the full-wave rectifier circuit of Fig. 2-48. If $R_L = 1\,\text{k}\Omega$ and $v_S = 120\sqrt{2}\sin(120\pi t)\,\text{V}$, use SPICE methods to determine (*a*) the magnitude (peak-to-peak) of the output ripple voltage and (*b*) the average value of output voltage. (*Netlist code available at author website.*) *Ans.* (*a*) $\Delta v_L = 2.79\,\text{V}$; (*b*) $V_{L0} = 168.34\,\text{V}$

2.53 The *level-discriminator circuit* (Fig. 2-49) has an output of zero, regardless of the polarity of the input signal, until the input reaches a threshold value. Above the threshold value, the output duplicates the input. Such a circuit can sometimes be used to eliminate the effects of low-level noise at the expense of slight distortion. Relate v_o to v_i for the circuit.
Ans. $v_o = v_i(1 - A/|v_i|)$ for $|v_i| > A$, and 0 for $|v_i| \le A$

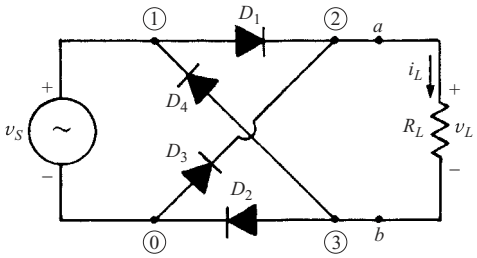


Fig. 2-48

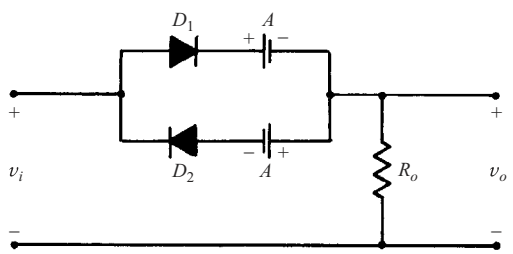


Fig. 2-49

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2.54 The diode of Fig. 2-39(*a*) is reversed, but all else remains the same. Write an equation relating v and i when (*a*) the switch is open and (*b*) the switch is closed.
Ans. (*a*) $v = R(i + I)$; (*b*) $v = R(i + I)$ for $i < I$, and $v = 0$ for $i \geq I$

2.55 The Zener diode in the voltage-regulator circuit of Fig. 2-45 has $v_Z = V_Z = 18.6\,\text{V}$ at a minimum i_Z of 15 mA. If $V_b = 24 \pm 3\,\text{V}$ and R_L varies from 250 Ω to 2 kΩ, (*a*) find the maximum value of R_S to maintain regulation and (*b*) specify the minimum power rating of the Zener diode.
Ans. (*a*) 26.8 Ω; (*b*) 4.65 W

2.56 The regulator circuit of Fig. 2-45 is modified by replacing the Zener diode with two Zener diodes in series to obtain a regulation voltage of 20 V. The characteristics of the two Zeners are

Zener 1: $V_Z = 9.2\,\text{V}$ for $15 \leq i_Z \leq 300\,\text{mA}$
Zener 2: $V_Z = 10.8\,\text{V}$ for $12 \leq i_Z \leq 240\,\text{mA}$

(*a*) if i_L varies from 10 mA to 90 mA and V_b varies from 22 V to 26 V, size R_S so that regulation is preserved. (*b*) Will either Zener exceed its rated current?
Ans. (*a*) 19.6 Ω; (*b*) for $V_b = 26\,\text{V}$, $i_{Z1} = i_{Z2} = 296\,\text{mA}$, which exceeds the rating of Zener 2

2.57 The two Zener diodes of Fig. 2-50 have negligible forward drops, and both regulate at constant V_Z for $50\,\text{mA} \leq i_Z \leq 500\,\text{mA}$. If $R_1 = R_L = 10\,\Omega$, $V_{Z1} = 8\,\text{V}$, and $V_{Z2} = 5\,\text{V}$, find the average value of load voltage when v_i is a 10-V square wave. *Ans.* 0.75 V

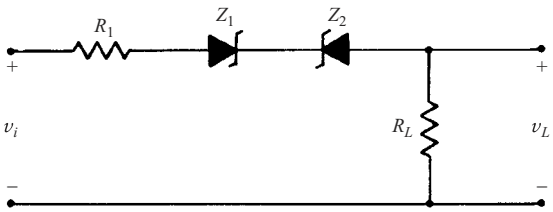


Fig. 2-50

2.58 The Zener diode of Problem 2.31 is used in a simple series circuit consisting of a variable dc voltage source V_S, the Zener diode, and a current-limiting resistor $R = 1\,\text{k}\Omega$. (*a*) Find the allowable range of V_S for which the Zener diode is safe and regulation is preserved. (*b*) Find an expression for the power dissipated by the Zener diode. *Ans.* (*a*) $10.2\,\text{V} \leq V_S \leq 55.2\,\text{V}$; (*b*) $P_D = V_Z(V_S - V_Z)/R$

2.59 The *varactor diode* is designed to operate reverse-biased and is manufactured by a process that increases the voltage-dependent depletion capacitance or junction capacitance C_j. A varactor diode is frequently connected in parallel with an inductor L to form a resonant circuit for which the resonant frequency, $f_R = 1/2\pi\sqrt{LC_j}$, is voltage-dependent. Such a circuit can form the basis of a *frequency modulation* (FM) transmitter. A varactor diode whose depletion capacitance is $C_j = 10^{-11}/(1 - 0.75v_D)^{1/2}\,\text{F}$ is connected in parallel with a 0.8-μH inductor; find the value of v_D required to establish resonance at a frequency of 100 MHz. *Ans.* $v_D = -11.966\,\text{V}$

2.60 An LED with luminous intensity described by (*1*) of Problem 2.32 is modeled by the piecewise-linear function of Fig. 2-11(*b*), with $R_F = 3\,\Omega$ and $V_F = 1.5\,\text{V}$. Find the maximum and minimum luminous intensities that result if the LED is used in a series circuit consisting of the LED, a current-limiting resistor $R = 125\,\Omega$, and a source $v_S = 5 + 1.13 \sin 0.1t\,\text{V}$. (*Note*: Since the period of v_S exceeds 1 minute, it is logical to assume that luminous intensity follows i_D without the necessity to consider the physics of the light-emitting process.) *Ans.* $I_{v\max} = 1.798\,\text{mcd}$, $I_{v\min} = 0.9204\,\text{mcd}$

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CHAPTER 3

Characteristics of Bipolar Junction Transistors

3.1. BJT CONSTRUCTION AND SYMBOLS

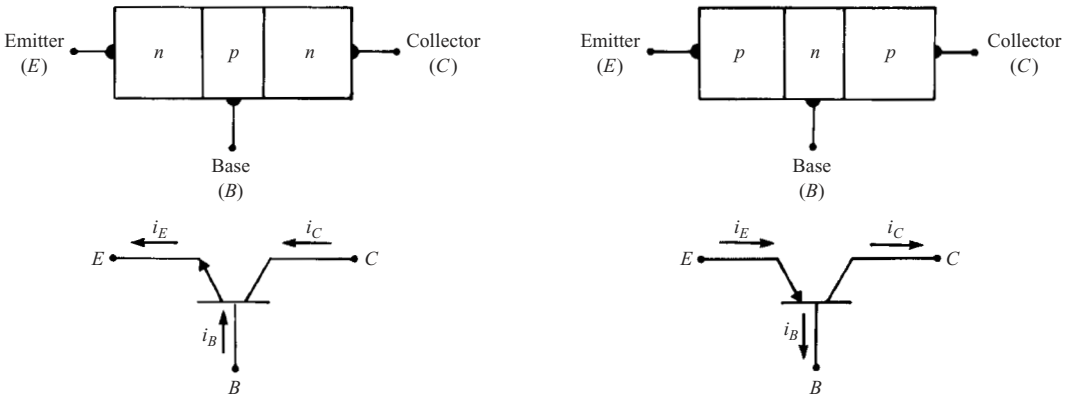
The *bipolar junction transistor* (BJT) is a three-element (*emitter*, *base*, and *collector*) device made up of alternating layers of *n*- and *p*-type semiconductor materials joined metallurgically. The transistor can be of *pnp* type (principal conduction by positive holes) or of *npn* type (principal conduction by negative electrons), as shown in Fig. 3-1 (where schematic symbols and positive current directions are also shown). The double-subscript notation is utilized in labeling terminal voltages, so that, for example, v_{BE} symbolizes the increase in potential from emitter terminal E to base terminal B. For reasons that will become apparent, terminal currents and voltages commonly consist of superimposed dc and ac components (usually sinusoidal signals). Table 3-1 presents the notation for terminal voltages and currents.

Table 3-1

Type of Value	Symbol		Examples
	Variable	Subscript	
total instantaneous	lowercase	uppercase	i_B, v_{BE}
dc	uppercase	uppercase	I_B, V_{BE}
quiescent-point	uppercase	uppercase plus Q	I_{BQ}, V_{BEQ}
ac instantaneous	lowercase	lowercase	i_b, v_{be}
rms	uppercase	lowercase	I_b, V_{be}
maximum (sinusoid)	uppercase	lowercase plus m	I_{bm}, V_{bem}

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Example 3.1. In the *npn* transistor of Fig. 3-1(*a*), 10^8 holes/μs move from the base to the emitter region while 10^{10} electrons/μs move from the emitter to the base region. An ammeter reads the base current as $i_B = 16\,\mu$A. Determine the emitter current i_E and the collector current i_C.



(*a*) *npn* Transistor (*b*) *pnp* Transistor

Fig. 3-1

The emitter current is found as the net rate of flow of positive charge into the emitter region:

$$i_E = (1.602 \times 10^{-19}\ \text{C/hole})(10^{14}\ \text{holes/s}) - (-1.602 \times 10^{-19}\ \text{C/electron})(10^{16}\ \text{electrons/s})$$
$$= 1.602 \times 10^{-5} + 1.602 \times 10^{-3} = 1.618\ \text{mA}$$

Further, by KCL,

$$i_C = i_E - i_B = 1.618 \times 10^{-3} - 16 \times 10^{-6} = 1.602\ \text{mA}$$

3.2. COMMON-BASE TERMINAL CHARACTERISTICS

The *common-base* (CB) connection is a two-port transistor arrangement in which the base shares a common point with the input and output terminals. The independent input variables are emitter current i_E and base-to-emitter voltage v_{EB}. The corresponding independent output variables are collector current i_C and base-to-collector voltage v_{CB}. Practical CB transistor analysis is based on two experimentally determined sets of curves:

1. *Input* or *transfer characteristics* relate i_E and v_{EB} (port input variables), with v_{CB} (port output variable) held constant. The method of laboratory measurement is indicated in Fig. 3-2(*a*), and the typical form of the resulting family of curves is depicted in Fig. 3-2(*b*).
2. *Output* or *collector characteristics* give i_C as a function of v_{CB} (port output variables) for constant values of i_E (port input variable), measured as in Fig. 3-2(*a*). Figure 3-2(*c*) shows the typical form of the resulting family of curves.

3.3. COMMON-EMITTER TERMINAL CHARACTERISTICS

The *common-emitter* (CE) connection is a two-port transistor arrangement (widely used because of its high current amplification) in which the emitter shares a common point with the input and output terminals. The independent port input variables are base current i_B and emitter-to-base voltage v_{BE}, and

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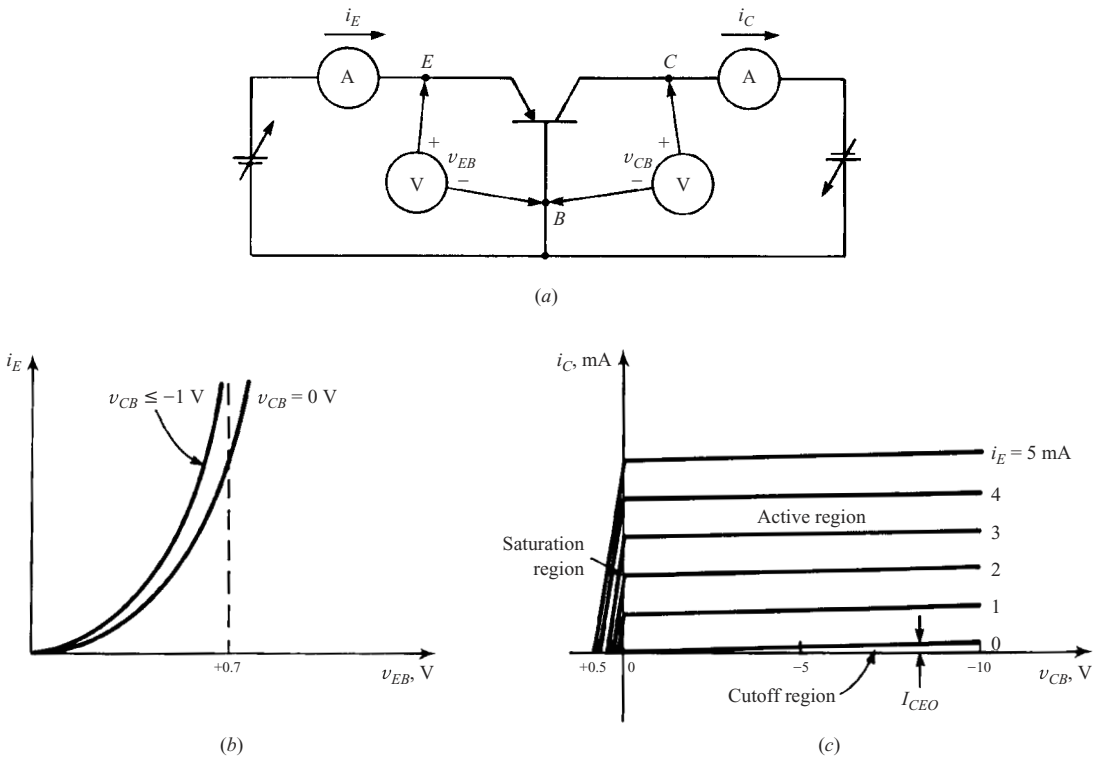


Fig. 3-2 Common-base characteristics (*pnp*, Si device)

the independent port output variables are collector current i_C and emitter-to-collector voltage v_{CE}. Like CB analysis, CE analysis is based on:

1. *Input* or *transfer characteristics* that relate the port input variables i_B and v_{BE}, with v_{CE} held constant. Figure 3-3(*a*) shows the measurement setup, and Fig. 3-3(*b*) the resulting input characteristics.
2. *Output* or *collector characteristics* that show the functional relationship between port outport variables i_C and v_{CE} for constant i_B, measured as in Fig. 3-3(*a*). Typical collector characteristics are displayed in Fig. 3-3(*c*).

3.4. BJT SPICE MODEL

The element specification statement for a BJT must explicitly name a model even if the default model parameters are intended for use. The general form of the transistor specification statement is as follows:

$$\text{Q}\cdots n_1\ n_2\ n_3\ \ \textit{model name}$$

Nodes n_1, n_2, and n_3 belong to the collector, base, and emitter, respectively. The *model name* is an arbitrary selection of alpha and numeric characters to uniquely identify the model. Positive current and voltage directions for the *pnp* and *npn* transistors are clarified by Fig. 3-4.

In addition, a .MODEL control statement must be added to the netlist code. This control statement specifies whether the transistor is *pnp* or *npn* and thus has one of the following two forms:

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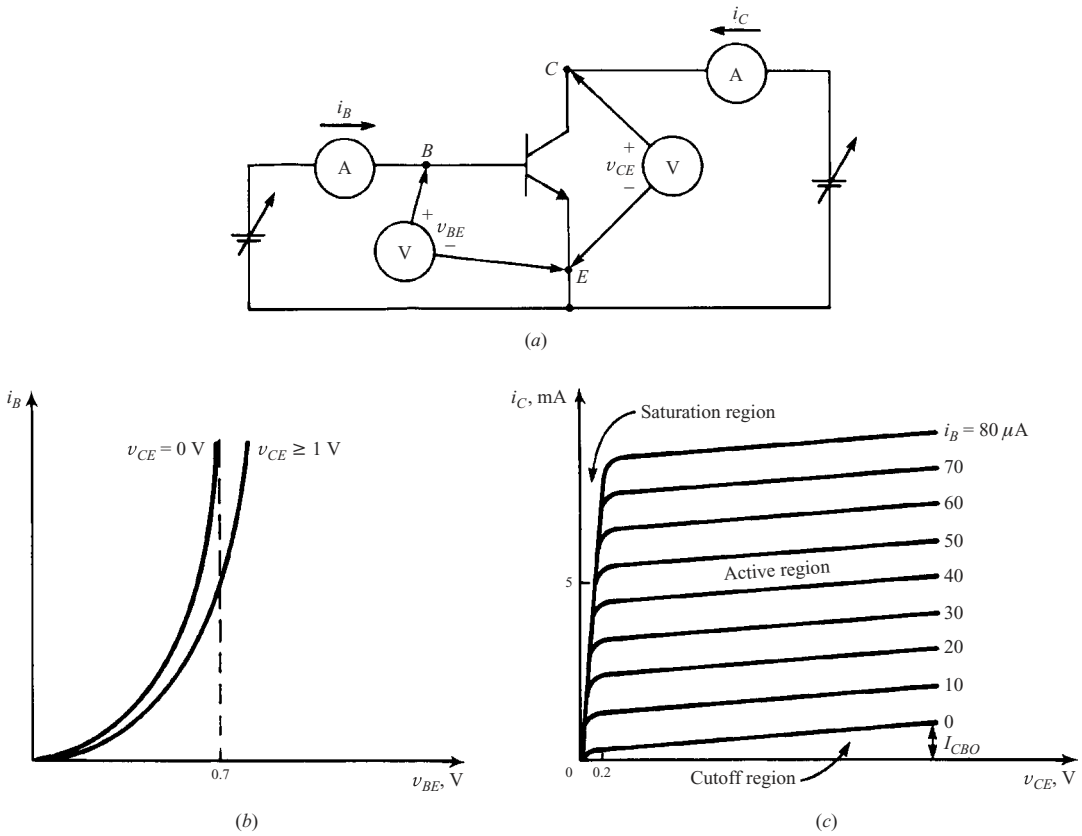


Fig. 3-3 Common-emitter characteristics (*npn*, Si device)

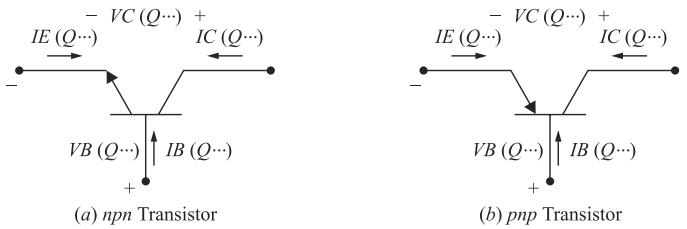


Fig. 3-4

.MODEL *model name* PNP (*parameters*)
.MODEL *model name* NPN (*parameters*)

If the parameter field is left blank, default values are assigned. Non-default desired parameter specifications are entered in the parameter field using the format *parameter name* = *value*. Specific parameters that are of concern in this book are documented by Table 3-2.

All parameter values are entered with positive values regardless of whether the transistor is *pnp* or *npn*. Two transistor models will be used in this chapter—*generic model* and *default model*—as introduced in Example 3.2.

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Table 3-2

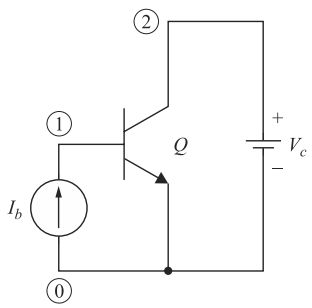
Parameter	Description	Major Impact	Default	Units
Is	saturation current	↑ Is, ↓ V_{BEQ}	1×10^{-16}	A
Ikf	high current roll-off	↓ Ikf, ↓ I_C	∞	A
Isc	base-collector leakage	↑ Isc, ↑ I_C	0	A
Bf	forward current gain	↑ Bf, ↑ I_C	100	
Br	reverse current gain	↑ Br, ↑ rev. I_C	1	
Rb	base resistance	↑ Rb, ↓ di_B/dv_{BE}	0	Ω
Rc	collector resistance	↑ Rc, ↑ V_{CEsat}	0	Ω
Va	forward Early voltage	↓ Va, ↑ di_C/dt	∞	V
Cjc	base-collector capacitance	high freq. response	0	F
Cje	base-emitter capacitance	high freq. response	0	F

Example 3.2. Use SPICE methods to generate the CE collector characteristics for an *npn* transistor characterized by (*a*) the default parameter values and (*b*) a reasonable set of values for the parameters appearing in Table 3-2.

(*a*) Figure 3-5(*a*) shows a connection method to obtain data for the collector characteristics. The netlist code that follows will generate the desired data for default parameter values.

```
Ex3_2.CIR
Ib 0 1 0uA
Q 2 1 0 QNPN
*Q 2 1 0 QNPNG
VC 2 0 0V
.MODEL QNPN NPN() ; Default BJT
*.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
*+ Br=3 Rb=1ohm Rc=1ohm Va=30V Cjc=10pF Cje=15pF)
.DC VC 0V 15V 1V Ib 0uA 150uA 25uA
.PROBE
.END
```

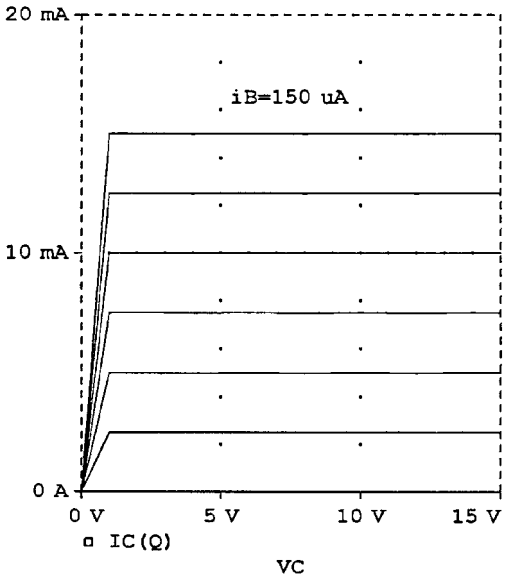
Execute ⟨Ex3_2.CIR⟩ and use the Probe feature of PSpice to produce the collector characteristics for the *default BJT model* (QNPN or QPNP) shown by Fig. 3-5(*b*).



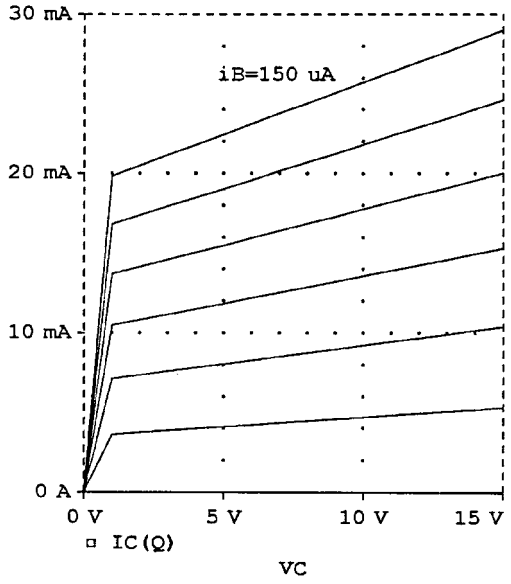
(*a*)

Fig. 3-5

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(*b*)

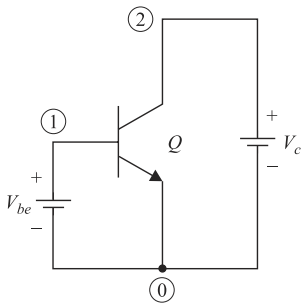


(*c*)

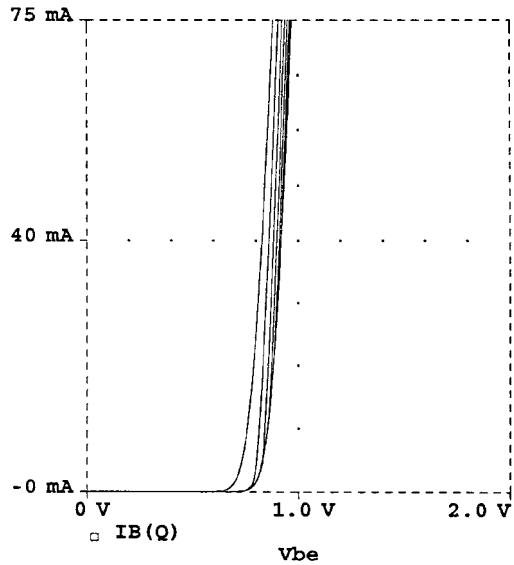
(*b*) Edit ⟨Ex3_2.CIR⟩ to move the leading asterisks up one position on both the transistor specification statement and the .MODEL statements. Execute the revised ⟨Ex3_2.CIR⟩ and use the Probe feature of PSpice to produce the collector characteristics for the *generic BJT model* (QNPNG or QPNPG) as displayed by Fig. 3-5(*c*).

Example 3.3. Apply SPICE methods to determine the CE transfer characteristics for the generic *npn* transistor (QNPNG).

Figure 3-6(*a*) presents the connection method chosen for determination of the transfer characteristics. The associated netlist code follows:



(*a*)



(*b*)

Fig. 3-6

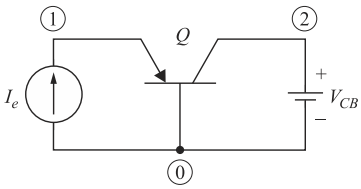
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```
Ex3_3.CIR
Vbe 1 0 0V
Q 2  1 0 QNPNG
Vc  2 0 1V
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=30V Cjc=10pF Cje=15pF)
.DC Vbe 0V 2V 0.01V Vc 0V 2V 0.2V
.PROBE
.END
```

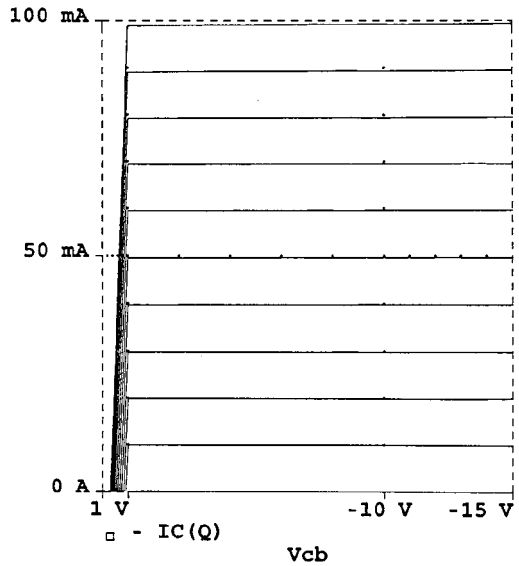
Execution of ⟨Ex3_3.CIR⟩ and use of the Probe feature of PSpice yields the desired transfer characteristics displayed by Fig. 3-6(*b*).

Example 3.4. Using SPICE methods, determine the CB collector characteristics for the generic *pnp* transistor (QPNPG).

Figure 3-7(*a*) shows the circuit for use in the determination. The netlist code below describes that circuit.



(*a*)



(*b*)

Fig. 3-7

```
Ex3_4.CIR
Ie  0 1 0mA
Q 2  0 1 QPNPG
Vcb 2 0 0V
.MODEL QPNPG pnp(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=30V Cjc=10pF Cje=15pF)
.DC Vcb 1V -15V 1V Ie 0mA 100mA 10mA
.PROBE
.END
```

Execution of ⟨Ex3_4.CIR⟩ and use of the Probe feature of PSpice results in the desired CB collector characteristics of Fig. 3-7(*b*).

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3.5. CURRENT RELATIONSHIPS

The two *pn* junctions of the BJT can be independently biased, to result in four possible transistor *operating modes* as summarized in Table 3-3. A junction is forward-biased if the *n* material is at a lower potential than the *p* material, and reverse-biased if the *n* material is at a higher potential than the *p* material.

Table 3-3

Emitter-Base Bias	Collector-Base Bias	Operating Mode
forward	forward	saturation
reverse	reverse	cutoff
reverse	forward	inverse
forward	reverse	linear or active

Saturation denotes operation (with $|v_{CE}| \approx 0.2\,\text{V}$ and $|v_{BC}| \approx 0.5\,\text{V}$ for Si devices) such that maximum collector current flows and the transistor acts much like a closed switch from collector to emitter terminals. [See Figures 3-2(*c*) and 3-3(*c*).]

Cutoff denotes operation near the voltage axis of the collector characteristics, where the transistor acts much like an open switch. Only leakage current (similar to I_o of the diode) flows in this mode of operation; thus, $i_C = I_{CEO} \approx 0$ for CB connection, and $i_C = I_{CBO} \approx 0$ for CE connection. Figures 3-2(*c*) and 3-3(*c*) indicate these leakage currents.

The *inverse* mode is a little-used, inefficient active mode with the emitter and collector interchanged.

The *active* or *linear* mode describes transistor operation in the region to the right of saturation and above cutoff in Figs. 3-2(*c*) and 3-3(*c*); here, near-linear relationships exist between terminal currents, and the following constants of proportionality are defined for dc currents:

$$\alpha(\equiv h_{FB}) \equiv \frac{I_C - I_{CBO}}{I_E} \tag{3.1}$$

$$\beta(\equiv h_{FE}) \equiv \frac{\alpha}{1-\alpha} \equiv \frac{I_C - I_{CEO}}{I_B} \tag{3.2}$$

where the thermally generated leakage currents are related by

$$I_{CEO} = (\beta + 1) I_{CBO} \tag{3.3}$$

The constant $\alpha < 1$ is a measure of the proportion of majority carriers (holes for *pnp* devices, electrons for *npn*) injected into the base region from the emitter that are received by the collector. Equation (*3.2*) is the dc current amplification characteristic of the BJT: Except for the leakage current, the base current is increased or amplified β times to become the collector current. Under dc conditions KCL gives

$$I_E = I_C + I_B \tag{3.4}$$

which, in conjunction with (*3.1*) through (*3.3*), completely describes the dc current relationships of the BJT in the active mode.

Example 3.5. Determine α and β for the transistor of Example 3.1 if leakage currents (flow due to holes) are negligible and the described charge flow is constant.

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If we assume $I_{CBO} = I_{CEO} = 0$, then

$$\alpha = \frac{i_C}{i_E} = \frac{i_E - i_B}{i_E} = \frac{1.602 - 0.016}{1.602} = 0.99$$

and

$$\beta = \frac{i_C}{i_B} = \frac{i_E - i_B}{i_B} = \frac{1.602 - 0.016}{0.016} = 99.125$$

Example 3.6. A BJT has $\alpha = 0.99$, $i_B = I_B = 25\,\mu\text{A}$, and $I_{CBO} = 200\,\text{nA}$. Find (*a*) the dc collector current, (*b*) the dc emitter current, and (*c*) the percentage error in emitter current when leakage current is neglected.

(*a*) With $\alpha = 0.99$, (*3.2*) gives

$$\beta = \frac{\alpha}{1 - \alpha} = 99$$

Using (*3.3*) in (*3.2*) then gives

$$I_C = \beta I_B + (\beta + 1) I_{CBO} = 99(25 \times 10^{-6}) + (99 + 1)(200 \times 10^{-9}) = 2.495\,\text{mA}$$

(*b*) The dc emitter current follows from (*3.1*):

$$I_E = \frac{I_C - I_{CBO}}{\alpha} = \frac{2.495 \times 10^{-3} - 200 \times 10^{-9}}{0.99} = 2.518\,\text{mA}$$

(*c*) Neglecting the leakage current, we have

$$I_C = \beta I_B = 99(25 \times 10^{-6}) = 2.475\,\text{mA} \qquad \text{so} \qquad I_E = \frac{I_C}{\alpha} = \frac{2.475}{0.99} = 2.5\,\text{mA}$$

giving an emitter-current error of

$$\frac{2.518 - 2.5}{2.518}(100\%) = 0.71\%$$

3.6. BIAS AND DC LOAD LINES

Supply voltages and resistors *bias* a transistor; that is, they establish a specific set of dc terminal voltages and currents, thus determining a point of active-mode operation (called the *quiescent point* or *Q point*). Usually, quiescent values are unchanged by the application of an ac signal to the circuit.

With the universal bias arrangement of Fig. 3-8(*a*), only one dc power supply (V_{CC}) is needed to establish active-mode operation. Use of the Thévenin equivalent of the circuit to the left of *a*, *b* leads to the circuit of Fig. 3-8(*b*), where

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \qquad V_{BB} = \frac{R_1}{R_1 + R_2} V_{CC} \tag{3.5}$$

If we neglect leakage current so that $I_{EQ} = (\beta + 1) I_{BQ}$ and assume the emitter-to-base voltage V_{BEQ} is constant ($\approx 0.7\,\text{V}$ and $\approx 0.3\,\text{V}$ for Si and Ge, respectively), then KVL around the emitter loop of Fig. 3-8(*b*) yields

$$V_{BB} = \frac{I_{EQ}}{\beta + 1} R_B + V_{BEQ} + I_{EQ} R_E \tag{3.6}$$

which can be represented by the emitter-loop equivalent bias circuit of Fig. 3-8(*c*). Solving (*3.6*) for I_{EQ} and noting that

$$I_{EQ} = \frac{I_{CQ}}{\alpha} \approx I_{CQ}$$

we obtain

$$I_{CQ} \approx I_{EQ} = \frac{V_{BB} - V_{BEQ}}{R_B/(\beta + 1) + R_E} \tag{3.7}$$

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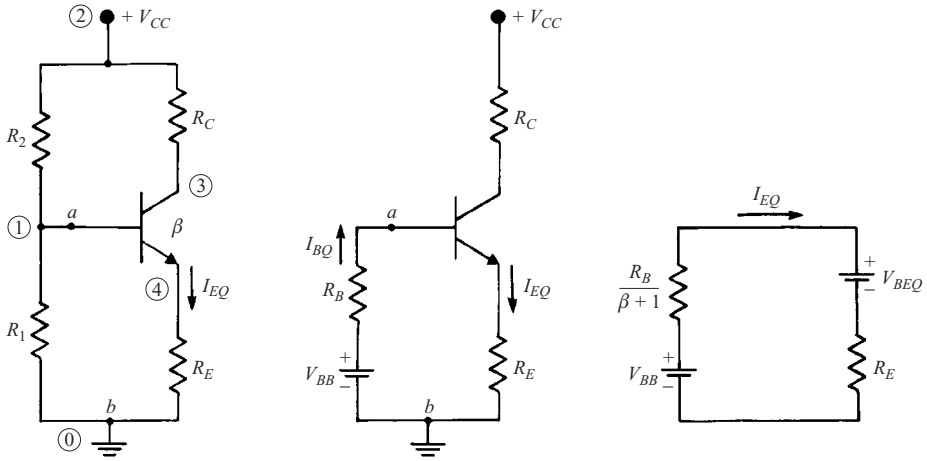


Fig. 3-8

If component values and the worst-case β value are such that

$$\frac{R_B}{\beta+1} \approx \frac{R_B}{\beta} \ll R_E \tag{3.8}$$

then I_{EQ} (and thus I_{CQ}) is nearly constant, regardless of changes in β; the circuit then has *β-independent* bias.

From Fig. 3-3(*c*) it is apparent that the family of collector characteristics is described by the mathematical relationship $i_C = f(v_{CE}, i_B)$ with independent variable v_{CE} and the parameter i_B. We assume that the collector circuit can be biased so as to place the Q point anywhere in the active region. A typical setup is shown in Fig. 3-9(*a*), from which

$$I_{CQ} = -\frac{V_{CEQ}}{R_{\text{dc}}} + \frac{V_{CC}}{R_{\text{dc}}}$$

Thus, if the *dc load line*,

$$i_C = -\frac{v_{CE}}{R_{\text{dc}}} + \frac{V_{CC}}{R_{\text{dc}}} \tag{3.9}$$

and the specification

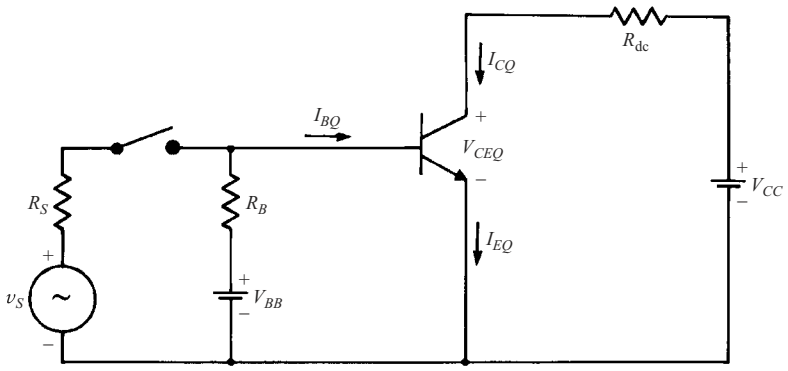
$$i_B = I_{BQ} \tag{3.10}$$

are combined with the relationship for the collector characteristics, the resulting system can be solved (analytically or graphically) for the collector quiescent quantities I_{CQ} and V_{CEQ}.

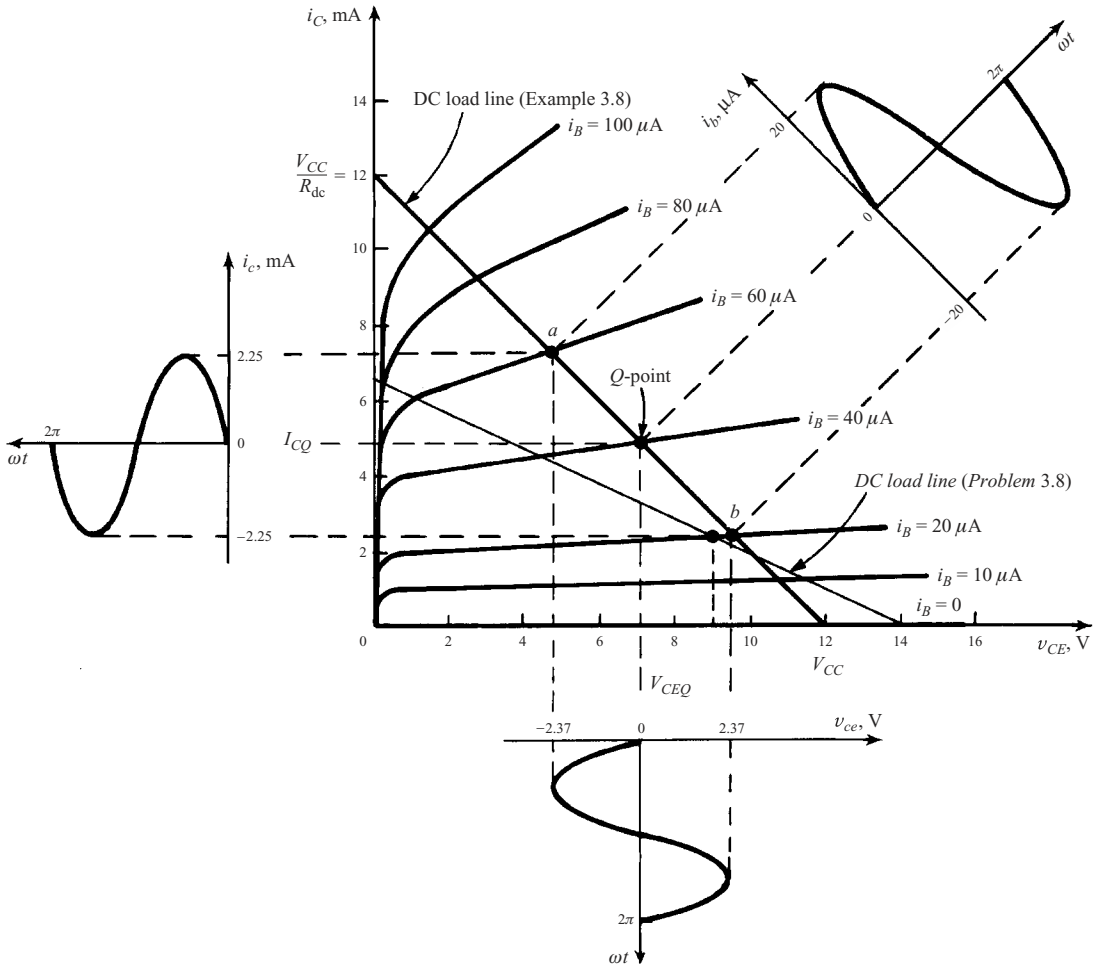
Example 3.7. For the transistor circuit of Fig. 3-8(*a*), $R_1 = 1\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, $R_C = 3\,\text{k}\Omega$, $R_E = 10\,\Omega$, and $V_{CC} = 15\,\text{V}$. If the transistor is the generic *npn* transistor of Example 3.3, use SPICE methods to determine the quiescent values I_{BQ}, V_{BEQ}, I_{CQ}, and V_{CEQ}.

The netlist code below models the circuit.

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(*a*)



(*b*)

Fig. 3-9

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```
EX3_7.CIR - CE quiescent values
R1  0 1 1kohm
R2  2 1 20kohm
RC  2 3 3kohm
RE  4 0 10ohm
VCC 2 0 15V
Q 3  1 4 QNPNG
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=30V Cjc=10pF Cje=15pF)
.DC VCC 15V 15V 1V
.PRINT DC IB(Q) IC(Q) V(1,4) V(3,4)
.END
```

Execute ⟨Ex3_7.CIR⟩ and poll the output file to find

```
   VCC       IB(Q)       IC(Q)      V(1,4)      V(3,4)
1.500E+01 1.428E-05 2.575E-03 6.748E-01 7.252E+00
```

where $I_{BQ} = \text{IB(Q)}$, $I_{CQ} = \text{IC(Q)}$, $V_{BEQ} = \text{V(1, 4)}$, and $V_{CEQ} = \text{V(3, 4)}$.

Example 3.8. The signal source switch of Fig. 3-9(*a*) is closed, and the transistor base current becomes

$$i_B = I_{BQ} + i_b = 40 + 20 \sin \omega t \quad \mu\text{A}$$

The collector characteristics of the transistor are those displayed in Fig. 3-9(*b*). If $V_{CC} = 12\,\text{V}$ and $R_{\text{dc}} = 1\,\text{k}\Omega$, graphically determine (*a*) I_{CQ} and V_{CEQ}, (*b*) i_c and v_{ce}, and (*c*) $h_{FE}(= \beta)$ at the Q point.

(*a*) The dc load line has ordinate intercept $V_{CC}/R_{\text{dc}} = 12\,\text{mA}$ and abscissa intercept $V_{CC} = 12\,\text{V}$ and is constructed on Fig. 3-9(*b*). The Q point is the intersection of the load line with the characteristic curve $i_B = I_{BQ} = 40\,\mu\text{A}$. The collector quiescent quantities may be read from the axes as $I_{CQ} = 4.9\,\text{mA}$ and $V_{CEQ} = 7.2\,\text{V}$.

(*b*) A time scale is constructed perpendicular to the load line at the Q point, and a scaled sketch of $i_b = 20 \sin \omega t\,\mu\text{A}$ is drawn [see Fig. 3-9(*b*)] and translated through the load line to sketches of i_c and v_{ce}. As i_b swings $\pm 20\,\mu\text{A}$ along the load line from points a to b, the ac components of collector current and voltage take on the values

$$i_c = 2.25 \sin \omega t \quad \text{mA} \qquad \text{and} \qquad v_{ce} = -2.37 \sin \omega t \quad \text{V}$$

The negative sign on v_{ce} signifies a 180° phase shift.

(*c*) From (*3.2*) with $I_{CEO} = 0$ [the $i_B = 0$ curve coincides with the v_{CE} axis in Fig. 3-9(*b*)],

$$h_{FE} = \frac{I_{CQ}}{I_{BQ}} = \frac{4.9 \times 10^{-3}}{40 \times 10^{-6}} = 122.5$$

It is clear that amplifiers can be biased for operation at any point along the dc load line. Table 3-4 shows the various classes of amplifiers, based on the percentage of the signal cycle over which they operate in the linear or active region.

Table 3-4

Class	Percentage of Active-Region Signal Excursion
A	100
AB	between 50 and 100
B	50
C	less than 50

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3.7. CAPACITORS AND AC LOAD LINES

Two common uses of capacitors (sized to appear as short circuits to signal frequencies) are illustrated by the circuit of Fig. 3-10(*a*).

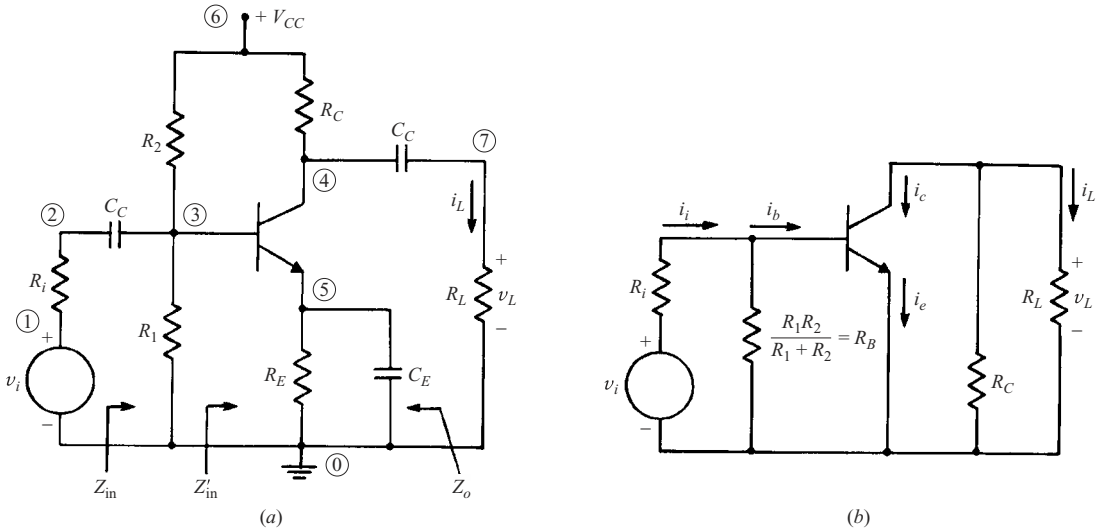


Fig. 3-10

1. Coupling capacitors (C_C) confine dc quantities to the transistor and its bias circuitry.
2. Bypass capacitors (C_E) effectively remove the gain-reducing emitter resistor R_E insofar as ac signals are concerned, while allowing R_E to play its role in establishing β-independent bias (Section 3.6).

The capacitors of Fig. 3-10(*a*) are shorted in the circuit as it appears to ac signals [Fig. 3-10(*b*)]. In Fig. 3-10(*a*), we note that the collector-circuit resistance seen by the dc bias current $I_{CQ}(\approx I_{EQ})$ is $R_{dc} = R_C + R_E$. However, from Fig. 3-10(*b*) it is apparent that the collector signal current i_c sees a collector-circuit resistance $R_{ac} = R_C R_L/(R_C + R_L)$. Since $R_{ac} \neq R_{dc}$ in general, the concept of an *ac load line* arises. By application of KVL to Fig. 3-10(*b*), the *v-i* characteristic of the external signal circuitry is found to be

$$v_{ce} = i_c R_{ac} \tag{3.11}$$

Since $i_c = i_C - I_{CQ}$ and $v_{ce} = v_{CE} - V_{CEQ}$, (*3.11*) can be written analogously to (*3.9*) as

$$i_C = -\frac{v_{CE}}{R_{ac}} + \frac{V_{CEQ}}{R_{ac}} + I_{CQ} \tag{3.12}$$

All excursions of the ac signals i_c and v_{ce} are represented by points on the ac load line, (*3.12*). If the value $i_C = I_{CQ}$ is substituted into (*3.12*), we find that $v_{CE} = V_{CEQ}$; thus, the ac load line intersects the dc load line at the Q point.

Example 3.9. Find the points at which the ac load line intersects the axes of the collector characteristic.

The i_C intercept ($i_{C\,max}$) is found by setting $v_{CE} = 0$ in (*3.12*):

$$i_{C\,max} = \frac{V_{CEQ}}{R_{ac}} + I_{CQ} \tag{3.13}$$

The v_{CE} intercept is found by setting $i_C = 0$ in (*3.12*):

$$v_{CE\,max} = V_{CEQ} + I_{CQ} R_{ac} \tag{3.14}$$

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Solved Problems

3.1 For a certain BJT, $\beta = 50$, $I_{CEO} = 3\,\mu A$, and $I_C = 1.2\,mA$. Find I_B and I_E.

By (*3.2*),

$$I_B = \frac{I_C - I_{CEO}}{\beta} = \frac{1.2 \times 10^{-3} - 3 \times 10^{-6}}{50} = 23.94\,\mu A$$

And, directly from (*3.4*),

$$I_E = I_C + I_B = 1.2 \times 10^{-3} - 23.94 \times 10^{-6} = 1.224\,mA$$

3.2 A Ge transistor with $\beta = 100$ has a base-to-collector leakage current I_{CBO} of $5\,\mu A$. If the transistor is connected for common-emitter operation, find the collector current for (*a*) $I_B = 0$ and (*b*) $I_B = 40\,\mu A$.

(*a*) With $I_B = 0$, only emitter-to-collector leakage flows, and, by (*3.3*),

$$I_{CEO} = (\beta + 1)I_{CBO} = (100 + 1)(5 \times 10^{-6}) = 505\,\mu A$$

(*b*) If we substitute (*3.3*) into (*3.2*) and solve for I_C, we get

$$I_C = \beta I_B + (\beta + 1)I_{CBO} = (100)(40 \times 10^{-6}) + (101)(5 \times 10^{-6}) = 4.505\,mA$$

3.3 A transistor with $\alpha = 0.98$ and $I_{CBO} = 5\,\mu A$ is biased so that $I_{BQ} = 100\,\mu A$. Find I_{CQ} and I_{EQ}.

By (*3.2*) and (*3.3*),

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = 49$$

so that

$$I_{CEO} = (\beta + 1)I_{CBO} = (49 + 1)(5 \times 10^{-6}) = 0.25\,mA$$

And, from (*3.2*) and (*3.4*),

$$I_{CQ} = \beta I_{BQ} + I_{CEO} = (49)(100 \times 10^{-6}) + 0.25 \times 10^{-3} = 5.15\,mA$$
$$I_{EQ} = I_{CQ} + I_{BQ} = 5.15 \times 10^{-3} + 100 \times 10^{-6} = 5.25\,mA$$

3.4 The transistor of Fig. 3-11 has $\alpha = 0.98$ and a base current of $30\,\mu A$. Find (*a*) β, (*b*) I_{CQ}, and (*c*) I_{EQ}. Assume negligible leakage current.

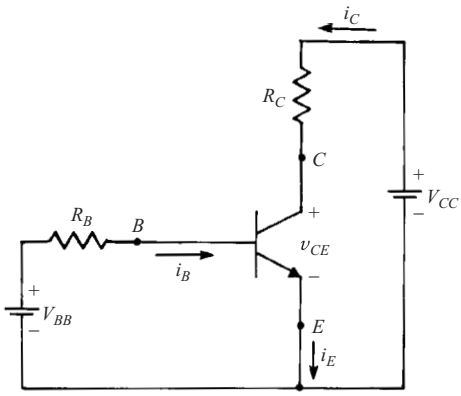


Fig. 3-11

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(*a*) $$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

(*b*) From (*3.2*) with $I_{CEO} = 0$, we have $I_{CQ} = \beta I_{BQ} = (49)(30 \times 10^{-6}) = 1.47\,\text{mA}$.

(*c*) From (*3.1*) with $I_{CBO} = 0$,

$$I_{EQ} = \frac{I_{CQ}}{\alpha} = \frac{1.47}{0.98} = 1.50\,\text{mA}$$

3.5 The transistor circuit of Fig. 3-11 is to be operated with a base current of $40\,\mu\text{A}$ and $V_{BB} = 6\,\text{V}$. The Si transistor ($V_{BEQ} = 0.7\,\text{V}$) has negligible leakage current. Find the required value of R_B.

By KVL around the base-emitter loop,

$$V_{BB} = I_{BQ}R_B + V_{BEQ} \qquad \text{so that} \qquad R_B = \frac{V_{BB} - V_{BEQ}}{I_{BQ}} = \frac{6 - 0.7}{40 \times 10^{-6}} = 132.5\,\text{k}\Omega$$

3.6 In the circuit of Fig. 3-11, $\beta = 100$, $I_{BQ} = 20\,\mu\text{A}$, $V_{CC} = 15\,\text{V}$, and $R_C = 3\,\text{k}\Omega$. If $I_{CBO} = 0$, find (*a*) I_{EQ} and (*b*) V_{CEQ}. (*c*) Find V_{CEQ} if R_C is changed to $6\,\text{k}\Omega$ and all else remains the same.

(*a*) $$\alpha = \frac{\beta}{\beta+1} = \frac{100}{101} = 0.9901$$

Now, using (*3.2*) and (*3.1*) with $I_{CBO} = I_{CEO} = 0$, we get

$$I_{CQ} = \beta I_{BQ} = (100)(20 \times 10^{-6}) = 2\,\text{mA}$$

and $$I_{EQ} = \frac{I_{CQ}}{\alpha} = \frac{2 \times 10^{-3}}{0.9901} = 2.02\,\text{mA}$$

(*b*) From an application of KVL around the collector circuit,

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 15 - (2)(3) = 9\,\text{V}$$

(*c*) If I_{BQ} is unchanged, then I_{CQ} is unchanged. The solution proceeds as in part *b*:

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 15 - (2)(6) = 3\,\text{V}$$

3.7 The transistor of Fig. 3-12 is a Si device with a base current of $40\,\mu\text{A}$ and $I_{CBO} = 0$. If $V_{BB} = 6\,\text{V}$, $R_E = 1\,\text{k}\Omega$, and $\beta = 80$, find (*a*) I_{EQ} and (*b*) R_B. (*c*) If $V_{CC} = 15\,\text{V}$ and $R_C = 3\,\text{k}\Omega$, find V_{CEQ}.

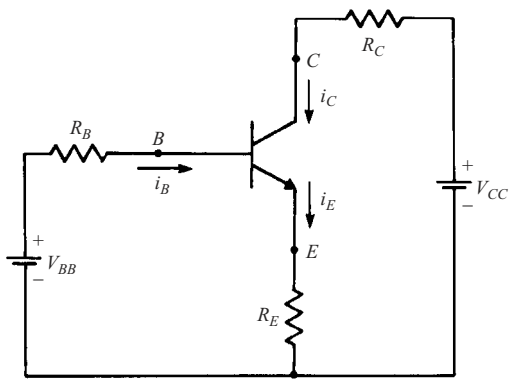


Fig. 3-12

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(*a*) $$\alpha = \frac{\beta}{\beta + 1} = \frac{80}{81} = 0.9876$$

Then combining (*3.1*) and (*3.2*) with $I_{CBO} = I_{CEO} = 0$ gives

$$I_{EQ} = \frac{I_{BQ}}{1 - \alpha} = \frac{40 \times 10^{-6}}{1 - 0.9876} = 3.226\,\text{mA}$$

(*b*) Applying KVL around the base-emitter loop gives

$$V_{BB} = I_{BQ}R_B + V_{BEQ} + I_{EQ}R_E$$

or (with V_{BEQ} equal to the usual 0.7 V for a Si device)

$$R_B = \frac{V_{BB} - V_{BEQ} - I_{EQ}R_E}{I_{BQ}} = \frac{6 - 0.7 - (3.226)(1)}{40 \times 10^{-6}} = 51.85\,\text{k}\Omega$$

(*c*) From (*3.2*) with $I_{CEO} = 0$,

$$I_{CQ} = \beta I_{BQ} = (80)(40 \times 10^{-6}) = 3.2\,\text{mA}$$

Then, by KVL around the collector circuit,

$$V_{CEQ} = V_{CC} - I_{EQ}R_E - I_{CQ}R_C = 15 - (3.226)(1) - (3.2)(3) = 2.174\,\text{V}$$

3.8 Assume that the CE collector characteristics of Fig. 3-9(*b*) apply to the transistor of Fig. 3-11. If $I_{BQ} = 20\,\mu\text{A}$, $V_{CEQ} = 9\,\text{V}$, and $V_{CC} = 14\,\text{V}$, find graphically (*a*) I_{CQ}, (*b*) R_C, (*c*) I_{EQ}, and (*d*) β if leakage current is negligible.

(*a*) The Q point is the intersection of $i_B = I_{BQ} = 20\,\mu\text{A}$ and $v_{CE} = V_{CEQ} = 9\,\text{V}$. The dc load line must pass through the Q point and intersect the v_{CE} axis at $V_{CC} = 14\,\text{V}$. Thus, the dc load line can be drawn on Fig. 3-9(*b*), and $I_{CQ} = 2.25\,\text{mA}$ can be read as the i_C coordinate of the Q point.

(*b*) The i_C intercept of the dc load line is $V_{CC}/R_{\text{dc}} = V_{CC}/R_C$, which, from Fig. 3-9(*b*), has the value 6.5 mA; thus,

$$R_C = \frac{V_{CC}}{6.5 \times 10^{-3}} = \frac{14}{6.5 \times 10^{-3}} = 2.15\,\text{k}\Omega$$

(*c*) By (*3.4*), $I_{EQ} = I_{CQ} + I_{BQ} = 2.25 \times 10^{-3} + 20 \times 10^{-6} = 2.27\,\text{mA}$.

(*d*) With $I_{CEO} = 0$, (*3.2*) yields

$$\beta = \frac{I_{CQ}}{I_{BQ}} = \frac{2.25 \times 10^{-3}}{20 \times 10^{-6}} = 112.5$$

3.9 In the *pnp* Si transistor circuit of Fig. 3-13, $R_B = 500\,\text{k}\Omega$, $R_C = 2\,\text{k}\Omega$, $R_E = 0$, $V_{CC} = 15\,\text{V}$, $I_{CBO} = 20\,\mu\text{A}$, and $\beta = 70$. Find the Q-point collector current I_{CQ}.

By (*3.3*), $I_{CEO} = (\beta + 1)I_{CBO} = (70 + 1)(20 \times 10^{-6}) = 1.42\,\text{mA}$. Now, application of the KVL around the loop that includes V_{CC}, R_B, $R_E(= 0)$, and ground

$$V_{CC} = V_{BEQ} + I_{BQ}R_B \qquad \text{so that} \qquad I_{BQ} = \frac{V_{CC} - V_{BEQ}}{R_B} = \frac{15 - 0.7}{500 \times 10^3} = 28.6\,\mu\text{A}$$

Thus, by (*3.2*),

$$I_{CQ} = \beta I_{BQ} + I_{CEO} = (70)(28.6 \times 10^{-6}) + 1.42 \times 10^{-3} = 3.42\,\text{mA}$$

3.10 The Si transistor of Fig. 3-14 is biased for constant base current. If $\beta = 80$, $V_{CEQ} = 8\,\text{V}$, $R_C = 3\,\text{k}\Omega$, and $V_{CC} = 15\,\text{V}$, find (*a*) I_{CQ} and (*b*) the required value of R_B. (*c*) Find R_B if the transistor is a Ge device.

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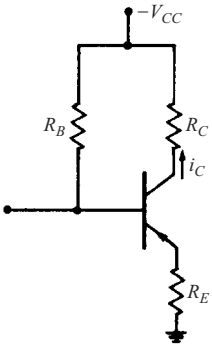


Fig. 3-13

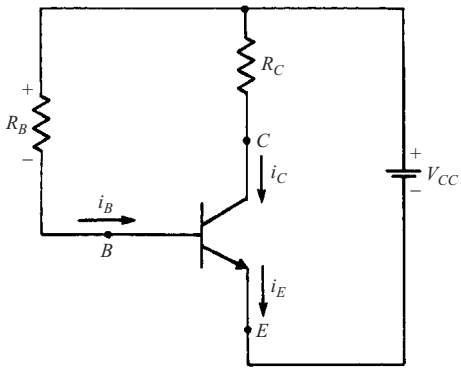


Fig. 3-14

(*a*) By KVL around the collector-emitter circuit,

$$I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_c} = \frac{15 - 8}{3 \times 10^3} = 2.333\,\text{mA}$$

(*b*) If leakage current is neglected, (*3.2*) gives

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{2.333 \times 10^{-3}}{80} = 29.16\,\mu\text{A}$$

Since the transistor is a Si device, $V_{BEQ} = 0.7\,\text{V}$ and, by KVL around the outer loop,

$$R_B = \frac{V_{CC} - V_{BEQ}}{I_{BQ}} = \frac{15 - 0.7}{29.16 \times 10^{-6}} = 490.4\,\text{k}\Omega$$

(*c*) The only difference here is that $V_{BEQ} = 0.3\,\text{V}$; thus

$$R_B = \frac{15 - 0.3}{29.16 \times 10^{-6}} = 504.1\,\text{k}\Omega$$

3.11 The Si transistor of Fig. 3-15 has $\alpha = 0.99$ and $I_{CEO} = 0$. Also, $V_{EE} = 4\,\text{V}$ and $V_{CC} = 12\,\text{V}$. (*a*) If $I_{EQ} = 1.1\,\text{mA}$, find R_E. (*b*) If $V_{CEQ} = -7\,\text{V}$, find R_C.

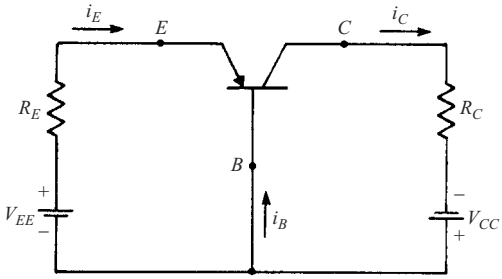


Fig. 3-15

(*a*) By KVL around the emitter-base loop,

$$R_E = \frac{V_{EE} + V_{BEQ}}{I_{EQ}} = \frac{4 + (-0.7)}{1.1 \times 10^{-3}} = 3\,\Omega$$

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(*b*) By KVL around the transistor terminals (which constitute a closed path),

$$V_{CBQ} = V_{CEQ} - V_{BEQ} = -7 - (-0.7) = -6.3\,\text{V}$$

With negligible leakage current, (*3.1*) gives

$$I_{CQ} = \alpha I_{EQ} = (0.99)(1.1 \times 10^{-3}) = 1.089\,\text{mA}$$

Finally, by KVL around the base-collector loop,

$$R_C = \frac{V_{CC} + V_{CBQ}}{I_{CQ}} = \frac{12 - 6.3}{1.089 \times 10^{-3}} = 5.234\,\text{k}\Omega$$

3.12 Collector characteristics for the Ge transistor of Fig. 3-15 are given in Fig. 3-16. If $V_{EE} = 2\,\text{V}$, $V_{CC} = 12\,\text{V}$, and $R_C = 2\,\text{k}\Omega$, size R_E so that $V_{CEQ} = -6.4\,\text{V}$.

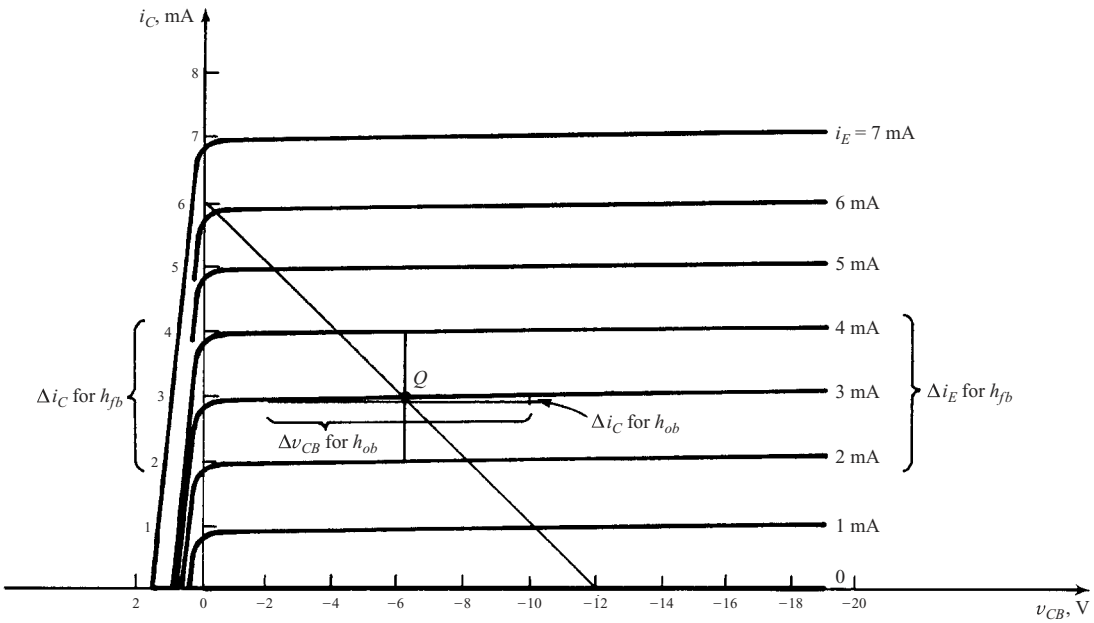


Fig. 3-16

We construct, on Fig. 3-16, a dc load line having v_{CB} intercept $-V_{CC} = -12\,\text{V}$ and i_C intercept $V_{CC}/R_C = 6\,\text{mA}$. The abscissa of the Q point is given by KVL around the transistor terminals:

$$V_{CBQ} = V_{CEQ} - V_{BEQ} = -6.4 - (-0.3) = -6.1\,\text{V}$$

With the Q point defined, we read $I_{EQ} = 3\,\text{mA}$ from the graph. Now KVL around the emitter-base loop leads to

$$R_E = \frac{V_{EE} + V_{BEQ}}{I_{EQ}} = \frac{2 + (-0.3)}{3 \times 10^{-3}} = 566.7\,\Omega$$

3.13 The circuit of Fig. 3-17 uses current- (or shunt-) feedback bias. The Si transistor has $I_{CEO} \approx 0$, $V_{CE\text{sat}} \approx 0$, and $h_{FE} = 100$. If $R_C = 2\,\text{k}\Omega$ and $V_{CC} = 12\,\text{V}$, size R_F for ideal *maximum symmetrical swing* (that is, location of the quiescent point such that $V_{CEQ} = V_{CC}/2$).

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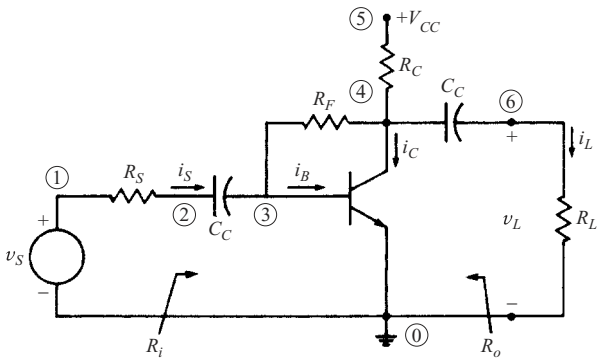


Fig. 3-17

Application of KVL to the collector-emitter bias circuit gives

$$(I_{BQ} + I_{CQ})R_C = V_{CC} - V_{CEQ}$$

With $I_{CQ} = h_{FE}I_{BQ}$, this leads to

$$I_{BQ} = \frac{V_{CC} - V_{CEQ}}{(h_{FE} + 1)R_C} = \frac{12 - 6}{(100 + 1)(2 \times 10^3)} = 29.7\,\mu\text{A}$$

Then, by KVL around the transistor terminals,

$$R_F = \frac{V_{CEQ} - V_{BEQ}}{I_{BQ}} = \frac{6 - 0.7}{29.7 \times 10^{-6}} = 178.5\,\text{k}\Omega$$

3.14 For the amplifier of Fig. 3-17, $C_C = 100\,\mu\text{F}$, $R_F = 180\,\text{k}\Omega$, $R_L = 2\,\text{k}\Omega$, $R_S = 100\,\text{k}\Omega$, $V_{CC} = 12\,\text{V}$, and $v_S = 4\sin(20 \times 10^3\pi t)\,\text{V}$. The transistor is described by the default *npn* model of Example 3.2. Use SPICE methods to (*a*) determine the quiescent values ($I_{BQ}, I_{CQ}, V_{BEQ}, V_{CEQ}$) and (*b*) plot the input and output currents and voltages (v_S, i_S, v_L, i_L).

(*a*) The netlist code that follows models the circuit:

```
Prb3_14.CIR - CE amplifier
vS  1 0 SIN(0V 4V 10kHz)
RS  1 2 100kohm
CC1 2 3 100uF
Q  4 3 0 QNPN
RF  3 4 180kohm
RC  4 5 2kohm
VCC 5 0 12V
CC2 4 6 100uF
RL  6 0 2kohm
.MODEL QNPN NPN() ; Default transistor
.DC VCC 12V 12V 1V
.PRINT DC IB(Q) IC(Q) V(3) V(4)
.TRAN 1us 0.1ms  ; Signal values
.PROBE
.END
```

Execute ⟨Prb3_14.CIR⟩ and poll the output file to find $I_{BQ} = \text{IB(Q)} = 29.3\,\mu\text{A}$, $I_{CQ} = \text{IC(Q)} = 2.93\,\text{mA}$, $V_{BEQ} = \text{V(3)} = 0.80\,\text{V}$, and $V_{CEQ} = \text{V(4)} = 6.08\,\text{V}$. Since $V_{CEQ} \simeq V_{CC}/2$, the transistor is biased for maximum symmetrical swing.

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(*b*) The Probe feature of PSpice is used to plot i_S, i_L, v_S, and v_L as displayed by Fig. 3-18. Notice the 180° phase shift between input and output quantities.

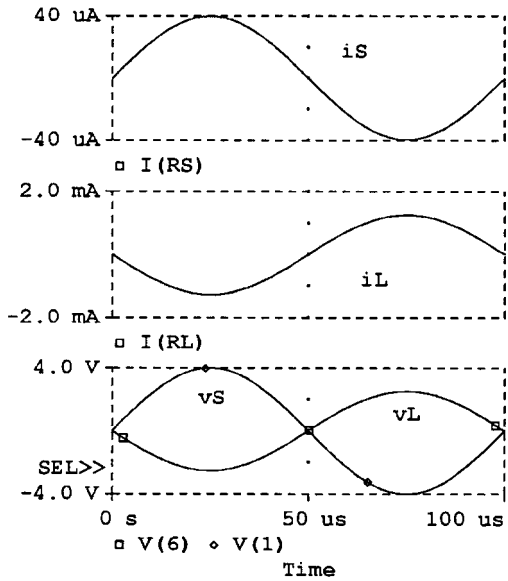


Fig. 3-18

3.15 Find the value of the emitter resistor R_E that, when added to the Si transistor circuit of Fig. 3-17, would bias for operation about $V_{CEQ} = 5\,\text{V}$. Let $I_{CEO} = 0$, $\beta = 80$, $R_F = 220\,\text{k}\Omega$, $R_C = 2\,\text{k}\Omega$, and $V_{CC} = 12\,\text{V}$.

Application of KVL around the transistor terminals yields

$$I_{BQ} = \frac{V_{CEQ} - V_{BEQ}}{R_F} = \frac{5 - 0.7}{220 \times 10^3} = 19.545\,\mu\text{A}$$

Since leakage current is zero, (*3.1*) and (*3.2*) give $I_{EQ} = (\beta + 1)I_{CQ}$; thus KVL around the collector circuit gives

$$(I_{BQ} + \beta I_{BQ})R_C + (\beta + 1)I_{BQ}R_E = V_{CC} - V_{CEQ}$$

so $$R_E = \frac{V_{CC} - V_{CEQ} - (\beta + 1)I_{BQ}R_C}{(\beta + 1)I_{BQ}} = \frac{12 - 5 - (80 + 1)(19.545 \times 10^{-6})(2 \times 10^3)}{(80 + 1)(19.545 \times 10^{-6})} = 2.42\,\text{k}\Omega$$

3.16 In the circuit of Fig. 3-12, $I_{BQ} = 30\,\mu\text{A}$, $R_E = 1\,\text{k}\Omega$, $V_{CC} = 15\,\text{V}$, and $\beta = 80$. Find the minimum value of R_C that will maintain the transistor quiescent point at saturation, if $V_{CE\text{sat}} = 0.2\,\text{V}$, β is constant, and leakage current is negligible.

We first find

$$\alpha = \frac{\beta}{\beta + 1} = \frac{80}{81} = 0.9876$$

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Then the use of (*3.2*) and (*3.1*) with negligible leakage current yields

$$I_{CQ} = \beta I_{BQ} = (80)(30 \times 10^{-6}) = 2.4\,\text{mA}$$

and

$$I_{EQ} = \frac{I_{CQ}}{\alpha} = \frac{2.4 \times 10^{-3}}{0.9876} = 2.43\,\text{mA}$$

Now KVL around the collector circuit leads to the minimum value of R_C to ensure saturation:

$$R_C = \frac{V_{CC} - V_{CE\text{sat}} - I_{EQ}R_E}{I_{CQ}} = \frac{15 - 0.2 - (2.43)(1)}{2.4 \times 10^{-3}} = 5.154\,\text{k}\Omega$$

3.17 The Si transistor of Fig. 3-19 has $\beta = 50$ and negligible leakage current. Let $V_{CC} = 18\,\text{V}$, $V_{EE} = 4\,\text{V}$, $R_E = 200\,\Omega$, and $R_C = 4\,\text{k}\Omega$. (*a*) Find R_B so that $I_{CQ} = 2\,\text{mA}$. (*b*) Determine the value of V_{CEQ} for V_B of part (*a*).

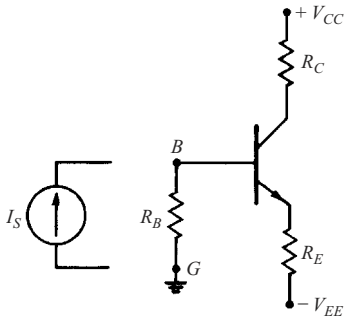


Fig. 3-19

(*a*) KVL around the base-emitter-ground loop gives

$$V_{EE} = I_{BQ}R_B + V_{BEQ} + I_{EQ}R_E \tag{1}$$

Also, from (*3.1*) and (*3.2*),

$$I_{EQ} = \frac{\beta + 1}{\beta} I_{CQ} \tag{2}$$

Now, using (*3.2*) and (*2*) in (*1*) and solving for R_B yields

$$R_B = \frac{\beta(V_{EE} - V_{BEQ})}{I_{CQ}} - (\beta + 1)R_E = \frac{50(4 - 0.7)}{2 \times 10^{-3}} - (50 + 1)(200) = 72.3\,\text{k}\Omega$$

(*b*) KVL around the collector-emitter-ground loop gives

$$V_{CEQ} = V_{CC} + V_{EE} - \left(R_C + \frac{\beta + 1}{\beta} R_E\right) I_{CQ}$$

$$= 18 + 4 - \left(4 \times 10^3 + \frac{50 + 1}{50} 200\right)(2 \times 10^{-3}) = 13.59\,\text{V}$$

3.18 The dc current source $I_S = 10\,\mu\text{A}$ of Fig. 3-19 is connected from G to node B. The Si transistor has negligible leakage current and $\beta = 50$. If $R_B = 75\,\text{k}\Omega$, $R_E = 200\,\Omega$, and $R_C = 4\,\text{k}\Omega$, find the dc current-gain ratio I_{CQ}/I_S for (*a*) $V_{CC} = 18\,\text{V}$ and $V_{EE} = 4\,\text{V}$, and (*b*) $V_{CC} = 22\,\text{V}$ and $V_{EE} = 0\,\text{V}$.

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(*a*) A Thévenin equivalent for the network to the left of terminals B, G has $V_{Th} = R_B I_S$ and $R_{Th} = R_B$. With the Thévenin equivalent circuit in place, KVL around the base-emitter loop yields

$$R_B I_S + V_{EE} = I_{BQ} R_B + V_{BEQ} + I_{EQ} R_E \tag{1}$$

Using (*3.2*) and (*2*) of Problem 3.17 in (*1*), solving for I_{CQ}, and then dividing by I_S results in the desired ratio:

$$\frac{I_{CQ}}{I_S} = \frac{R_B I_S + V_{EE} - V_{BEQ}}{I_S\left(\dfrac{R_B}{\beta} + \dfrac{\beta+1}{\beta} R_E\right)} = \frac{(75 \times 10^3)(10 \times 10^{-6}) + 4 - 0.7}{(10 \times 10^{-6})\left(\dfrac{75 \times 10^3}{50} + \dfrac{50+1}{50} 200\right)} = 237.67 \tag{2}$$

Note that the value of V_{CC} must be large enough so that cutoff does not occur, but otherwise it does not affect the value of I_{CQ}.

(*b*) $V_{EE} = 0$ in (*2*) directly gives

$$\frac{I_{CQ}}{I_S} = \frac{(75 \times 10^3)(10 \times 10^{-6}) - 0.7}{(10 \times 10^{-6})\left(\dfrac{75 \times 10^3}{50} + \dfrac{50+1}{50} 200\right)} = 2.93$$

Obviously, V_{EE} strongly controls the dc current gain of this amplifier.

3.19 In the circuit of Fig. 3-20, $V_{CC} = 12\,\text{V}$, $V_S = 2\,\text{V}$, $R_C = 4\,\text{k}\Omega$, and $R_S = 100\,\text{k}\Omega$. The Ge transistor is characterized by $\beta = 50$, $I_{CEO} = 0$, and $V_{CE\text{sat}} = 0.2\,\text{V}$. Find the value of R_B that just results in saturation if (*a*) the capacitor is present, and (*b*) the capacitor is replaced with a short circuit.

(*a*) Application of KVL around the collector loop gives the collector current at the onset of saturation as

$$I_{CQ} = \frac{V_{CC} - V_{CE\text{sat}}}{R_C} = \frac{12 - 0.2}{4 \times 10^3} = 2.95\,\text{mA}$$

With C blocking, $I_S = 0$; hence the use of KVL leads to

$$R_B = \frac{V_{CC} - V_{BEQ}}{I_{BQ}} = \frac{V_{CC} - V_{BEQ}}{I_{CQ}/\beta} = \frac{12 - 0.3}{(2.95 \times 10^{-3})/50} = 198.3\,\text{k}\Omega$$

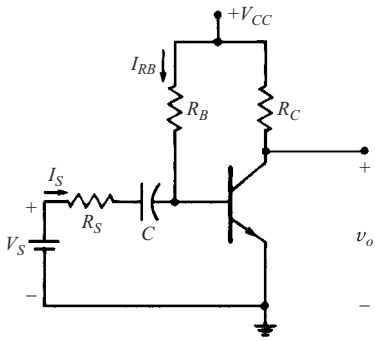


Fig. 3-20

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(b) With C shorted, the application of (3.2), KCL, and KVL results in

$$I_{BQ} = \frac{I_{CQ}}{\beta} = I_S + I_{RB} = \frac{V_S - V_{BEQ}}{R_S} + \frac{V_{CC} - V_{BEQ}}{R_B}$$

so that

$$R_B = \frac{V_{CC} - V_{BEQ}}{\dfrac{I_{CQ}}{\beta} - \dfrac{V_S - V_{BEQ}}{R_S}} = \frac{12 - 0.3}{\dfrac{2.95 \times 10^{-3}}{50} - \dfrac{2 - 0.3}{100 \times 10^3}} = 278.6\,\text{k}\Omega$$

3.20 The Si *Darlington transistor pair* of Fig. 3-21 has negligible leakage current, and $\beta_1 = \beta_2 = 50$. Let $V_{CC} = 12\,\text{V}$, $R_E = 1\,\text{k}\Omega$, and $R_2 \to \infty$. (a) Find the value of R_1 needed to bias the circuit so that $V_{CEQ2} = 6\,\text{V}$. (b) with R_1 as found in part a, find V_{CEQ1}.

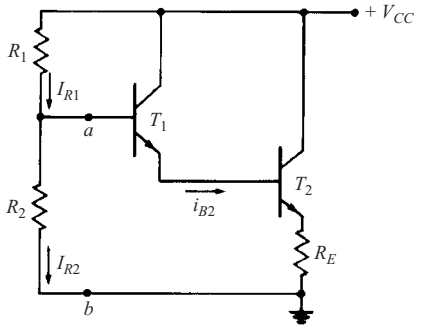


Fig. 3-21

(a) Since $R_2 \to \infty$, $I_{R2} = 0$ and $I_{BQ1} = I_{R1}$. By KVL,

$$I_{EQ2} = \frac{V_{CC} - V_{CEQ2}}{R_E} = \frac{12 - 6}{1 \times 10^3} = 6\,\text{mA}$$

Now

$$I_{BQ2} = \frac{I_{EQ2}}{\beta_2 + 1} = I_{EQ1}$$

and

$$I_{R1} = I_{BQ1} = \frac{I_{EQ1}}{\beta_1 + 1} = \frac{I_{EQ2}}{(\beta_1 + 1)(\beta_2 + 1)} = \frac{6 \times 10^{-3}}{(50 + 1)(50 + 1)} = 2.31\,\mu\text{A}$$

By KVL (around a path that includes R_1, both transistors, and R_E) and Ohm's law,

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{V_{CC} - V_{BEQ1} - V_{BEQ2} - I_{EQ2}R_E}{I_{R1}} = \frac{12 - 0.7 - 0.7 - (6 \times 10^{-3})(1 \times 10^3)}{2.31 \times 10^{-6}} = 1.99\,\text{M}\Omega$$

(b) Applying KVL around a path including both transistors and R_E, we have

$$V_{CEQ1} = V_{CC} - V_{BEQ2} - I_{EQ2}R_E = 12 - 0.7 - (6 \times 10^{-3})(1 \times 10^3) = 5.3\,\text{V}$$

3.21 The Si Darlington transistor pair of Fig. 3-21 has negligible leakage current, and $\beta_1 = \beta_2 = 60$. Let $R_1 = R_2 = 1\,\text{M}\Omega$, $R_E = 500\,\Omega$, and $V_{CC} = 12\,\text{V}$. Find (a) I_{EQ2}, (b) V_{CEQ2}, and (c) I_{CQ1}.

(a) A Thévenin equivalent for the circuit to the left of terminals a, b has

$$V_{Th} = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{1 \times 10^6}{1 \times 10^6 + 1 \times 10^6} 12 = 6\,\text{V}$$

and

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(1 \times 10^6)(1 \times 10^6)}{1 \times 10^6 + 1 \times 10^6} = 500\,\text{k}\Omega$$

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With the Thévenin circuit in place, KVL gives

$$V_{Th} = I_{BQ1}R_{Th} + V_{BEQ1} + V_{BEQ2} + I_{EQ2}R_E \tag{1}$$

Realizing that

$$I_{EQ2} = (\beta_2 + 1)I_{BQ2} = (\beta_2 + 1)(\beta_1 + 1)I_{BQ1}$$

we can substitute for I_{BQ1} in (*1*) and solve for I_{EQ2}, obtaining

$$I_{EQ2} = \frac{(\beta_1 + 1)(\beta_2 + 1)(V_{Th} - V_{BEQ1} - V_{BEQ2})}{R_{Th} + (\beta_1 + 1)(\beta_2 + 1)R_E} = \frac{(60 + 1)(60 + 1)(6 - 0.7 - 0.7)}{500 \times 10^3 + (60 + 1)(60 + 1)(500)} = 7.25\,\text{mA}$$

(*b*) By KVL,

$$V_{CEQ2} = V_{CC} - I_{EQ2}R_E = 12 - (7.25 \times 10^{-3})(500) = 8.375\,\text{V}$$

(*c*) From (*3.1*) and (*3.2*),

$$I_{CQ1} = \frac{\beta_1}{\beta_1 + 1} I_{EQ1} = \frac{\beta_1}{\beta_1 + 1} I_{BQ2} = \frac{\beta_1}{\beta_1 + 1} \frac{I_{EQ2}}{\beta_2 + 1} = \frac{60}{60 + 1} \frac{7.25 \times 10^{-3}}{60 + 1} = 116.9\,\mu\text{A}$$

3.22 The Si transistors in the differential amplifier circuit of Fig. 3-22 have negligible leakage current, and $\beta_1 = \beta_2 = 60$. Also, $R_C = 6.8\,\text{k}\Omega$, $R_B = 10\,\text{k}\Omega$, and $V_{CC} = V_{EE} = 15\,\text{V}$. Find the value of R_E needed to bias the amplifier such that $V_{CEQ1} = V_{CEQ2} = 8\,\text{V}$.

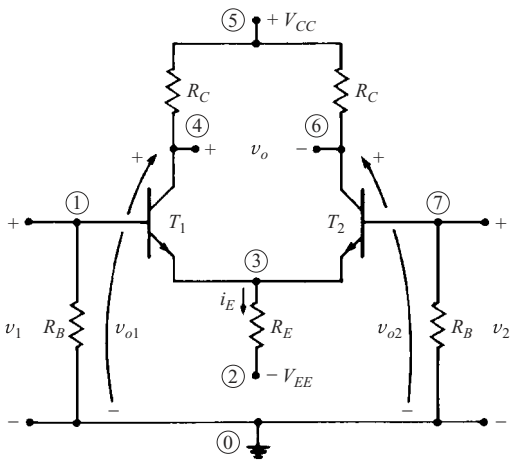


Fig. 3-22

By symmetry, $I_{EQ1} = I_{EQ2}$. Then, by KCL,

$$i_E = I_{EQ1} + I_{EQ2} = 2I_{EQ1} \tag{1}$$

Using (*1*) and (*2*) of Problem 3.17 (which apply to the T_1 circuit here), along with KVL around the left collector loop, gives

$$V_{CC} + V_{EE} = \frac{\beta_1}{\beta_1 + 1} I_{EQ1}R_C + V_{CEQ1} + 2I_{EQ1}R_E \tag{2}$$

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Applying KVL around the left base loop gives

$$V_{EE} = I_{BQ1}R_B + V_{BEQ1} + i_E R_E = \frac{I_{EQ1}}{\beta_1 + 1} R_B + V_{BEQ1} + 2I_{EQ1}R_E \tag{3}$$

Solving (3) for $2I_{EQ1}R_E$, substituting the result into (2), and solving for I_{EQ1} yield

$$I_{EQ1} = \frac{(\beta_1 + 1)(V_{CC} - V_{CEQ1} + V_{BEQ1})}{\beta_1 R_C - R_B} = \frac{(60 + 1)(15 - 8 + 0.7)}{(60)(6.8 \times 10^3) - 10 \times 10^3} = 1.18\,\text{mA}$$

and, by (3),

$$R_E = \frac{V_{EE} - V_{BEQ1} - \dfrac{R_B}{\beta_1 + 1} I_{EQ1}}{2I_{EQ1}} = \frac{15 - 0.7 - \dfrac{10 \times 10^3}{60 + 1} 1.18 \times 10^{-3}}{2(1.18 \times 10^{-3})} = 5.97\,\text{k}\Omega$$

3.23 The Si transistor of Fig. 3-23 has negligible leakage current, and $\beta = 100$. If $V_{CC} = 15\,\text{V}$, $V_{EE} = 4\,\text{V}$, $R_E = 3.3\,\text{k}\Omega$, and $R_C = 7.1\,\text{k}\Omega$, find (*a*) I_{BQ} and (*b*) V_{CEQ}.

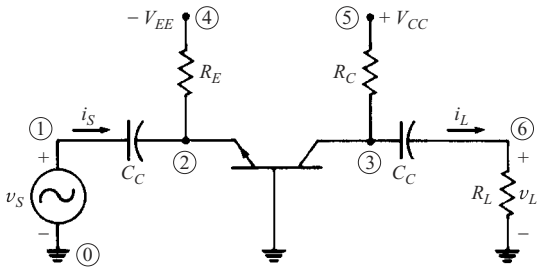


Fig. 3-23

(*a*) By KVL around the base-emitter loop,

$$I_{EQ} = \frac{V_{EE} - V_{BEQ}}{R_E} = \frac{4 - 0.7}{3.3 \times 10^3} = 1\,\text{mA}$$

Then, by (3.1) and (3.2),

$$I_{BQ} = \frac{I_{EQ}}{\beta + 1} = \frac{1 \times 10^{-3}}{100 + 1} = 9.9\,\mu\text{A}$$

(*b*) KVL and (2) of Problem 3.17 yield

$$V_{CEQ} = V_{CC} + V_{EE} - I_{EQ}R_E - I_{CQ}R_C = V_{CC} + V_{EE} - \left(R_E + \frac{\beta}{\beta + 1} R_C\right) I_{EQ}$$

$$= 15 + 4 - \left(3.3 \times 10^3 + \frac{100}{100 + 1} 7.1 \times 10^3\right)(1 \times 10^{-3}) = 8.67\,\text{V}$$

3.24 For the transistor circuit of Fig. 3-23, $C_C = 100\,\mu\text{F}$, $R_E = 3.3\,\text{k}\Omega$, $R_C = 8.1\,\text{k}\Omega$, $R_L = 15\,\text{k}\Omega$, $V_{CC} = 15\,\text{V}$, $V_{EE} = 4\,\text{V}$, and $v_S = 0.01\sin(2000\pi t)\,\text{V}$. The transistor can be described by the generic *npn* model. Use SPICE methods to (*a*) determine the quiescent voltage V_{CEQ} and (*b*) plot the input and output currents and voltages.

(*a*) The netlist code below describes the circuit.

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```
Prb3_24.CIR - CB amplifier
vs   1 0 SIN(0V 10mV 1kHz)
CC1  1 2 100uF
RE   2 4 3.3kohm
VEE  0 4 4V
Q 3  0 2 QNPNG
RC   3 5 8.1k
VCC  5 0 15V
CC2  3 6 100uF
RL   6 0 15kohm
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=30V Cjc=10pF Cje=15pF)
.DC VCC 15V 15V 1V
.PRINT DC V(3,2)
.TRAN 1us 1ms
.PROBE
.END
```

After executing ⟨Prb3_24.CIR⟩, examine the output file to find $V_{CEQ} = \text{V}(3, 2) = 7.47\,\text{V}$. Since $V_{CEQ} \simeq V_{CC}/2$, the transistor is biased for maximum symmetrical swing.

(*b*) Use the Probe feature of PSpice to plot the input and output currents and voltages as displayed by Fig. 3-24. Notice that this circuit amplifies the output voltage while the output current is actually less in amplitude than the input current.

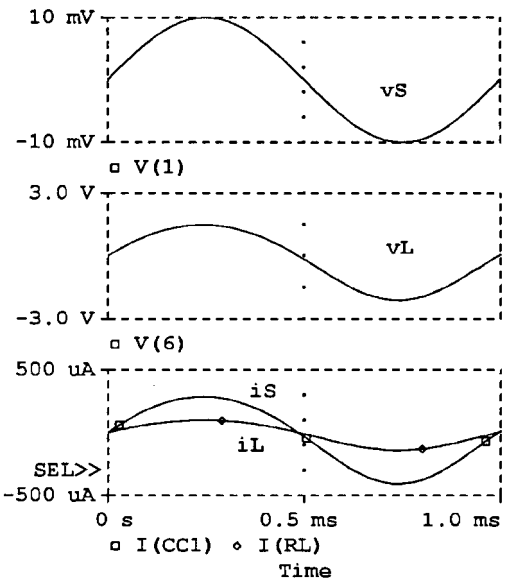


Fig. 3-24

3.25 Find the proper collector current bias for maximum symmetrical (or undistorted) swing along the ac load line of a transistor amplifier for which $V_{CEsat} = I_{CEO} = 0$.

For *maximum symmetrical swing*, the Q point must be set at the midpoint of the ac load line. Hence, from (*3.13*), we want

$$I_{CQ} = \frac{1}{2} i_{C\max} = \frac{1}{2}\left(\frac{V_{CEQ}}{R_{ac}} + I_{CQ}\right) \tag{1}$$

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But for a circuit such as that in Fig. 3-9(*a*), KVL gives

$$V_{CEQ} \approx V_{CC} - I_{CQ}R_{\text{dc}} \tag{2}$$

which becomes an equality if no emitter resistor is present. Substituting (*2*) into (*1*), assuming equality, and solving for I_{CQ} yield the desired result:

$$I_{CQ} = \frac{V_{CC}}{R_{\text{ac}} + R_{\text{dc}}} \tag{3}$$

3.26 In the circuit of Fig. 3-8(*a*), $R_E = 300\,\Omega$, $R_C = 500\,\Omega$, $V_{CC} = 15\,\text{V}$, $\beta = 100$, and the Si transistor has β-independent bias. Size R_1 and R_2 for maximum symmetrical swing if $V_{CE\text{sat}} \approx 0$.

For maximum symmetrical swing, the quiescent collector current is

$$I_{CQ} = \frac{1}{2}\frac{V_{CC}}{R_E + R_C} = \frac{15}{2(300 + 500)} = 9.375\,\text{mA}$$

Standard practice is to use a factor of 10 as the margin of inequality for β independence in (*3.8*). Then,

$$R_B = \frac{\beta R_E}{10} = \frac{(100)(300)}{10} = 3\,\text{k}\Omega$$

and, from (*3.7*),

$$V_{BB} \approx V_{BEQ} + I_{CQ}(1.1R_E) = 0.7 + (9.375 \times 10^{-3})(330) = 3.794\,\text{V}$$

Equations (*3.5*) may now be solved simultaneously to obtain

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{3 \times 10^3}{1 - 3.794/15} = 4.02\,\text{k}\Omega$$

and

$$R_2 = R_B\frac{V_{CC}}{V_{BB}} = 3 \times 10^3\,\frac{15}{3.794} = 11.86\,\text{k}\Omega$$

3.27 In the circuit of Fig. 3-10(*a*), the transistor is a Si device, $R_E = 200\,\Omega$, $R_2 = 10R_1 = 10\,\text{k}\Omega$, $R_L = R_C = 2\,\text{k}\Omega$, $\beta = 100$, and $V_{CC} = 15\,\text{V}$. Assume that C_C and C_E are very large, that $V_{CE\text{sat}} \approx 0$, and that $i_C = 0$ at cutoff. Find (*a*) I_{CQ}, (*b*) V_{CEQ}, (*c*) the slope of the ac load line, (*d*) the slope of the dc load line, and (*e*) the peak value of undistorted i_L.

(*a*) Equations (*3.5*) and (*3.7*), give

$$R_B = \frac{(1 \times 10^3)(10 \times 10^3)}{11 \times 10^3} = 909\,\Omega \qquad \text{and} \qquad V_{BB} = \frac{1 \times 10^3}{11 \times 10^3}\,15 = 1.364\,\text{V}$$

so

$$I_{CQ} \approx \frac{V_{BB} - V_{BEQ}}{R_B/(\beta + 1) + R_E} = \frac{1.364 - 0.7}{(909/101) + 200} = 3.177\,\text{mA}$$

(*b*) KVL around the collector-emitter circuit, with $I_{CQ} \approx I_{EQ}$, gives

$$V_{CEQ} = V_{CC} - I_{CQ}(R_E + R_C) = 15 - (3.177 \times 10^{-3})(2.2 \times 10^3) = 8.01\,\text{V}$$

(*c*)

$$\text{Slope} = \frac{1}{R_{\text{ac}}} = \frac{1}{R_C} + \frac{1}{R_L} = 2\,\frac{1}{2 \times 10^3} = 1\,\text{mS}$$

(*d*)

$$\text{Slope} = \frac{1}{R_{\text{dc}}} = \frac{1}{R_C + R_E} = \frac{1}{2.2 \times 10^3} = 0.454\,\text{mS}$$

(*e*) From (*3.14*), the ac load line intersects the v_{CE} axis at

$$v_{CE\,\text{max}} = V_{CEQ} + I_{CQ}R_{\text{ac}} = 8.01 + (3.177 \times 10^{-3})(1 \times 10^3) = 11.187\,\text{V}$$

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Since $v_{CE\max} < 2V_{CEQ}$, cutoff occurs before saturation and thus sets V_{cem}. With the large capacitors appearing as ac shorts,

$$i_L = \frac{v_L}{R_L} = \frac{v_{ce}}{R_L}$$

or, in terms of peak values,

$$I_{Lm} = \frac{V_{cem}}{R_L} = \frac{v_{CE\max} - V_{CEQ}}{R_L} = \frac{11.187 - 8.01}{2 \times 10^3} = 1.588\,\text{mA}$$

3.28 In the circuit of Fig. 3-8(*a*), $R_C = 300\,\Omega$, $R_E = 200\,\Omega$, $R_1 = 2\,\text{k}\Omega$, $R_2 = 15\,\text{k}\Omega$, $V_{CC} = 15\,\text{V}$, and $\beta = 110$ for the Si transistor. Assume that $I_{CQ} \approx I_{EQ}$ and $V_{CE\text{sat}} \approx 0$. Find the maximum symmetrical swing in collector current (*a*) if an ac base current is injected, and (*b*) if V_{CC} is changed to 10 V but all else remains the same.

(*a*) From (*3.5*) and (*3.7*),

$$R_B = \frac{(2 \times 10^3)(15 \times 10^3)}{17 \times 10^3} = 1.765\,\text{k}\Omega \qquad \text{and} \qquad V_{BB} = \frac{2 \times 10^3}{17 \times 10^3}\,15 = 1.765\,\text{V}$$

so $$I_{CQ} \approx I_{EQ} = \frac{V_{BB} - V_{BEQ}}{R_B/(\beta + 1) + R_E} = \frac{1.765 - 0.7}{1765/111 + 200} = 4.93\,\text{mA}$$

By KVL around the collector-emitter circuit with $I_{CQ} \approx I_{EQ}$,

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) = 15 - (4.93 \times 10^{-3})(200 + 300) = 12.535\,\text{V}$$

Since $V_{CEQ} > V_{CC}/2 = 7.5\,\text{V}$, cutoff occurs before saturation, and i_C can swing $\pm 4.93\,\text{mA}$ about I_{CQ} and remain in the active region.

(*b*) $$V_{BB} = \frac{R_1}{R_1 + R_2}\,V_{CC} = \frac{2 \times 10^3}{17 \times 10^3}\,10 = 1.1765\,\text{V}$$

so that $$I_{CQ} \approx I_{EQ} = \frac{V_{BB} - V_{BEQ}}{R_B/(\beta + 1) + R_E} = \frac{1.1765 - 0.7}{1765/111 + 200} = 2.206\,\text{mA}$$

and $$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) = 10 - (2.206 \times 10^{-3})(0.5) = 8.79\,\text{V}$$

Since $V_{CEQ} > V_{CC}/2 = 5\,\text{V}$, cutoff again occurs before saturation, and i_C can swing $\pm 2.206\,\text{mA}$ about I_{CQ} and remain in the active region of operation. Here, the 33.3 percent reduction in power supply voltage has resulted in a reduction of over 50 percent in symmetrical collector-current swing.

3.29 If a Si transistor were removed from the circuit of Fig. 3-8(*a*) and a Ge transistor of identical β were substituted, would the Q point move in the direction of saturation or of cutoff?

Since R_1, R_2, and V_{CC} are unchanged, R_B and V_{BB} would remain unchanged. However, owing to the different emitter-to-base forward drops for Si (0.7 V) and Ge (0.3 V) transistors,

$$I_{CQ} \approx \frac{V_{BB} - V_{BEQ}}{R_B/(\beta + 1) + R_E}$$

would be higher for the Ge transistor. Thus, the Q point would move in the direction of saturation.

3.30 In the circuit of Fig. 3-10(*a*), $V_{CC} = 12\,\text{V}$, $R_C = R_L = 1\,\text{k}\Omega$, $R_E = 100\,\Omega$, and $C_C = C_E \to \infty$. The Si transistor has negligible leakage current, and $\beta = 100$. If $V_{CE\text{sat}} = 0$ and the transistor is to have β-independent bias (by having $R_1 \| R_2 = \beta R_E/10$), size R_1 and R_2 for maximum symmetrical swing.

Evaluating R_{ac} and R_{dc}, we find

$$R_{\text{ac}} = R_L \| R_C = \frac{(1 \times 10^3)(1 \times 10^3)}{1 \times 10^3 + 1 \times 10^3} = 500\,\Omega \qquad R_{\text{dc}} = R_C + R_E = 1 \times 10^3 + 100 = 1100\,\Omega$$

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Thus, according to (*3*) of Problem 3.25, maximum symmetrical swing requires that

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{12}{500 + 1100} = 7.5\,\text{mA}$$

Now,
$$R_B = R_1 \| R_2 = \frac{\beta R_E}{10} = \frac{(100)(100)}{10} = 1\,\text{k}\Omega$$

and, by (*3.6*) and (*2*) of Problem 3.17,

$$V_{BB} = \left(\frac{R_B}{\beta} + \frac{\beta + 1}{\beta}\, R_E\right) I_{CQ} + V_{BEQ} = \left(\frac{1 \times 10^3}{100} + \frac{100 + 1}{100}\, 100\right) 7.5 \times 10^{-3} + 0.7 = 1.53\,\text{V}$$

Finally, from (*3.5*),

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{1 \times 10^3}{1 - 1.53/12} = 1.34\,\text{k}\Omega \qquad \text{and} \qquad R_2 = \frac{R_B V_{CC}}{V_{BB}} = \frac{(1 \times 10^3)(12)}{1.53} = 10.53\,\text{k}\Omega$$

3.31 The Si transistor of Fig. 3-10(*a*) has $V_{CE\text{sat}} = I_{CBO} = 0$ and $\beta = 75$. C_E is removed from the circuit, and $C_C \to \infty$. Also, $R_1 = 1\,\text{k}\Omega$, $R_2 = 9\,\text{k}\Omega$, $R_E = R_L = R_C = 1\,\text{k}\Omega$, and $V_{CC} = 15\,\text{V}$. (*a*) Sketch the dc and ac load lines for this amplifier on a set of i_C-v_{CE} axes. (*b*) Find the maximum undistorted value of i_L, and determine whether cutoff or saturation limits i_L swing.

(*a*)
$$R_{dc} = R_C + R_E = 1 \times 10^3 + 1 \times 10^3 = 2\,\text{k}\Omega$$

and
$$R_{ac} = R_E + R_C \| R_L = 1 \times 10^3 + \frac{(1 \times 10^3)(1 \times 10^3)}{1 \times 10^3 + 1 \times 10^3} = 1.5\,\text{k}\Omega$$

By (*3.5*),

$$V_{BB} = \frac{R_1}{R_2}\, V_{CC} = \frac{1 \times 10^3}{9 \times 10^3}\, 15 = 1.667\,\text{V} \qquad \text{and} \qquad R_B = R_1 \| R_2 = \frac{(1 \times 10^3)(9 \times 10^3)}{1 \times 10^3 + 9 \times 10^3} = 900\,\Omega$$

and from (*3.7*),

$$I_{CQ} = \frac{(\beta + 1)(V_{BB} - V_{BEQ})}{R_B + (\beta + 1) R_E} = \frac{(75 + 1)(1.667 - 0.7)}{900 + (75 + 1)(1 \times 10^3)} = 0.96\,\text{mA}$$

By KVL around the collector loop and (*2*) of Problem 3.17,

$$V_{CEQ} = V_{CC} - \left(R_C + \frac{\beta + 1}{\beta}\, R_E\right) I_{CQ} = 15 - \left(1 \times 10^3 + \frac{75 + 1}{75}\, 1 \times 10^3\right) 0.96 \times 10^{-3} = 13.07\,\text{V}$$

The ac load-line intercepts now follow directly from (*3.13*) and (*3.14*):

$$i_{C\,\max} = \frac{V_{CEQ}}{R_{ac}} + I_{CQ} = \frac{13.07}{1.5 \times 10^3} + 0.96 \times 10^{-3} = 9.67\,\text{mA}$$
$$v_{CE\,\max} = V_{CEQ} + I_{CQ} R_{ac} = 13.07 + (0.96 \times 10^{-3})(1.5 \times 10^3) = 14.51\,\text{V}$$

The dc load-line intercepts follow from (*3.9*):

$$i_C\text{-axis intercept} = \frac{V_{CC}}{R_{dc}} = \frac{15}{2 \times 10^3} = 7.5\,\text{mA}$$
$$v_{CE}\text{-axis intercept} = V_{CC} = 15\,\text{V}$$

The required load lines are sketched in Fig. 3.25.

(*b*) Since $I_{CQ} < \frac{1}{2} i_{C\,\max}$, it is apparent that cutoff limits the undistorted swing of i_c to $\pm I_{CQ} = \pm 1.92\,\text{mA}$. By current division,

$$i_L = \frac{R_E}{R_E + R_L}\, i_c = \frac{1 \times 10^3}{1 \times 10^3 + 1 \times 10^3}\, (\pm 0.96\,\text{mA}) = \pm 0.48\,\text{mA}$$

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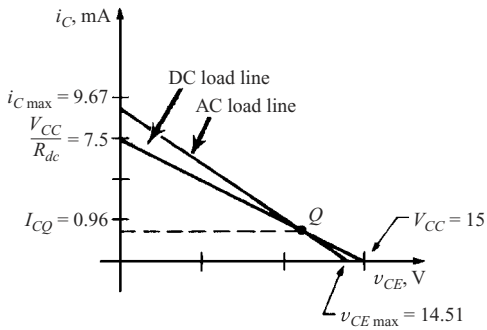


Fig. 3-25

3.32 In the *common-collector* (CC) or *emitter-follower* (EF) amplifier of Fig. 3-26(*a*), $V_{CC} = 12\,\text{V}$, $R_E = 1\,\text{k}\Omega$, $R_L = 3\,\text{k}\Omega$, and $C_C \to \infty$. The Si transistor is biased so that $V_{CEQ} = 5.7\,\text{V}$ and has the collector characteristic of Fig. 3-26(*b*). (*a*) Construct the dc load line. (*b*) Find the value of β. (*c*) Determine the value of R_B.

(*a*) The dc load line must intercept the v_{CE} axis at $V_{CC} = 12\,\text{V}$. It intercepts the i_C axis at

$$\frac{V_{CC}}{R_{\text{dc}}} = \frac{V_{CC}}{R_E} = \frac{12}{1 \times 10^3} = 12\,\text{mA}$$

The intercepts are connected to form the dc load line shown on Fig. 3-26(*b*).

(*b*) I_{BQ} is determined by entering Fig. 3-26(*b*) at $V_{CEQ} = 5.7\,\text{V}$ and interpolating between i_B curves to find $I_{BQ} \approx 50\,\mu\text{A}$. I_{CQ} is then read as $\approx 6.3\,\text{mA}$. Thus,

$$\beta = \frac{I_{CQ}}{I_{BQ}} = \frac{6.3 \times 10^{-3}}{50 \times 10^{-6}} = 126$$

(*c*) By KVL,

$$R_B = \frac{V_{CC} - V_{BEQ} - \dfrac{\beta + 1}{\beta} I_{CQ} R_E}{I_{BQ}} = \frac{12 - 0.7 - \dfrac{126 + 1}{126}(6 \times 10^{-3})(1 \times 10^3)}{50 \times 10^{-6}} = 105.05\,\text{k}\Omega$$

3.33 The amplifier of Fig. 3-27 uses an Si transistor for which $V_{BEQ} = 0.7\,\text{V}$. Assuming that the collector-emitter bias does not limit voltage excursion, classify the amplifier according to Table 3-4 if (*a*) $V_B = 1.0\,\text{V}$ and $v_S = 0.25\cos\omega t\,\text{V}$, (*b*) $V_B = 1.0\,\text{V}$ and $v_S = 0.5\cos\omega t\,\text{V}$, (*c*) $V_B = 0.5\,\text{V}$ and $v_S = 0.6\cos\omega t\,\text{V}$, (*d*) $V_B = 0.7\,\text{V}$ and $v_S = 0.5\cos\omega t\,\text{V}$.

As long as $v_S + V_B > 0.7\,\text{V}$, the emitter-base junction is forward-biased; thus classification becomes a matter of determining the portion of the period of v_S over which the above inequality holds.

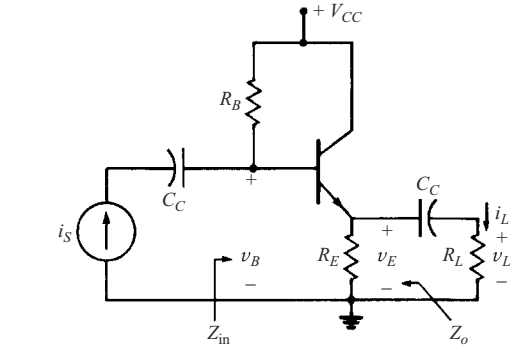
(*a*) $v_S + V_B \geq 0.75\,\text{V}$ through the complete cycle; thus the transistor is always in the active region, and the amplifier is of class A.

(*b*) $0.5 \leq v_S + V_B \leq 1.5\,\text{V}$; thus the transistor is cut off for a portion of the negative excursion v_S. Since cutoff occurs during less than 180°, the amplifier is of class AB.

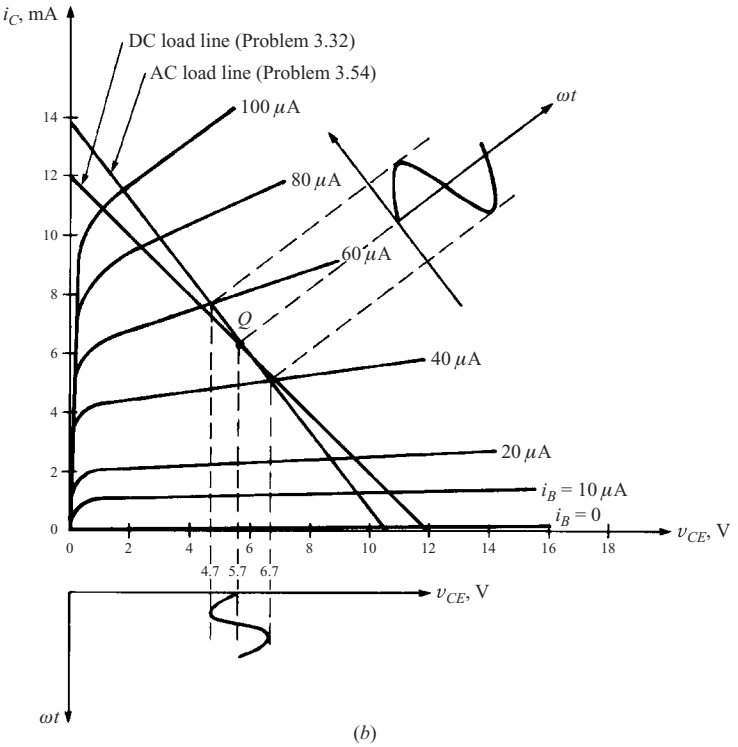
(*c*) $-0.1 \leq v_S + V_B \leq 1.1\,\text{V}$, which gives conduction for less than 180° of the period of v_S, for class C operation.

(*d*) $v_S + V_B \geq 0.7\,\text{V}$ over exactly 180° of the period of v_S, for class B operation.

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(*a*)



(*b*)

Fig. 3-26

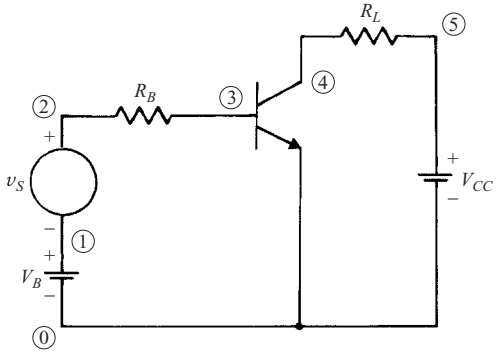


Fig. 3-27

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Supplementary Problems

3.34 The leakage currents of a transistor are $I_{CBO} = 5\,\mu A$ and $I_{CEO} = 0.4$ mA, and $I_B = 30\ \mu A$. Determine the value of I_C. *Ans.* 277 mA

3.35 For a BJT, $I_C = 5.2$ mA, $I_B = 50\ \mu A$, and $I_{CBO} = 0.5\ \mu A$. (*a*) Find β and I_{EQ}. (*b*) What is the percentage error in the calculation of β if the leakage current is assumed zero? *Ans.* (*a*) 102.96, 5.25 mA; (*b*) 1.01%

3.36 Collector-to-base leakage current can be modeled by a current source as in Fig. 3-28, with the understanding that transistor action relates currents I'_C, I'_B, and I_E ($I'_C = \alpha I_E$, and $I'_C = \beta I'_B$). Prove that

$$(a)\ I_C = \beta I_B + (\beta + 1)I_{CBO} \quad (b)\ I_B = \frac{I_E}{\beta + 1} - I_{CBO} \quad (c)\ I_E = \frac{\beta + 1}{\beta}(I_C - I_{CBO})$$

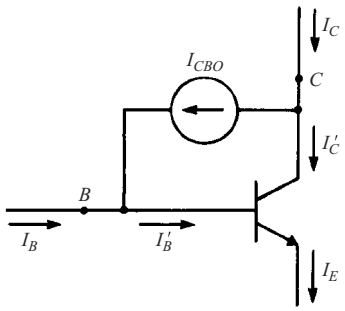


Fig. 3-28

3.37 If the transistor of Problem 3.4 were replaced by a new transistor with 1 percent greater α, what would be the percentage change in emitter current? *Ans.* a 96.07% increase

3.38 In the circuit of Fig. 3-11, $V_{CE\text{sat}} = 0.2$ V, $\alpha = 0.99$, $I_{BQ} = 20\,\mu A$, $V_{CC} = 15$ V, and $R_C = 15\,k\Omega$. What is the value of V_{CEQ}? *Ans.* $V_{CEQ} = V_{CE\text{sat}} = 0.2$ V

3.39 In many switching applications, the transistor may be utilized without a heat sink, since $P_C \approx 0$ in cutoff and P_C is small in saturation. Support this statement by calculating the collector power dissipated in (*a*) Problem 3.6 (active-region bias) and (*b*) Problem 3.38 (saturation-region bias).
Ans. (*a*) 18 mW; (*b*) 0.39 mW

3.40 The collector characteristics of the transistor of Fig. 3-11 are given in Fig. 3-9(*b*). If $I_{BQ} = 40\,\mu A$, $V_{CC} = 15$ V, and $R_C = 2.2\,k\Omega$, specify the minimum power rating of the transistor to ensure there is no danger of thermal damage. *Ans.* 22.54 mW

3.41 In the circuit of Fig. 3-13, $V_{CC} = 20$ V, $R_C = 5\,k\Omega$, $R_E = 4\,k\Omega$, and $R_B = 500\,k\Omega$. The Si transistor has $I_{CBO} = 0$ and $\beta = 50$. Find I_{CQ} and V_{CEQ}. *Ans.* 1.91 mA, 2.64 V

3.42 The transistor of Problem 3.41 failed and was replaced with a new transistor with $I_{CBO} = 0$ and $\beta = 75$. Is the transistor still biased for active-region operation?
Ans. Since the calculated $V_{CEQ} = -6.0\text{ V} < 0$, the transistor is not in the active region.

3.43 What value of R_B will result in saturation of the Si transistor of Fig. 3-13 if $V_{CC} = 20$ V, $R_C = 5\,k\Omega$, $R_E = 4\,k\Omega$, $\beta = 50$, and $V_{CE\text{sat}} = 0.2$ V? *Ans.* $R_B \leq 442.56\,k\Omega$

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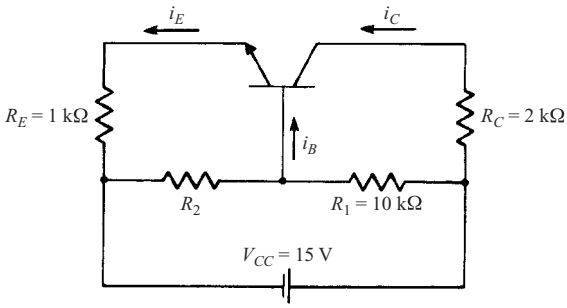


Fig. 3-29

3.44 The circuit of Fig. 3-29 illustrates a method for biasing a CB transistor using a single dc source. The transistor is a Si device ($V_{BEQ} = 0.7\,\text{V}$), $\beta = 99$, and $I_{BQ} = 30\,\mu\text{A}$. Find (*a*) R_2, and (*b*) V_{CEQ}.
Ans. (*a*) $3.36\,\text{k}\Omega$; (*b*) $6.06\,\text{V}$

3.45 Rework Problem 3.28(*a*) with $R_2 = 5\,\text{k}\Omega$ and all else unchanged.
Ans. $\pm 13.16\,\text{mA}$ and $I_{CQ} = 16.84\,\text{mA}$

3.46 Because of a poor solder joint, resistor R_1 of Problem 3.28(*a*) becomes open-circuited. Calculate the percentage change in I_{CQ} that will be observed. *Ans.* $+508.5\%$

3.47 The circuit of Problem 3-28(*a*) has β-independent bias ($R_E \geq 10R_B/\beta$). Find the allowable range of β if I_{CQ} can change at most ± 2 percent from its value for $\beta = 110$. *Ans.* $86.4 \leq \beta \leq 149.7$

3.48 For the circuit of Fig. 3-27, $v_S = 0.25\cos\omega t\,\text{V}$, $R_B = 30\,\text{k}\Omega$, $V_B = 1\,\text{V}$, and $V_{CC} = 12\,\text{V}$. The transistor is described by the default *npn* model. If $V_{CE\text{sat}} \simeq 0$ and $I_{CBO} = 0$, use SPICE methods to determine the range of R_L for class A operation. *Hint*: A sweep of R_L values can determine the particular value of R_L for which $V_{CEQ} = V_{CC}/2$. (*Netlist code available at author website.*) *Ans.* $R_L \leq 7.74\,\text{k}\Omega$

3.49 If an emitter resistor is added to the circuit of Fig. 3-17, find the value of R_F needed to bias for maximum symmetrical swing. Let $V_{CC} = 15\,\text{V}$, $R_E = 1.5\,\text{k}\Omega$, and $R_C = 5\,\text{k}\Omega$. Assume the transistor is an Si device with $I_{CEO} = V_{CE\text{sat}} = 0$ and $\beta = 80$. *Ans.* $477.4\,\text{k}\Omega$

3.50 In the circuit of Fig. 3-20, the Ge transistor has $I_{CEO} = 0$ and $\beta = 50$. Assume the capacitor is replaced with a short circuit. Let $V_S = 2\,\text{V}$, $V_{CC} = 12\,\text{V}$, $R_C = 4\,\text{k}\Omega$, $R_S = 100\,\text{k}\Omega$, and $R_B = 330\,\text{k}\Omega$. Find the ratios (*a*) I_{CQ}/I_s and (*b*) V_{CEQ}/V_S. *Ans.* (*a*) 374.6; (*b*) 0.755

3.51 In the differential amplifier circuit of Fig. 3-22, the two identical transistors are characterized by the default *npn* model. Let $R_B = 10\,\text{k}\Omega$, $R_E = R_C = 6.8\,\text{k}\Omega$, and $V_{CC} = V_{EE} = 15\,\text{V}$. Use SPICE methods to determine (*a*) V_{BEQ1} and (*b*) voltages $v_{o1} = v_{o2}$. (*Netlist code available from author website.*)
Ans. (*a*) $V_{BEQ1} = \text{V}(4, 3) = 8.89\,\text{V}$; (*b*) $v_{o1} = v_{o2} = \text{V}(4) = \text{V}(6) = 8.01\,\text{V}$

3.52 In the amplifier of Fig. 3-10(*a*), $R_1 = 1\,\text{k}\Omega$, $R_2 = 9\,\text{k}\Omega$, $R_E = 100\,\Omega$, $R_L = 1\,\text{k}\Omega$, $V_{CC} = 12\,\text{V}$, $C_C = C_E \to \infty$, and $\beta = 100$. The Si transistor has negligible leakage current, with $V_{CE\text{sat}} = I_{CBO} = 0$. Find R_C so that v_L exhibits maximum symmetrical swing. *Ans.* $1.89\,\text{k}\Omega$

3.53 If in Problem 3.31, R_1 is changed to $9\,\text{k}\Omega$ and all else remains unchanged, determine the maximum undistorted swing of i_c. *Ans.* $\pm 1.5\,\text{mA}$

3.54 In the CC amplifier of Problem 3.32, let $i_S = 10\sin\omega t\,\mu\text{A}$. Calculate v_L after graphically determining v_{CE}.
Ans. The ac load line and v_{CE} are sketched on Fig. 3-26: $v_{CE} \approx 5.7 - \sin\omega t\,\text{V}$; $v_L = \sin\omega t\,\text{V}$

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CHAPTER 4

Characteristics of Field-Effect Transistors and Triodes

4.1. INTRODUCTION

The operation of the *field-effect transistor* (FET) can be explained in terms of only majority-carrier (one-polarity) charge flow; the transistor is therefore called *unipolar*. Two kinds of field-effect devices are widely used: the *junction field-effect transistor* (JFET) and the *metal-oxide-semiconductor field-effect transistor* (MOSFET).

4.2. JFET CONSTRUCTION AND SYMBOLS

The physical arrangement of, and symbols for, the two kinds of JFET are shown in Fig. 4-1. Conduction is by the passage of charge carriers from *source* (*S*) to *drain* (*D*) through the *channel* between the *gate* (*G*) elements.

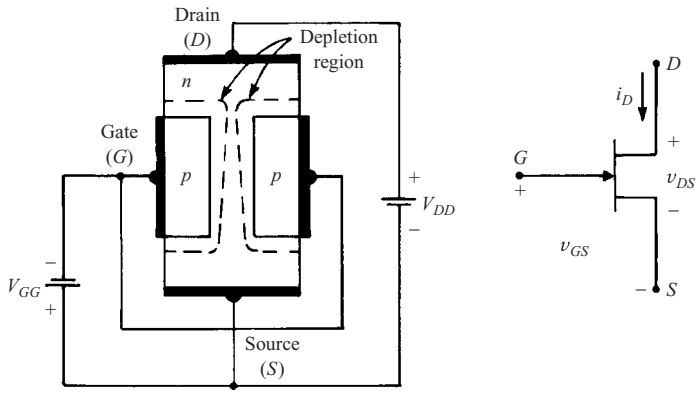
The transistor can be an *n-channel* device (conduction by electrons) or a *p-channel* device (conduction by holes); a discussion of *n*-channel devices applies equally to *p*-channel devices if *complementary* (opposite in sign) voltages and currents are used. Analogies between the JFET and the BJT are shown in Table 4-1. Current and voltage symbology for FETs parallels that given in Table 3-1.

4.3. JFET TERMINAL CHARACTERISTICS

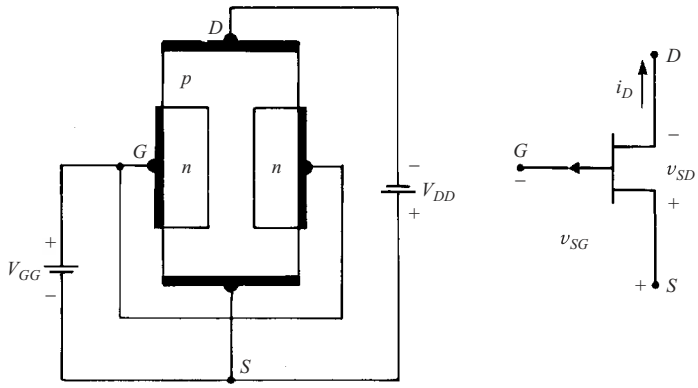
The JFET is almost universally applied in the *common-source* (CS) two-port arrangement of Fig. 4-1, where v_{GS} maintains a reverse bias of the gate-source *pn* junction. The resulting gate leakage current is negligibly small for most analyses (usually less than 1 μA), allowing the gate to be treated as an open circuit. Thus, no input characteristic curves are necessary.

Typical *output* or *drain characteristics* for an *n*-channel JFET in CS connection with $v_{GS} \leq 0$ are given in Fig. 4-2(*a*). For a constant value of v_{GS}, the JFET acts as a linear resistive device (in the *ohmic region*) until the *depletion region* of the reverse-biased gate-source junction extends the width of the channel (a condition called *pinchoff*). Above pinchoff but below avalanche breakdown, drain current i_D

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(*a*) *n*-channel JFET



(*b*) *p*-channel JFET

Fig. 4-1

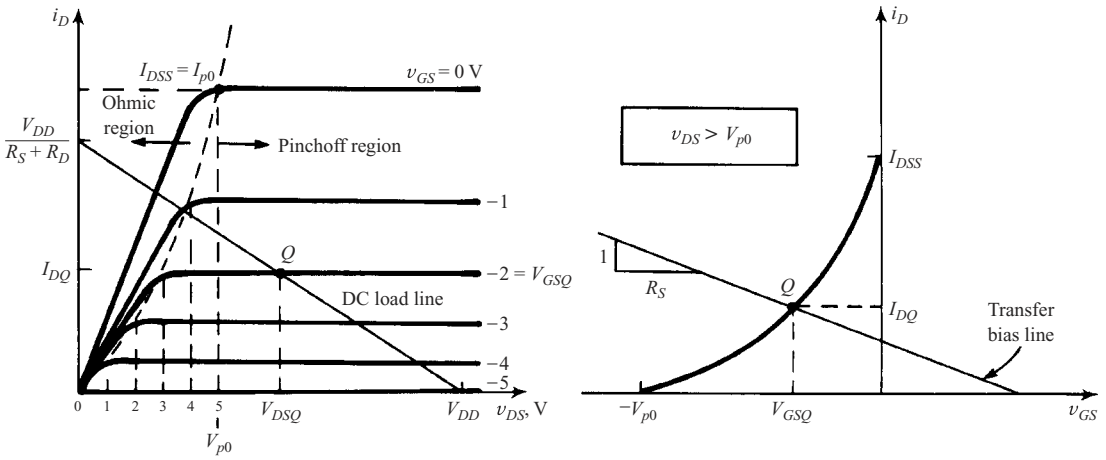
remains nearly constant as v_{DS} is increased. For specification purposes, the *shorted-gate parameters* I_{DSS} and V_{p0} are defined as indicated in Fig. 4-2(*a*); typically, V_{p0} is between 4 and 5 V. As gate potential decreases, the *pinchoff voltage*, that is, the source-to-drain voltage V_p at which pinchoff occurs, also decreases, approximately obeying the equation

$$V_p = V_{p0} + v_{GS} \tag{4.1}$$

Table 4-1

JFET	BJT
source S	emitter E
drain D	collector C
gate G	base B
drain supply V_{DD}	collector supply V_{CC}
gate supply V_{GG}	base supply V_{BB}
drain current i_D	collector current i_C

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(*a*) Drain characteristics (*b*) Transfer characteristic

Fig. 4-2 CS *n*-channel JFET

The drain current shows an approximate square-law dependence on source-to-gate voltage for constant values of v_{DS} in the pinchoff region:

$$i_D = I_{DSS}\left(1 + \frac{v_{GS}}{V_{p0}}\right)^2 \tag{4.2}$$

This accounts for the unequal vertical spacing of the characteristic curves in Fig. 4-2(*a*). Figure 4-2(*b*) is the graph of (*4.2*), known as the *transfer characteristic* and utilized in bias determination. The transfer characteristic is also determined by the intersections of the drain characteristics with a fixed vertical line, $v_{DS} =$ constant. To the extent that the drain characteristics actually are horizontal in the pinchoff region, one and the same transfer characteristic will be found for all $v_{DS} > V_{p0}$. (See Fig. 4-4 for a slightly nonideal case.)

4.4. JFET SPICE MODEL

The element specification statement for a JFET must explicitly assign a *model name* that is an arbitrary selection of alpha and numeric characters. The general form is

$$\text{J}\cdots n_1\ n_2\ n_3\ \textit{model name}$$

Nodes n_1, n_2, and n_3 belong to the drain, gate, and source, respectively. Only the *n*-channel JFET is addressed in this book. Positive voltage and current directions for the device are clarified by Fig. 4-3.

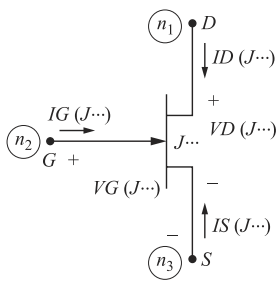


Fig. 4-3

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A .MODEL control statement must appear in the netlist code for a JFET circuit. The control statement has the following format:

.MODEL *model name* NJF (*parameters*)

If the parameter field is left blank, default values are assigned. Nondefault parameters are entered in the parameter field using the format *parameter name* = *value*. The specific parameters of concern in the book are documented by Table 4-2. The SPICE model describes the JFET in the pinchoff region by

$$i_D = \frac{I_{DSS}}{(Vto)^2}(Vto + v_{GS})^2 = Beta(Vto + v_{GS})^2$$

Table 4-2

Parameter	Description	Major Impact	Default	Units
Vto	pinchoff voltage	shorted-gate current	−2	V
Beta	transcond. coeff.	shorted-gate current	0.0001	A/V^2
Rd	drain resistance	current limit	0	Ω
Rs	source resistance	current limit	0	Ω
CGS	gate-source cap.	high frequency	0	F
CGD	gate-drain cap.	high frequency	0	F

Example 4.1. Use SPICE methods to generate (*a*) the CS drain characteristics and (*b*) the transfer characteristic for an *n*-channel JFET that has the parameter values Vto = −4 V, Beta = 0.0005 A/V^2, Rd = 1 Ω, Rs = 1 Ω, and CGS = CGD = 2 pF.

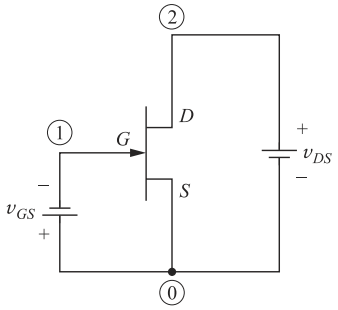
(*a*) Figure 4-4(*a*) shows a connection method for measurement of both the drain characteristics and the transfer characteristic. The following netlist code generates the drain characteristics that have been plotted using the Probe feature of PSpice as Fig. 4-4(*b*).

```
Ex4_1a.CIR - JFET drain characteristics
vGS 1 0 0V
vDS 2 0 0V
J 2  1 0 NJFET
.MODEL NJFET NJF ( Vto=-4V Beta=0.0005ApVsq
+ Rd=1ohm Rs=1ohm CGS=2pF CGD=2pF)
.DC vDS 0V 25V 0.5V vGS 0V -4V 0.5V
.PROBE
.END
```

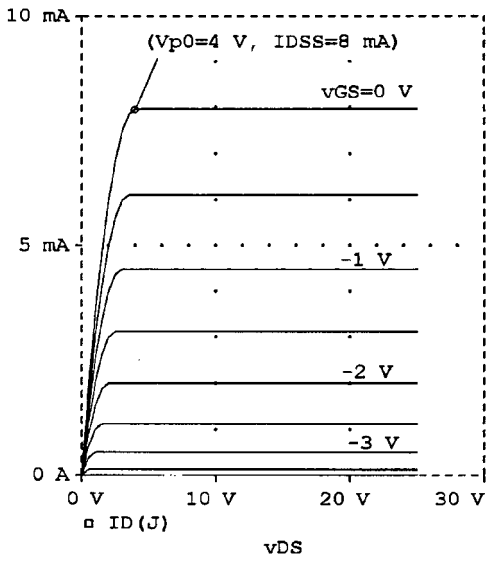
(*b*) The netlist code below holds v_{DS} constant to calculate the transfer characteristic that has been plotted by use of the Probe feature as Fig. 4-4(*c*).

```
Ex4_1b.CIR - JFET transfer characteristic
vGS 1 0 0V
vDS 2 0 10V
J 2  1 0 NJFET
.MODEL NJFET NJF ( Vto=-4V Beta=0.0005ApVsq
+ Rd=1ohm Rs=1ohm CGS=2pF CGD=2pF)
.DC vGS 0V -4V 0.5V
.PROBE
.END
```

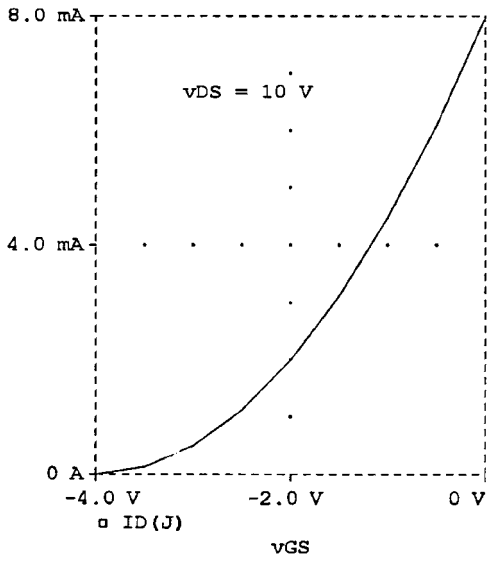
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(*a*)



(*b*)



(*c*)

Fig. 4-4

4.5. JFET BIAS LINE AND LOAD LINE

The commonly used *voltage-divider* bias arrangement of Fig. 4-5(*a*) can be reduced to its equivalent in Fig. 4-5(*b*), where the Thévenin parameters are given by

$$R_G = \frac{R_1 R_2}{R_1 + R_2} \qquad \text{and} \qquad V_{GG} = \frac{R_1}{R_1 + R_2} V_{DD} \tag{4.3}$$

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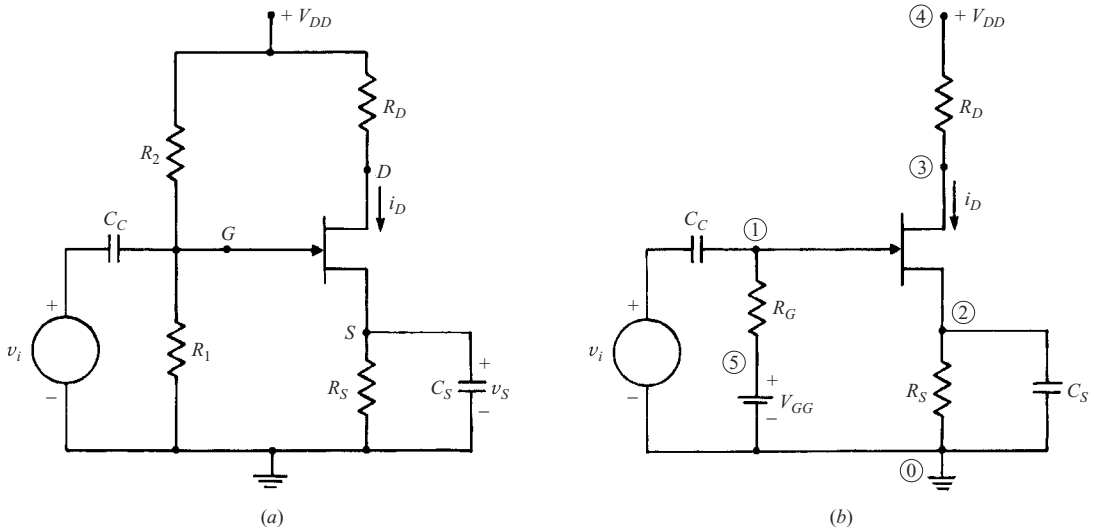


Fig. 4-5

With $i_G = 0$, application of KVL around the gate-source loop of Fig. 4-5(b) yields the equation of the *transfer bias line*,

$$i_D = \frac{V_{GG}}{R_S} - \frac{v_{GS}}{R_S} \tag{4.4}$$

which can be solved simultaneously with (*4.2*) or plotted as indicated on Fig. 4-2(b) to yield I_{DQ} and V_{GSQ}, two of the necessary three quiescent variables.

Application of KVL around the drain-source loop of Fig. 4-5(b) leads to the equation of the *dc load line*,

$$i_D = \frac{V_{DD}}{R_S + R_D} - \frac{v_{DS}}{R_S + R_D} \tag{4.5}$$

which, when plotted on the drain characteristics of Fig. 4-2(a), yields the remaining quiescent value, V_{DSQ}. Alternatively, with I_{DQ} already determined,

$$V_{DSQ} = V_{DD} - (R_S + R_D)I_{DQ}$$

Example 4.2. In the amplifier of Fig. 4-5(a), $V_{DD} = 20\,\text{V}$, $R_1 = 1\,\text{M}\Omega$, $R_2 = 15.7\,\text{M}\Omega$, $R_D = 3\,\text{k}\Omega$, and $R_S = 2\,\text{k}\Omega$. If the JFET characteristics are given by Fig. 4-6, find (a) I_{DQ}, (b) V_{GSQ}, and (c) V_{DSQ}.

(a) By (*4.3*),

$$V_{GG} = \frac{R_1}{R_1 + R_2} V_{DD} = \frac{1 \times 10^6}{16.7 \times 10^6} 20 = 1.2\,\text{V}$$

On Fig. 4-6(a), we construct the transfer bias line (*4.4*); it intersects the transfer characteristic at the Q point, giving $I_{DQ} = 1.5\,\text{mA}$.

(b) The Q point of Fig. 4-6(a) also gives $V_{GSQ} = -2\,\text{V}$.

(c) We construct the dc load line on the drain characteristics, making use of the v_{DS} intercept of $V_{DD} = 20\,\text{V}$ and the i_D intercept of $V_{DD}/(R_S + R_D) = 4\,\text{mA}$. The Q point was established at $I_{DQ} = 1.5\,\text{mA}$ in part a and at $V_{GSQ} = -2\,\text{V}$ in part b; its abscissa is $V_{DSQ} = 12.5\,\text{V}$. Analytically,

$$V_{DSQ} = V_{DD} - (R_S + R_D)I_{DQ} = 20 - (5 \times 10^3)(1.5 \times 10^{-3}) = 12.5\,\text{V}$$

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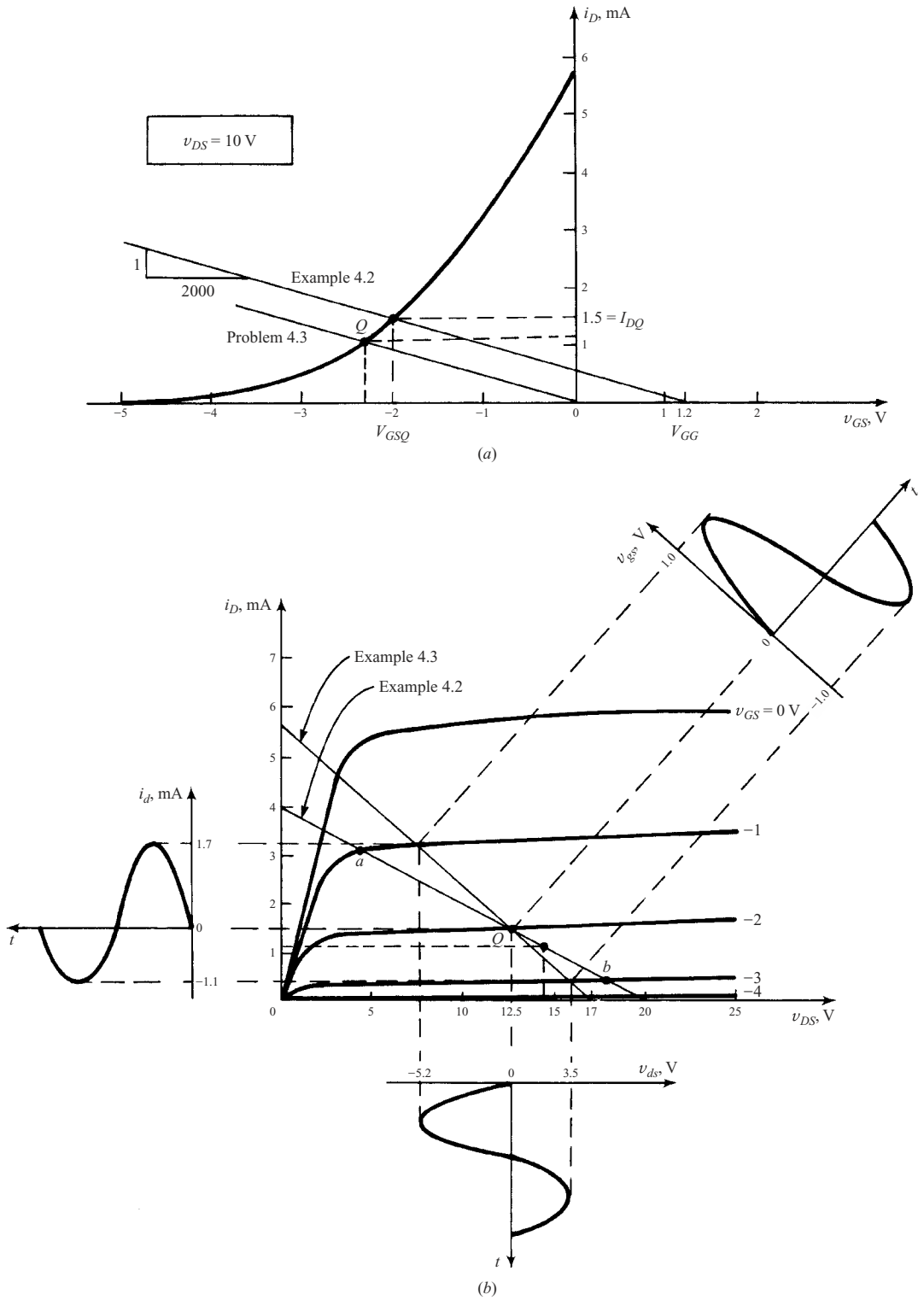


Fig. 4-6

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4.6. GRAPHICAL ANALYSIS FOR THE JFET

As is done in BJT circuits (Section 3.7), coupling (or blocking) capacitors are introduced to confine dc quantities to the JFET and its bias circuitry. Further, bypass capacitors C_S effectively remove the gain-reducing source resistor insofar as ac signals are concerned, while allowing R_S to be utilized in favorably setting the gate-source bias voltage; consequently, an ac load line is introduced with analysis techniques analogous to those of Section 3.7.

Graphical analysis is favored for large-ac-signal conditions in the JFET, since the square-law relationship between v_{GS} and i_D leads to signal distortion.

Example 4.3. For the amplifier of Example 4.2, let $v_i = \sin t(\omega = 1\,\text{rad/s})$ and $C_S \to \infty$. Graphically determine v_{ds} and i_d.

Since C_S appears as a short to ac signals, an ac load line must be added to Fig. 4-6(b), passing through the Q point and intersecting the v_{DS} axis at

$$V_{DSQ} + I_{DQ}R_{\text{ac}} = 12.5 + (1.5)(3) = 17\,\text{V}$$

We next construct an auxiliary time axis through Q, perpendicular to the ac load line, for the purpose of showing, on additional auxiliary axes as constructed in Fig. 4-6(b), the excursions of i_d and v_{ds} as $v_{gs} = v_i$ swings ± 1 V along the ac load line. Note the distortion in both signals, introduced by the square-law behavior of the JFET characteristics.

4.7. MOSFET CONSTRUCTION AND SYMBOLS

The n-channel MOSFET (Fig. 4-7) has only a single p region (called the *substrate*), one side of which acts as a conducting channel. A metallic gate is separated from the conducting channel by an insulating metal oxide (usually SiO_2), whence the name *insulated-gate* FET (IGFET) for the device. The p-channel MOSFET, formed by interchanging p and n semiconductor materials, is described by complementary voltages and currents.

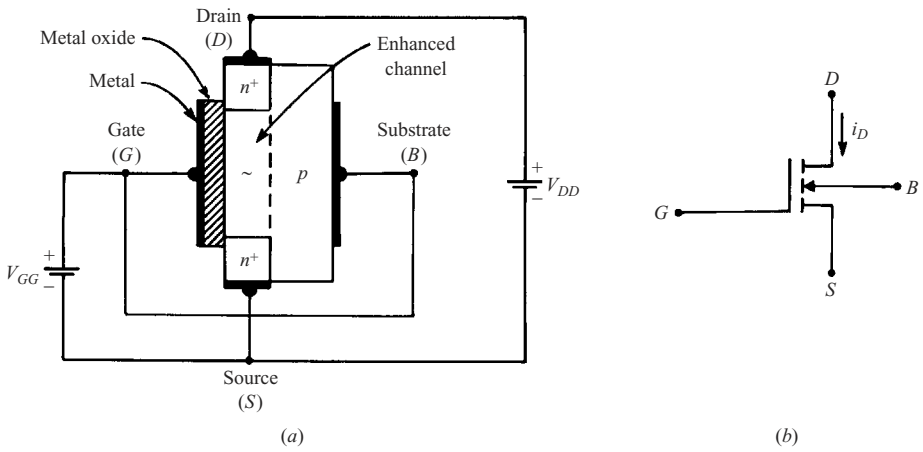


Fig. 4-7

4.8. MOSFET TERMINAL CHARACTERISTICS

In an n-channel MOSFET, the gate (positive plate), metal oxide film (dielectric), and substrate (negative plate) form a capacitor, the electric field of which controls channel resistance. When the positive potential of the gate reaches a *threshold voltage* V_T (typically 2 to 4 V), sufficient free electrons

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are attracted to the region immediately beside the metal oxide film (this is called *enhancement-mode* operation) to induce a conducting channel of low resistivity. If the source-to-drain voltage is increased, the enhanced channel is depleted of free charge carriers in the area near the drain, and pinchoff occurs as in the JFET. Typical drain and transfer characteristics are displayed in Fig. 4-8, where $V_T = 4\,\text{V}$ is used for illustration. Commonly, the manufacturer specifies V_T and a value of pinchoff current $I_{D\text{on}}$; the corresponding value of source-to-gate voltage is $V_{GS\text{on}}$.

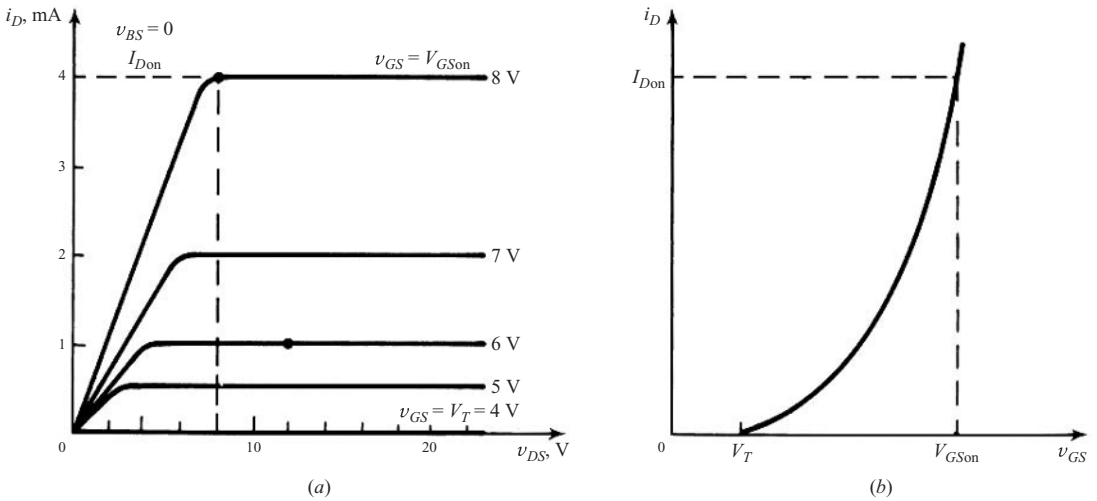


Fig. 4-8

The enhancement-mode MOSFET, operating in the pinchoff region, is described by (*4.1*) and (*4.2*) if V_{p0} and I_{DSS} are replaced with $-V_T$ and $I_{D\text{on}}$, respectively, and if the substrate is shorted to the source, as in Fig. 4-9(*a*). Then

$$i_D = I_{D\text{on}}\left(1 - \frac{v_{GS}}{V_T}\right)^2 \tag{4.6}$$

where $v_{GS} \geq V_T$.

Although the enhancement-mode MOSFET is the more popular (it is widely used in digital switching circuits), a *depletion-mode* MOSFET, characterized by a lightly doped channel between heavily doped source and drain electrode areas, is commercially available that can be operated like the JFET (see Problem 4.22). However, that device displays a gate-source input impedance several orders of magnitude smaller than that of the JFET.

4.9. MOSFET SPICE MODEL

The element specification statement for a MOSFET must explicitly assign a *model name* (an arbitrary selection of alpha and numeric characters) having the general form

$$\text{M}\cdots n_1\ n_2\ n_3\ n_4\ \textit{model name}$$

Nodes n_1, n_2, n_3, and n_4 belong to the drain, gate, source, and substrate, respectively. Only the *n*-channel MOSFET is addressed where the device positive voltage and current directions are clarified by Fig. 4-10.

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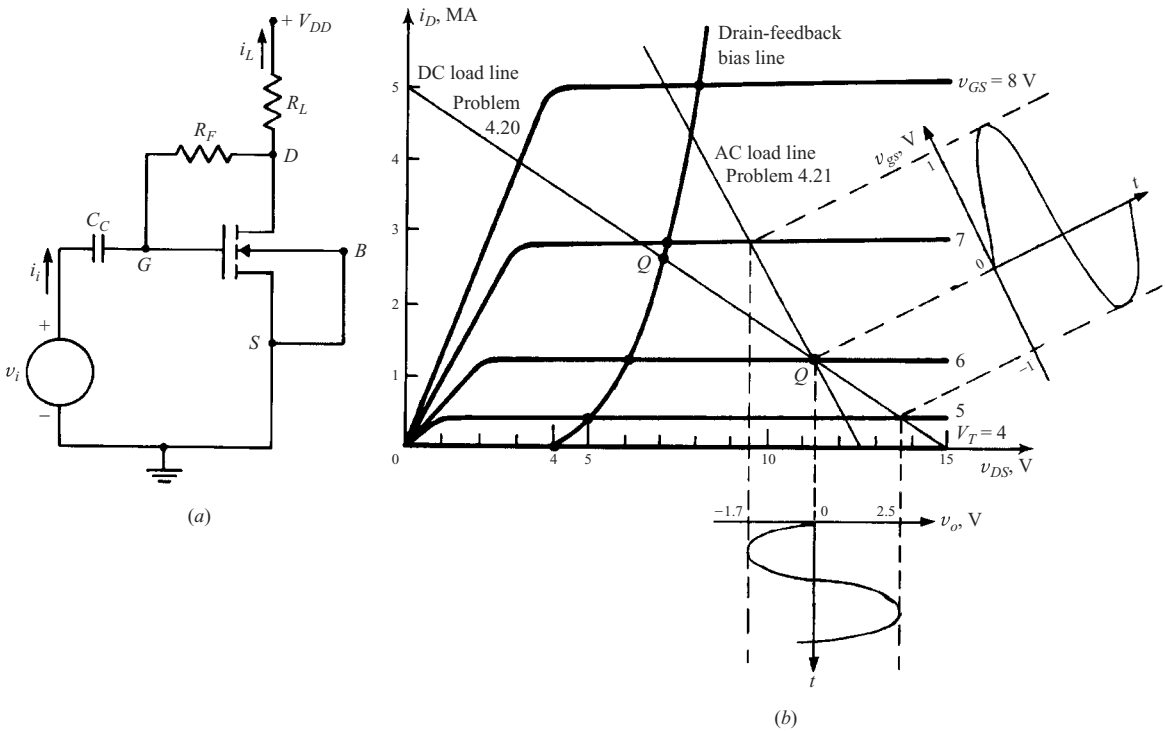


Fig. 4-9

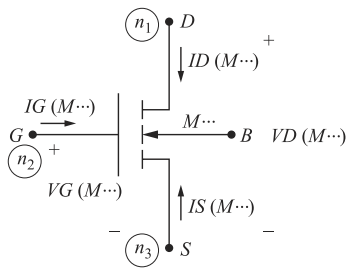


Fig. 4-10

Format of the .MODEL control statement that must appear in the netlist code for a MOSFET circuit is as follows:

.MODEL *model name* NMOS (*parameters*)

A blank parameter field results in assignment of default parameter values. Nondefault parameters are entered in the parameter field as *parameter name* = *value*. The specific parameters of concern in this book are documented by Table 4-3. The SPICE model characterizes the enhancement mode MOSFET in the pinchoff region by

$$i_D = \frac{I_{D\text{on}}}{V_T^2}(v_{GS} - V_T)^2 = \frac{Kp}{2}(v_{GS} - V_T)^2$$

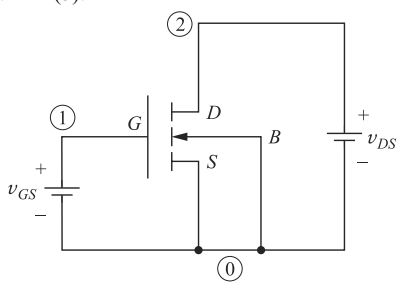
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Table 4-3

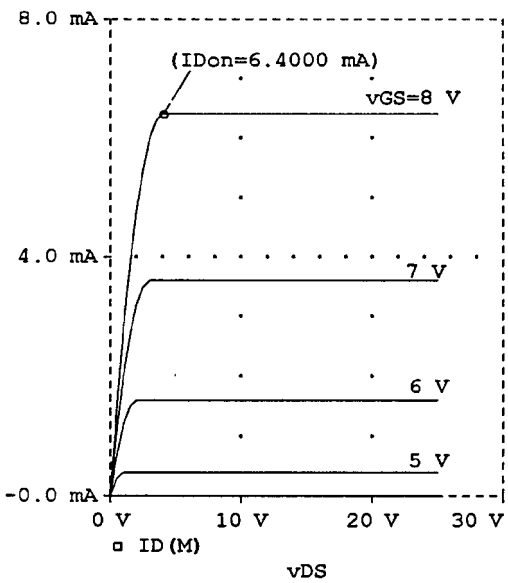
Parameter	Description	Default	Units
Vto	Threshold voltage	0	V
Kp	Transcond. coeff.	2×10^{-5}	A/V^2
Rd	Drain resistance	0	Ω
Rg	Gate resistance	0	Ω

Example 4.4. Use SPICE methods to generate (*a*) the CS drain characteristics and (*b*) the transfer characteristic for an *n*-channel MOSFET that has the parameter values Vto = 4 V, Kp = 0.0008 A/V^2, Rd = 1 Ω, and Rg = 1 kΩ.

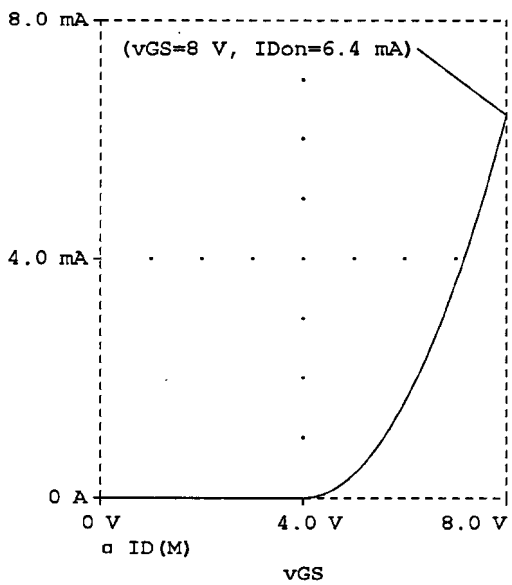
(*a*) Figure 4-11(*a*) shows the chosen connection method for measurement of both the drain characteristics and the transfer characteristic. The netlist code below generates the drain characteristic that has been plotted using the Probe feature of PSpice as Fig. 4-11(*b*).



(*a*)



(*b*)



(*c*)

Fig. 4-11

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```
Ex4_4a.CIR - MOSFET drain characteristics
vGS 1 0 0V
vDS 2 0 0V
M 2  1 0 0 NMOSG
.MODEL NMOSG NMOS (Vto=4V Kp=0.0008ApVsq
+ Rd=1ohm Rg=1kohm)
.DC vDS 0V 25V 0.5V vGS 0V 8V 1V
.PROBE
.END
```

(*b*) The following netlist code maintains v_{DS} constant to determine the transfer characteristic that is plotted by use of Probe as Fig. 4-11(*c*).

```
Ex4_4b.CIR - MOSFET transfer characteristic
vGS 1 0 0V
vDS 2 0 15V
M 2  1 0 0 NMOSG
.MODEL NMOSG NMOS (Vto=4V Kp=0.0008ApVsq
+ Rd=1ohm Rg=1kohm)
.DC vGS 0V 8V 0.1V
.PROBE
.END
```

4.10. MOSFET BIAS AND LOAD LINES

Although the transfer characteristic of the MOSFET differs from that of the JFET [compare Fig. 4-2(*b*)] with Figs. 4-8(*b*) and 4-27], simultaneous solution with the transfer bias line (*4.4*) allows determination of the gate-source bias V_{GSQ}. Further, graphical procedures in which dc and ac load lines are constructed on drain characteristics can be utilized with both enhancement-mode and depletion-mode MOSFETS.

The voltage-divider bias arrangement (Fig. 4-5) is readily applicable to the enhancement-mode MOSFET; however, since V_{GSQ} and V_{DSQ} are of the same polarity, *drain-feedback bias*, illustrated in Fig. 4-9(*a*), can be utilized to compensate partially for variations in MOSFET characteristics.

Example 4.5. In the amplifier of Fig. 4-9(*a*), $V_{DD} = 15\,\text{V}$, $R_L = 3\,\text{k}\Omega$, and $R_F = 50\,\text{M}\Omega$. If the MOSFET drain characteristics are given by Fig. 4-9(*b*), determine the values of the quiescent quantities.

The dc load line is constructed on Fig. 4-9(*b*) with v_{DS} intercept of $V_{DD} = 15\,\text{V}$ and i_D intercept of $V_{DD}/R_L = 5\,\text{mA}$. With gate current negligible (see Section 4.3), no voltage appears across R_F, and so $V_{GS} = V_{DS}$. The *drain-feedback bias line* of Fig. 4-9(*b*) is the locus of all points for which $V_{GS} = V_{DS}$. Since the Q point must lie on both the dc load line and the drain-feedback bias line, their intersection is the Q point. From Fig. 4-9(*b*), $I_{DQ} \approx 2.65\,\text{mA}$ and $V_{DSQ} = V_{GSQ} \approx 6.90\,\text{V}$.

Example 4.6. The drain-feedback biased amplifier of Fig. 4-9(*a*) has the circuit element values of Example 4.5 except that the MOSFET is characterized by the parameter values of Example 4.4. Apply SPICE methods to determine the quiescent values.

The netlist code below describes the circuit.

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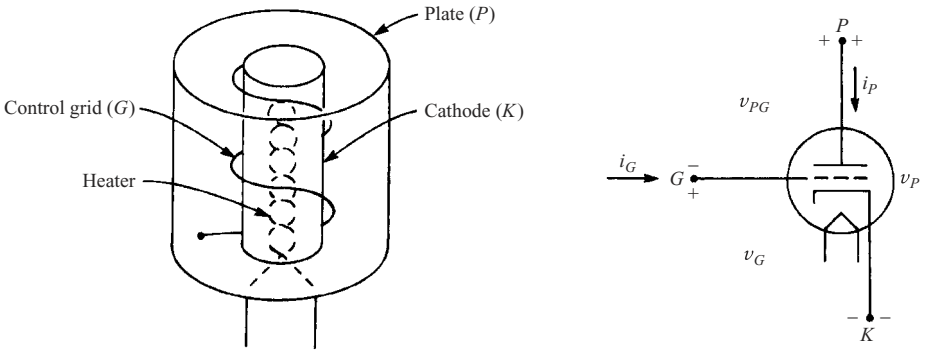
```
Ex4_6.CIR - Drain-feedback bias
vi  1 0 0V ; Value inconsequential
CC  1 2 100uF; Value inconsequential
RF  2 3 50MEGohm
RL  3 4 3kohm
VDD 4 0 15V
M 3  2 0 0 NMOSG
.MODEL NMOSG NMOS (Vto=4V Kp=0.0008ApVsq
+ Rd=1ohm Rg=1kohm)
.DC VDD 15V 15V 1V
.PRINT DC ID(M) V(2) V(3)
.PROBE
.END
```

Execute ⟨Ex4_6.CIR⟩ and poll the output file to find $I_{DQ} = \text{ID(M)} = 2.79\,\text{mA}$, $V_{DSQ} = \text{V(3)} = V_{GSQ} = \text{V(2)} = 6.64\,\text{V}$.

4.11. TRIODE CONSTRUCTION AND SYMBOLS

A *vacuum tube* is an evacuated enclosure containing (1) a *cathode* that emits electrons, with a *heater* used to elevate the cathode temperature to a level at which thermionic emission occurs; (2) an *anode* or *plate* that attracts the emitted electrons when operated at a positive potential relative to the cathode; and usually (3) one or more intermediate electrodes (called *grids*) that modify the emission-attraction process. Analogous to FETS, the voltage applied to the grids controls current flowing into the plate lead.

The single grid of the *vacuum triode* is called the *control grid*; it is made of small-diameter wire and inserted between the plate and cathode as suggested in Fig. 4-12(*a*). The mesh of the grid is sufficiently coarse so as not to impede current flow from plate to cathode through collision of electrons with the grid wire; moreover, the grid is placed physically close to the cathode so that its electric field can exert considerable control over electron emission from the cathode surface. The symbols for the total instantaneous currents and voltages of the triode are shown in Fig. 4-12(*b*); component, average, rms, and maximum values are symbolized as in Table 3-1.



(*a*) (*b*)

Fig. 4-12

4.12. TRIODE TERMINAL CHARACTERISTICS AND BIAS

The voltage-current characteristics of the triode are experimentally determined with the cathode sharing a common connection with the input and output ports. If plate voltage v_P and grid voltage v_G

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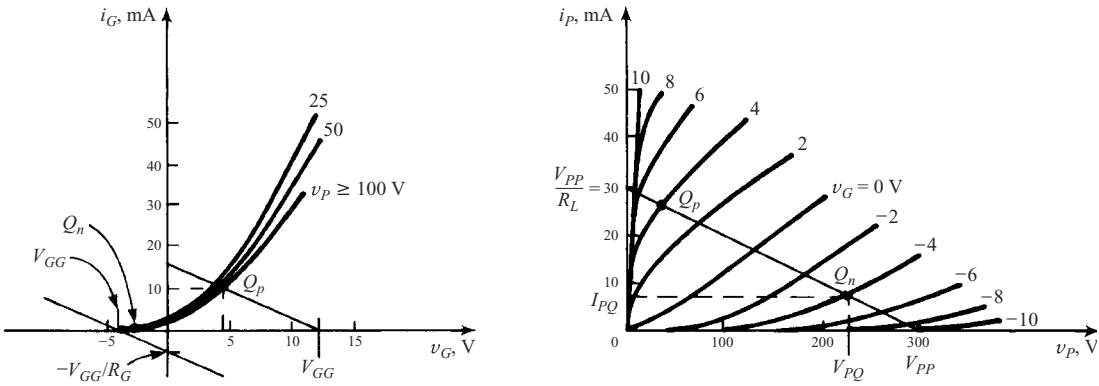
are taken as independent variables, and grid current i_G as the dependent variable, then the *input characteristics* (or *grid characteristics*) have the form

$$i_G = f_1(v_P, v_G) \tag{4.7}$$

of which Fig. 4-13(*a*) is a typical experimentally determined plot. Similarly, with v_P and v_G as independent variables, the plate current i_P becomes the dependent variable of the *output characteristics* (or *plate characteristics*)

$$i_P = f_2(v_P, v_G) \tag{4.8}$$

of which a typical plot is displayed in Fig. 4-13(*b*).



(*a*) Grid characteristics (*b*) Plate characteristics

Fig. 4-13

The triode input characteristics of Fig. 4-13(*a*) show that operation with a positive grid voltage results in flow of grid current; however, with a negative grid voltage (the common application), negligible grid current flows and the plate characteristics are reasonably approximated by a three-halves-power relationship involving a linear combination of plate and grid voltages:

$$i_P = \kappa(v_P + \mu v_G)^{3/2} \tag{4.9}$$

where κ denotes the *perveance* (a constant that depends upon the mechanical design of the tube) and μ is the *amplification factor*, a constant whose significance is elucidated in Chapter 7 when small-signal amplification of the triode is addressed.

To establish a range of triode operation favorable to the signal to be amplified, a quiescent point must be determined by dc bias circuitry. The basic triode amplifier of Fig. 4-14 has a grid power supply V_{GG} of such polarity as to maintain v_G negative (the more common mode of operation). With no input signal ($v_S = 0$), application of KVL around the grid loop of Fig. 4-14 yields the equation of the *grid bias line*,

$$i_G = -\frac{V_{GG}}{R_G} - \frac{v_G}{R_G} \tag{4.10}$$

which can be solved simultaneously with (4.7) or plotted as indicated on Fig. 4-13(*a*) to determine the quiescent values I_{GQ} and V_{GQ}. If V_{GG} is of the polarity indicated in Fig. 4-14, the grid is negatively biased, giving the Q point labeled Q_n. At that point, $I_{GQ} \approx 0$ and $V_{GQ} \approx -V_{GG}$; these approximate solutions suffice in the case of negative grid bias. However, if the polarity of V_{GG} were reversed, the grid would have a positive bias, and the quiescent point Q_p would give $I_{GQ} > 0$ and $V_{GQ} < V_{GG}$.

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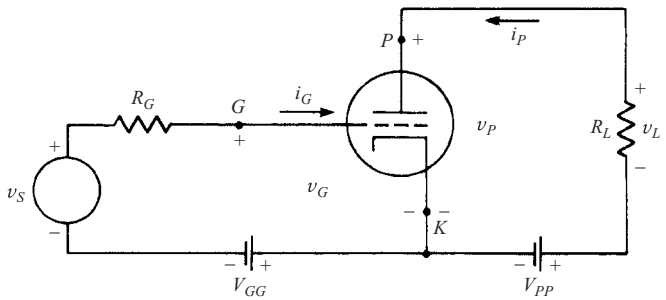


Fig. 4-14 Basic triode amplifier

Voltage summation around the plate circuit of Fig. 4-14 leads to the equation of the *dc load line*

$$i_P = \frac{V_{PP}}{R_L} - \frac{v_P}{R_L} \tag{4.11}$$

which, when plotted on the plate characteristics of Fig. 4-13(*b*), yields the quiescent values V_{PQ} and I_{PQ} at its intersection with the curve $v_G = V_{GQ}$.

Example 4.7. In the triode amplifier of Fig. 4-14, $V_{GG} = 4\,\text{V}$, $V_{PP} = 300\,\text{V}$, $R_L = 10\,\text{k}\Omega$, and $R_G = 2\,\text{k}\Omega$. The plate characteristics for the triode are given by Fig. 4-13(*b*). (*a*) Draw the dc load line; then determine the quiescent values (*b*) I_{GQ}, (*c*) V_{GQ}, (*d*) I_{PQ}, and (*e*) V_{PQ}.

(*a*) For the given values, the dc load line (*4.11*) has the i_P intercept

$$\frac{V_{PP}}{R_L} = \frac{300}{10 \times 10^3} = 30\,\text{mA}$$

and the v_P intercept $V_{PP} = 300\,\text{V}$. These intercepts have been utilized to draw the dc load line on the plate characteristics of Fig. 4-13(*b*).

(*b*) Since the polarity of V_{GG} is such that v_G is negative, negligible grid current will flow ($I_{GQ} \approx 0$).

(*c*) For negligible grid current, (*4.10*) evaluated at the Q point yields $V_{GQ} = -V_{GG} = -4\,\text{V}$.

(*d*) The quiescent plate current is read as the projection of Q_n onto the i_P axis of Fig. 4-13(*b*) and is $I_{PQ} = 8\,\text{mA}$.

(*e*) Projection of Q_n onto the v_P axis of Fig. 4-13(*b*) gives $V_{PQ} = 220\,\text{V}$.

Solved Problems

4.1 If $C_S = 0$ and all else is unchanged in Example 4.2, find the extremes between which v_S swings.

Voltage v_{gs} will swing along the dc load line of Fig 4-6(*b*) (which is now identical to the ac load line) from point *a* to point *b*, giving, as extremes of i_D, 3.1 mA and 0.4 mA. The corresponding extremes of $v_S = i_D R_S$ are 6.2 V and 0.8 V.

4.2 For the MOSFET amplifier of Example 4.5, let $V_{GSQ} = 6.90\,\text{V}$. Calculate I_{DQ} from the analog of (*4.2*) developed in Section 4.8.

From the drain characteristics of Fig. 4-9(*b*), we see that $V_T = 4\,\text{V}$ and that $I_{D\text{on}} = 5\,\text{mA}$ at $V_{GS\text{on}} = 8\,\text{V}$. Thus,

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$$I_{DQ} = I_{Don}\left(1 - \frac{V_{GSQ}}{V_T}\right)^2 = 5 \times 10^{-3}\left(1 - \frac{6.90}{4}\right)^2 = 2.63\,\text{mA}$$

(Compare Example 4.5.)

4.3 By a method called *self-bias*, the Q point of a JFET amplifier may be established using only a single resistor from gate to ground [Fig. 4-5(b) with $V_{GG} = 0$]. If $R_D = 3\,\text{k}\Omega$, $R_S = 2\,\text{k}\Omega$, $R_G = 5\,\text{M}\Omega$, and $V_{DD} = 20\,\text{V}$ in Fig. 4-5(b), and the JFET characteristics are given by Fig. 4-6, find (a) I_{DQ}, (b) V_{GSQ}, and (c) V_{DSQ}.

(a) On Fig. 4-6(a) we construct a transfer bias line having a v_{GS} intercept of $V_{GG} = 0$ and a slope of $-1/R_S = -0.5\,\text{mS}$; the ordinate of its intersection with the transfer characteristic is $I_{DQ} = 1.15\,\text{mA}$.

(b) The abscissa of the Q point of Fig. 4-6(a) is $V_{GSQ} = -2.3\,\text{V}$.

(c) The dc load line from Example 4.2, already constructed on Fig. 4-6(b), is applicable here. The Q point was established at $I_{DQ} = 1.15\,\text{mA}$ in (a); the corresponding abscissa is $V_{DSQ} \approx 14.2\,\text{V}$.

4.4 Work Problem 4.3, except with the JFET described by the parameter values of Example 4.1, using SPICE methods to illustrate the ease with which quiescent values for a JFET circuit can be determined.

The netlist code below describes the circuit of Fig. 4-5(b) with $V_{GG} = 0$.

```
Prb4_4.CIR - Self-bias
RG  1 0 5MEGohm ; VGG not used
RS  2 0 2kohm
RD  3 4 3kohm
VDD 4 0 20V
J 3  1 2 NJFET
.MODEL NJFET NJF( Vto=-4V Beta=0.0005ApVsq
+ Rd=1ohm Rs=1ohm CGS=2pF CGD=2pF)
.DC VDD 20V 20V 1V
.PRINT DC ID(J) V(1,2) V(3,2)
.END
```

Execute <Prb4_4.CIR> and examine the output file to find (a) $I_{DQ} = \text{ID}(J) = 1.22\,\text{mA}$, ($b$) $V_{GSQ} = \text{V}(1, 2) = -2.44\,\text{V}$, and ($c$) $V_{DSQ} = \text{V}(3, 2) = 13.9\,\text{V}$.

4.5 Replace the JFET of Fig. 4-5 with an n-channel enhancement-mode MOSFET characterized by Fig. 4-8. Let $V_{DD} = 16\,\text{V}$, $V_{GSQ} = 8\,\text{V}$, $V_{DSQ} = 12\,\text{V}$, $I_{DQ} = 1\,\text{mA}$, $R_1 = 5\,\text{M}\Omega$, and $R_2 = 3\,\text{M}\Omega$. Find (a) V_{GG}, (b) R_S, and (c) R_D.

(a) By (*4.3*), $V_{GG} = R_1 V_{DD}/(R_1 + R_2) = 10\,\text{V}$.

(b) Application of KVL around the smaller gate-source loop of Fig. 4-5(b) with $i_G = 0$ leads to

$$R_S = \frac{V_{GG} - V_{GSQ}}{I_{DQ}} = \frac{10 - 8}{1 \times 10^{-3}} = 2\,\text{k}\Omega$$

(c) Using KVL around the drain-source loop of Fig. 4-5(b) and solving for R_D yield

$$R_D = \frac{V_{DD} - V_{DSQ} - I_{DQ}R_S}{I_{DQ}} = \frac{16 - 12 - (1 \times 10^{-3})(2 \times 10^3)}{1 \times 10^{-3}} = 2\,\text{k}\Omega$$

4.6 The JFET amplifier of Fig. 4-15 shows a means of self-bias that allows extremely high input impedance even if low values of gate-source bias voltage are required. Find the Thévenin equivalent voltage and resistance for the network to the left of a, b.

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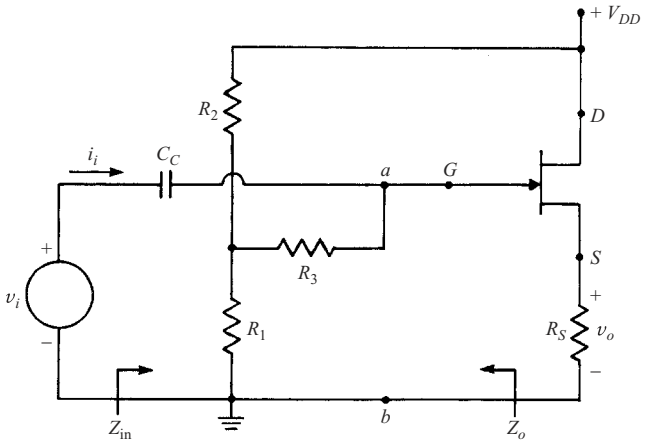


Fig. 4-15

With a, b open there is no voltage drop across R_3, and the voltage at the open-circuited terminals is determined by the R_1-R_2 voltage divider:

$$v_{Th} = V_{GG} = \frac{R_1}{R_1 + R_2} V_{DD}$$

With V_{DD} deactivated (shorted), the resistance to the left of a, b is

$$R_{Th} = R_G = R_3 + \frac{R_1 R_2}{R_1 + R_2}$$

It is apparent that if R_3 is made large, then $R_G = Z_{\text{in}}$ is large regardless of the values of R_1 and R_2.

4.7 The manufacturer's specification sheet for a certain kind of *n*-channel JFET has nominal and worst-case shorted-gate parameters as follows:

Value	I_{DSS}, mA	V_{p0}, V
maximum	7	4.2
nominal	6	3.6
minimum	5	3.0

Sketch the nominal and worst-case transfer characteristics that can be expected from a large sample of the device.

Values can be calculated for the nominal, maximum, and minimum transfer characteristics using (*4.2*) over the range $-V_{p0} \le v_{GS} \le 0$. The results are plotted in Fig. 4-16.

4.8 A self-biased JFET amplifier (Fig. 4-15) is to be designed with $V_{DSQ} = 15\,\text{V}$ and $V_{DD} = 24\,\text{V}$, using a device as described in Problem 4.7. For the control of gain variation, the quiescent drain current must satisfy $I_{DQ} = 2 \pm 0.4\,\text{mA}$ regardless of the particular parameters of the JFET utilized. Determine appropriate values of R_S and R_D.

Quiescent points are first established on the transfer characteristics of Fig. 4-16: $Q_{\max}$ at $I_{DQ} = 2.4\,\text{mA}$, Q_{nom} at $I_{DQ} = 2.0\,\text{mA}$, and $Q_{\min}$ at $I_{DQ} = 1.6\,\text{mA}$. A transfer bias line is then constructed to pass through the origin (i.e., we choose $V_{GG} = 0$) and Q_{nom}. Since its slope is $-1/R_S$, the source resistor value may be determined as

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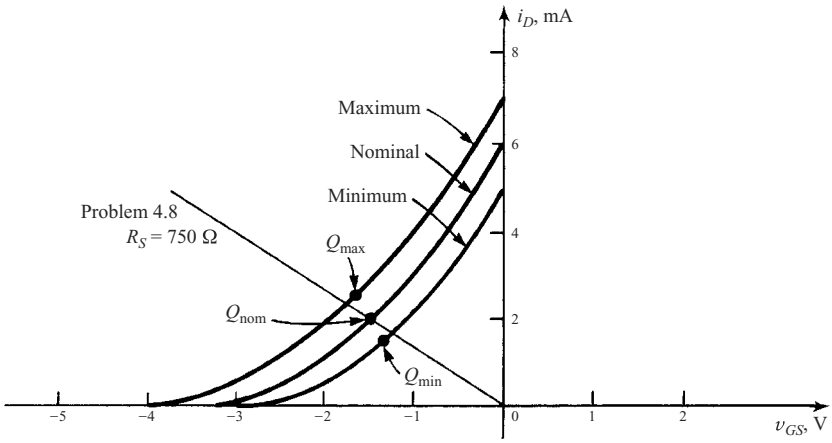


Fig. 4-16

$$R_S = \frac{0-(-3)}{(4-0)\times 10^{-3}} = 750\,\Omega$$

The drain resistor value is found by applying KVL around the drain-source loop and solving for R_D:

$$R_D = \frac{V_{DD} - V_{DSQ} - I_{DQ}R_S}{I_{DQ}} = \frac{24 - 15 - (0.002)(750)}{0.002} = 3.75\,\text{k}\Omega$$

When R_S and R_D have these values, the condition on I_{DQ} is satisfied.

4.9 An *n*-channel JFET has worst-case shorted-gate parameters given by the manufacturer as follows:

Value	I_{DSS}, mA	V_{p0}, V
maximum	8	6
minimum	4	3

If the JFET is used in the circuit of Fig. 4-5(*b*), where $R_S = 0$, $R_G = 1\,\text{M}\Omega$, $R_D = 2.2\,\text{k}\Omega$, $V_{GG} = -1\,\text{V}$, and $V_{DD} = 15\,\text{V}$, use SPICE methods to find the maximum and minimum values of I_{DQ} and the maximum and minimum values of V_{DSQ} that could be expected. Model the JFET by default parameters except for Vto and Beta.

The netlist code below describes the circuit.

```
Prb4_9.CIR - Worst-case study
.PARAM Vpo=-3V, Ion=8mA
RG  1 5 1MEGohm
VGG 5 0 -1V
RD  3 4 2.2kohm
VDD 4 0 15V
J 3  1 0 NJFET ; RS not used
.MODEL NJFET NJF( Vto={Vpo} Beta={Ion/Vpo^2} )
.DC PARAM Vpo -3V -6V 3V PARAM Ion 4mA 8mA 4mA
.PRINT DC ID(J) V(3)
.END
```

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Execute ⟨Prb4_9.CIR⟩ and examine the output file to find the two pairs of values

$$I_{DQ\,\min} = 1.78\,\text{mA}, \qquad V_{DSQ\,\max} = 11.09\,\text{V}$$
$$I_{DQ\,\max} = 5.15\,\text{mA}, \qquad V_{DSQ\,\min} = 3.66\,\text{V}$$

4.10 Gate current is negligible for the *p*-channel JFET of Fig. 4-17. If $V_{DD} = -20\,\text{V}$, $I_{DSS} = -10\,\text{mA}$, $I_{DQ} = -8\,\text{mA}$, $V_{p0} = -4\,\text{V}$, $R_S = 0$, and $R_D = 1.5\,\text{k}\Omega$, find (*a*) V_{GG} and (*b*) V_{DSQ}.

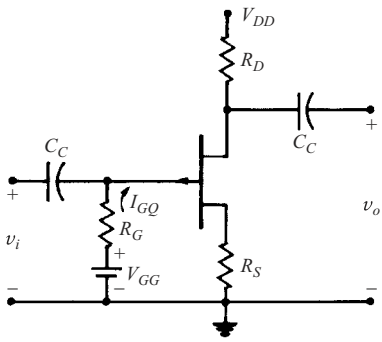


Fig. 4-17

(*a*) Solving (*4.2*) for v_{GS} and substituting *Q*-point conditions yield

$$V_{GSQ} = V_{p0}\left[\left(\frac{I_{DQ}}{I_{DSS}}\right)^{1/2} - 1\right] = -4\left[\left(\frac{-8}{-10}\right)^{1/2} - 1\right] = 0.422\,\text{V}$$

With negligible gate current, KVL requires that $V_{GG} = V_{GSQ} = 0.422\,\text{V}$.

(*b*) Applying KVL around the drain-source loop gives

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = (-20) - (-8 \times 10^{-3})(1.5 \times 10^{3}) = -8\,\text{V}$$

4.11 The *n*-channel enhancement-mode MOSFET of Fig. 4-18 is characterized by $V_T = 4\,\text{V}$ and $I_{D\text{on}} = 10\,\text{mA}$. Assume negligible gate current, $R_1 = 50\,\text{k}\Omega$, $R_2 = 0.4\,\text{M}\Omega$, $R_S = 0$, $R_D = 2\,\text{k}\Omega$, and $V_{DD} = 15\,\text{V}$. Find (*a*) V_{GSQ}, (*b*) I_{DQ}, and (*c*) V_{DSQ}.

(*a*) With negligible gate current, (*4.3*) leads to

$$V_{GSQ} = V_{GG} = \frac{R_2}{R_2 + R_1}V_{DD} = \frac{50 \times 10^{3}}{50 \times 10^{3} + 0.4 \times 10^{6}}\,15 = 1.67\,\text{V}$$

(*b*) By (*4.6*),

$$I_{DQ} = I_{D\text{on}}\left(1 - \frac{V_{GSQ}}{V_T}\right)^2 = 10 \times 10^{-3}\left(1 - \frac{1.67}{4}\right)^2 = 3.39\,\text{mA}$$

(*c*) By KVL around the drain-source loop,

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 15 - (3.39 \times 10^{-3})(2 \times 10^{3}) = 8.22\,\text{V}$$

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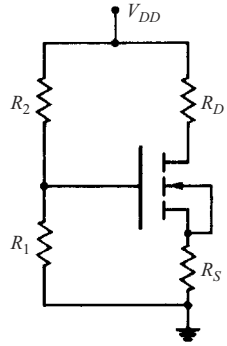


Fig. 4-18

4.12 For the *n*-channel enhancement-mode MOSFET of Fig. 4-18, gate current is negligible, $I_{Don} = 10\,\text{mA}$, and $V_T = 4\,\text{V}$. If $R_S = 0$, $R_1 = 50\,\text{k}\Omega$, $V_{DD} = 15\,\text{V}$, $V_{GSQ} = 3\,\text{V}$, and $V_{DSQ} = 9\,\text{V}$, determine the values of (*a*) R_1 and (*b*) R_D.

(*a*) Since $i_G = 0$, $V_{GSQ} = V_{GG}$ of (*4.3*). Solving for R_2 gives

$$R_2 = R_1\left(\frac{V_{DD}}{V_{GSQ}} - 1\right) = 50 \times 10^3\left(\frac{15}{3} - 1\right) = 200\,\text{k}\Omega$$

(*b*) By (*4.6*),

$$I_{DQ} = I_{Don}\left(1 - \frac{V_{GSQ}}{V_T}\right)^2 = 10 \times 10^{-3}\left(1 - \frac{3}{4}\right)^2 = 0.625\,\text{mA}$$

Then KVL around the drain-source loop requires that

$$R_D = \frac{V_{DD} - V_{DSQ}}{I_{DQ}} = \frac{15 - 9}{0.625 \times 10^{-3}} = 9.6\,\text{k}\Omega$$

4.13 A *p*-channel MOSFET operating in the enhancement mode is characterized by $V_T = -3\,\text{V}$ and $I_{DQ} = -8\,\text{mA}$ when $V_{GSQ} = -4.5\,\text{V}$. Find (*a*) V_{GSQ} if $I_{DQ} = -16\,\text{mA}$ and (*b*) I_{DQ} if $V_{GSQ} = -5\,\text{V}$.

(*a*) Using the given data in (*4.6*) leads to

$$I_{Don} = \frac{I_{DQ}}{(1 - V_{GSQ}/V_T)^2} = \frac{-8 \times 10^{-3}}{(1 - (-4.5) - 3)^2} = -32\,\text{mA}$$

Rearrangement of (*4.6*) now allows solution for V_{GSQ}:

$$V_{GSQ} = V_T\left[1 - \left(\frac{I_{DQ}}{I_{Don}}\right)^{1/2}\right] = (-3)\left[1 - \left(\frac{-16}{-32}\right)^{1/2}\right] = -0.88\,\text{V}$$

(*b*) By (*4.6*),

$$I_{DQ} = I_{Don}\left(1 - \frac{V_{GSQ}}{V_T}\right)^2 = -32 \times 10^{-3}\left(1 - \frac{-5}{-3}\right)^2 = -14.22\,\text{mA}$$

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4.14 The *n*-channel JFET circuit of Fig. 4-19 employs one of several methods of self-bias. (*a*) Assume negligible gate leakage current ($i_G \approx 0$), and show that if $V_{DD} > 0$, then $V_{GSQ} < 0$, and hence the device is properly biased. (*b*) If $R_D = 3\,\text{k}\Omega$, $R_S = 1\,\text{k}\Omega$, $V_{DD} = 15\,\text{V}$, and $V_{DSQ} = 7\,\text{V}$, find I_{DQ} and V_{GSQ}.

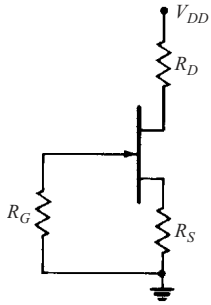


Fig. 4-19

(*a*) By KVL,

$$I_{DQ} = \frac{V_{DD} - V_{DSQ}}{R_S + R_D} \tag{1}$$

Now $V_{DSQ} < V_{DD}$, so it is apparent that $I_{DQ} > 0$. Since $i_G \approx 0$, KVL around the gate-source loop gives

$$V_{GSQ} = -I_{DQ}R_S < 0 \tag{2}$$

(*b*) By (*1*),

$$I_{DQ} = \frac{15 - 7}{3 \times 10^3 + 1 \times 10^3} = 2\,\text{mA}$$

and (*2*),

$$V_{GSQ} = -(2 \times 10^{-3})(1 \times 10^3) = -2\,\text{V}$$

4.15 The *n*-channel JFET of Fig. 4-20 is characterized by $I_{DSS} = 5\,\text{mA}$ and $V_{p0} = 3\,\text{V}$. Let $R_D = 3\,\text{k}\Omega$, $R_S = 8\,\text{k}\Omega$, $V_{DD} = 15\,\text{V}$, and $V_{SS} = -8\,\text{V}$. Find V_{GSQ} and V_0 (*a*) if $V_G = 0$ and (*b*) if $V_G = 10\,\text{V}$.

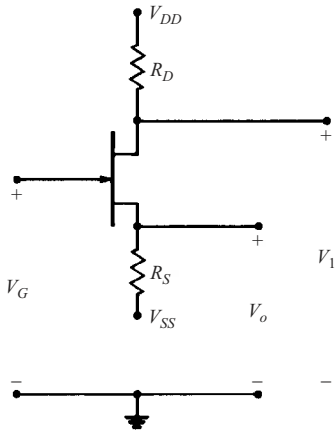


Fig. 4-20

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(*a*) Applying KVL around the gate-source loop yields

$$V_G = V_{GSQ} + R_S I_{DQ} + V_{SS} \tag{1}$$

Solving (*1*) for I_{DQ} and equating the result to the right side of (*4.2*) gives

$$\frac{V_G - V_{GSQ} - V_{SS}}{R_S} = I_{DSS}\left(1 + \frac{V_{GSQ}}{V_{p0}}\right)^2 \tag{2}$$

Rearranging (*2*) leads to the following quadratic in V_{GSQ}:

$$V_{GSQ}^2 + V_{p0}\frac{V_{p0} + 2I_{DSS}R_S}{I_{DSS}R_S}V_{GSQ} + \frac{V_{p0}^2}{I_{DSS}R_S}(I_{DSS}R_S - V_G + V_{SS}) = 0 \tag{3}$$

Substituting known values into (*3*) and solving for V_{GSQ} with the quadratic formula lead to

$$V_{GSQ}^2 + 3\frac{3 + (2)(5\times10^{-3})(8\times10^{-3})}{(5\times10^{-3})(8\times10^{3})}V_{GSQ} + \frac{(3)^2}{(5\times10^{-3})(8\times10^{3})}[(5\times10^{-3})(8\times10^{3}) - 0 - 8] = 0$$

so that

$$V_{GSQ}^2 + 6.225V_{GSQ} + 7.2 = 0$$

and $V_{GSQ} = -4.69\,\text{V}$ or $-1.53\,\text{V}$. Since $V_{GSQ} = -4.69\,\text{V} < -V_{p0}$, this value must be considered extraneous as it will result in $i_D = 0$. Hence, $V_{GSQ} = -1.53\,\text{V}$. Now, from (*4.2*),

$$I_{DQ} = I_{DSS}\left(1 + \frac{V_{GSQ}}{V_{p0}}\right)^2 = 5\times10^{-3}\left(1 + \frac{-1.53}{3}\right)^2 = 1.2\,\text{mA}$$

and, by KVL,

$$V_0 = I_{DQ}R_S + V_{SS} = (1.2\times10^{-3})(8\times10^{3}) + (-8) = 1.6\,\text{V}$$

(*b*) Substitution of known values into (*3*) leads to

$$V_{GSQ}^2 + 6.225V_{GSQ} + 4.95 = 0$$

which, after elimination of the extraneous root, results in $V_{GSQ} = -0.936\,\text{V}$. Then, as in part *a*,

$$I_{DQ} = I_{DSS}\left(1 + \frac{V_{GSQ}}{V_{p0}}\right)^2 = 5\times10^{-3}\left(1 + \frac{-0.936}{4}\right)^2 = 2.37\,\text{mA}$$

and

$$V_0 = I_{DQ}R_S + V_{SS} = (2.37\times10^{-3})(8\times10^{3}) + (-8) = 10.96\,\text{V}$$

4.16 Find the equivalent of the two identical *n*-channel JFETs connected in parallel in Fig. 4-21.

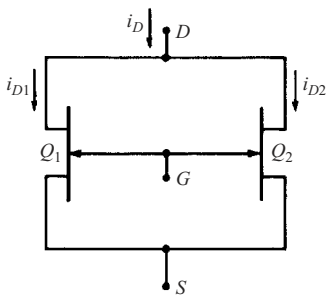


Fig. 4-21

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Assume the devices are described by (*4.2*); then

$$i_D = i_{D1} + i_{D2} = I_{DSS}\left(1 + \frac{v_{GS}}{V_{p0}}\right)^2 + I_{DSS}\left(1 + \frac{v_{GS}}{V_{p0}}\right)^2 = 2I_{DSS}\left(1 + \frac{v_{GS}}{V_{p0}}\right)^2$$

Because the two devices are identical and connected in parallel, the equivalent JFET has the same pinchoff voltage as the individual devices. However, it has a value of shorted-gate current I_{DSS} equal to twice that of the individual devices.

4.17 The differential amplifier of Fig. 4-22 includes identical JFETs with $I_{DSS} = 10\,\text{mA}$ and $V_{p0} = 4\,\text{V}$. Let $V_{DD} = 15\,\text{V}$, $V_{SS} = 5\,\text{V}$, and $R_S = 3\,\text{k}\Omega$. If the JFETs are described by (*4.2*), find the value of R_D required to bias the amplifier such that $V_{DSQ1} = V_{DSQ2} = 7\,\text{V}$.

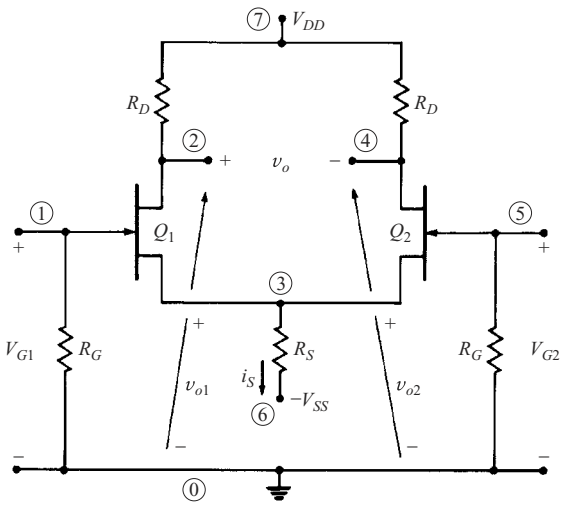


Fig. 4-22

By symmetry, $I_{DQ1} = I_{DQ2}$. KCL at the source node requires that

$$I_{SQ} = I_{DQ1} + I_{DQ2} = 2I_{DQ1} \tag{1}$$

With $i_{G1} = 0$, KVL around the left gate-source loop gives

$$V_{GSQ1} = V_{SS} - I_{SQ}R_S = V_{SS} - 2I_{DQ1}R_S \tag{2}$$

Solving (*4.2*) for V_{GSQ} and equating the result to the right side of (*2*) gives

$$V_{p0}\left[\left(\frac{I_{DQ1}}{I_{DSS}}\right)^{1/2} - 1\right] = V_{SS} - 2I_{DQ1}R_S \tag{3}$$

Rearranging (*3*) results in a quadratic in I_{DQ}:

$$I_{DQ1}^2 - \left[\frac{V_{SS} + V_{p0}}{R_S} + \left(\frac{V_{p0}}{2R_S}\right)^2 \frac{1}{I_{DSS}}\right] I_{DQ1} + \left(\frac{V_{SS} + V_{p0}}{2R_S}\right)^2 = 0 \tag{4}$$

Substituting known values into (*4*) yields

$$I_{DQ1}^2 - 3.04 \times 10^{-3} I_{DQ1} + 2.25 \times 10^{-6} = 0 \tag{5}$$

Applying the quadratic formula to (*5*) and disregarding the extraneous root yields $I_{DQ1} = 1.27\,\text{mA}$.

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Now the use of KVL around the left drain-source loop gives

$$V_{DD} + V_{SS} - V_{DSQ1} = I_{DQ1}R_D + I_{SQ}R_S \tag{6}$$

Substituting (*1*) into (*6*) and solving the result for R_D leads to the desired result:

$$R_D = \frac{V_{DD} + V_{SS} - V_{DSQ1} - 2I_{DQ1}R_S}{I_{DQ1}} = \frac{15 + 5 - 7 - 2(1.27 \times 10^{-3})(3 \times 10^3)}{1.27 \times 10^{-3}} = 4.20\,\text{k}\Omega$$

4.18 For the series-connected identical JFETs of Fig. 4-23, $I_{DSS} = 8\,\text{mA}$ and $V_{p0} = 4\,\text{V}$. If $V_{DD} = 15\,\text{V}$, $R_D = 5\,\text{k}\Omega$, $R_S = 2\,\text{k}\Omega$, and $R_G = 1\,\text{M}\Omega$, find (*a*) V_{DSQ1}, (*b*) I_{DQ1}, (*c*) V_{GSQ1}, (*d*) V_{GSQ2}, and (*e*) V_{DSQ2}.

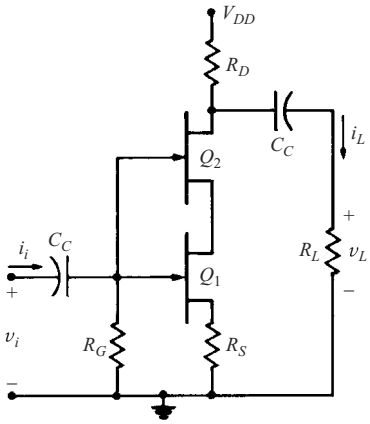


Fig. 4-23

(*a*) By KVL,

$$V_{GSQ1} = V_{GSQ2} + V_{DSQ1} \tag{1}$$

But, since $I_{DQ1} \equiv I_{DQ2}$, (*4.2*) leads to

$$I_{DSS}\left(1 + \frac{V_{GSQ1}}{V_{p0}}\right)^2 = I_{DSS}\left(1 + \frac{V_{GSQ2}}{V_{p0}}\right)^2$$

or,

$$V_{GSQ1} = V_{GSQ2} \tag{2}$$

Substitution of (*2*) into (*1*) yields $V_{DSQ1} = 0$.

(*b*) With negligible gate current, KVL applied around the lower gate-source loop requires that $V_{GSQ1} = -I_{DQ1}R_S$. Substituting into (*4.2*) and rearranging now give a quadratic in I_{DQ1}:

$$I_{DQ1}^2 - \left(\frac{V_{p0}}{R_S}\right)^2\left(\frac{1}{I_{DSS}} + \frac{2R_S}{V_{p0}}\right)I_{DQ1} + \left(\frac{V_{p0}}{R_S}\right)^2 = 0 \tag{3}$$

Substitution of known values gives

$$I_{DQ1}^2 - 4.5 \times 10^{-3} I_{DQ1} + 4 \times 10^{-6} = 0$$

from which we obtain $I_{DQ1} = 3.28\,\text{mA}$ and $1.22\,\text{mA}$. The value $I_{DQ1} = 3.28\,\text{mA}$ would result in $V_{GSQ1} < -V_{p0}$, so that value is extraneous. Hence, $I_{DQ1} = 1.22\,\text{mA}$.

(*c*)

$$V_{GSQ1} = -I_{DQ1}R_S = -(1.22 \times 10^{-3})(2 \times 10^3) = -2.44\,\text{V}$$

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(*d*) From (*1*) with $V_{DSQ1} = 0$, we have $V_{GSQ2} = V_{GSQ1} = -2.44\,\text{V}$.

(*e*) By KVL,

$$V_{DSQ2} = V_{DD} - V_{DSQ1} - I_{DQ1}(R_S + R_D) = 15 - 0 - (1.22 \times 10^{-3})(2 \times 10^3 + 5 \times 10^3) = 6.46\,\text{V}$$

4.19 Identical JFETs characterized by $i_G = 0$, $I_{DSS} = 10\,\text{mA}$, and $V_{p0} = 4\,\text{V}$ are connected as shown in Fig. 4-24. Let $R_D = 1\,\text{k}\Omega$, $R_S = 2\,\text{k}\Omega$, and $V_{DD} = 15\,\text{V}$, and find (*a*) V_{GSQ1}, (*b*) I_{DQ2}, (*c*) V_{GSQ2}, (*d*) V_{DSQ1}, and (*e*) V_{DSQ2}.

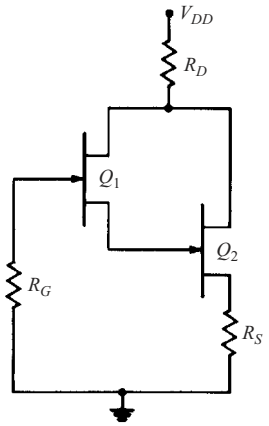


Fig. 4-24

(*a*) With negligible gate current, (*4.2*) gives

$$I_{G2} = I_{DQ1} = 0 = I_{DSS}\left(1 + \frac{V_{GSQ1}}{V_{p0}}\right)^2$$

so $$V_{GSQ1} = -V_{p0} = -4\,\text{V}$$

(*b*) With negligible gate current, KVL applied around the lower left-hand loop yields

$$V_{GSQ2} = -V_{GSQ1} - I_{DQ2}R_S \tag{1}$$

Substituting (*1*) into (*4.2*) and rearranging give

$$I_{DQ2}^2 - \left(\frac{V_{p0}}{R_S}\right)^2\left[\frac{1}{I_{DSS}} + 2\left(1 - \frac{V_{GSQ1}}{V_{p0}}\right)\frac{R_S}{V_{p0}}\right]I_{DQ2} + \left(\frac{V_{p0} - V_{GSQ1}}{R_S}\right)^2 = 0$$

which becomes, with known values substituted,

$$I_{DQ2}^2 - 8.4 \times 10^{-3} I_{DQ2} + 1.6 \times 10^{-5} = 0$$

The quadratic formula may be used to find the relevant root $I_{DQ2} = 2.92\,\text{mA}$.

(*c*) With negligible gate current, KVL leads to

$$V_{GSQ2} = -V_{GSQ1} - I_{DQ2}R_S = -(-4) - (2.92 \times 10^{-3})(2 \times 10^3) = -1.84\,\text{V}$$

(*d*) By KVL,

$$\begin{aligned} V_{DSQ1} &= V_{DD} - (I_{DQ1} + I_{DQ2})R_D - I_{DQ2}R_S - V_{GSQ2} \\ &= 15 - (0 + 2.92 \times 10^{-3})(1 \times 10^3) - (2.92 \times 10^{-3})(2 \times 10^3) - (-1.84) = 8.08\,\text{V} \end{aligned}$$

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(*e*) By KVL,

$$V_{DSQ2} = V_{DD} - (I_{DQ1} + I_{DQ2})R_D - I_{DQ2}R_S$$
$$= 15 - (0 + 2.92 \times 10^{-3})(1 \times 10^3) - (2.92 \times 10^{-3})(2 \times 10^3) = 6.24\,\text{V}$$

4.20 Fixed bias can also be utilized for the enhancement-mode MOSFET, as is illustrated by the circuit of Fig. 4-25. The MOSFET is described by the drain characteristic of Fig. 4-9. Let $R_1 = 60\,\text{k}\Omega$, $R_2 = 40\,\text{k}\Omega$, $R_D = 3\,\text{k}\Omega$, $R_L = 1\,\text{k}\Omega$, $V_{DD} = 15\,\text{V}$, and $C_C \to \infty$. (*a*) Find V_{GSQ}. (*b*) Graphically determine V_{DSQ} and I_{DQ}.

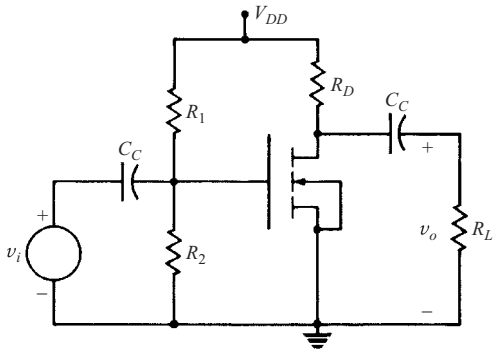


Fig. 4-25

(*a*) Assume $i_G = 0$. Then, by (*4.3*),

$$V_{GSQ} = V_{GG} = \frac{R_2}{R_2 + R_1} V_{DD} = \frac{40 \times 10^3}{40 \times 10^3 + 60 \times 10^3} 15 = 6\,\text{V}$$

(*b*) The dc load line is constructed on Fig. 4-9 with v_{DS} intercept $V_{DD} = 15\,\text{V}$ and i_D intercept $V_{DD}/R_L = 5\,\text{mA}$. The Q-point quantities can be read directly from projections back to the i_D and v_{DS} axes; they are $V_{DSQ} \approx 11.3\,\text{V}$ and $I_{DQ} \approx 1.4\,\text{mA}$.

4.21 For the enhancement-mode MOSFET amplifier of Problem 4.20, let $v_i = \sin \omega t$ and graphically determine v_o.

We have, first,

$$R_{\text{ac}} = R_D \| R_L = \frac{(3 \times 10^3)(1 \times 10^3)}{3 \times 10^3 + 1 \times 10^3} = 0.75\,\text{k}\Omega$$

An ac load line must be added to Fig. 4-9; it passes through the Q point and intersects the v_{DS} axis at

$$V_{DSQ} + I_{DQ}R_{\text{ac}} = 11.3 + (1.4 \times 10^{-3})(0.75 \times 10^3) = 12.35\,\text{V}$$

Now we construct an auxiliary time axis through the Q point and perpendicular to the ac load line; on it, we construct the waveform $v_{gs} = v_i$ as it swings $\pm 1\,\text{V}$ along the ac load line about the Q point. An additional auxiliary time axis is constructed perpendicular to the v_{DS} axis, to display the output voltage $v_o = v_{ds}$ as v_{gs} swings along the ac load line.

4.22 If, instead of depending on the enhanced channel (see Fig. 4-7) for conduction, the region between the two heavily doped n^+ regions of the MOSFET is made up of lightly doped n material, a *depletion-enhancement-mode* MOSFET can be formed with drain characteristics as

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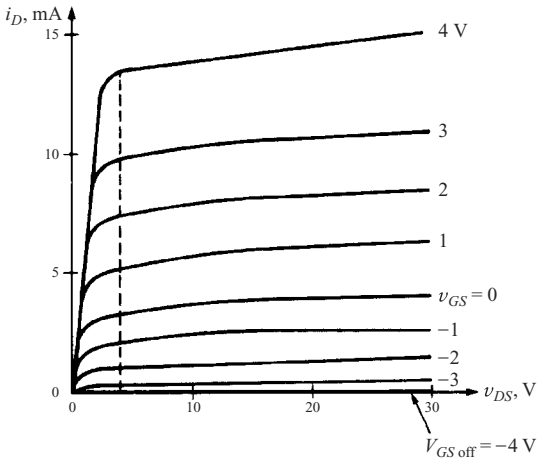


Fig. 4-26

displayed by Fig. 4-26, where v_{GS} may be either positive or negative. Construct a transfer characteristic for the drain characteristics of Fig. 4-26, and clearly label the regions of depletion-mode and enhancement-mode operation.

If a constant value of $v_{DS} = V_{GSon} = 4\,\text{V}$ is taken as indicated by the broken line on Fig. 4-26, the transfer characteristic of Fig. 4-27 results. $v_{GS} = 0$ is the dividing line between depletion- and enhancement-mode operation.

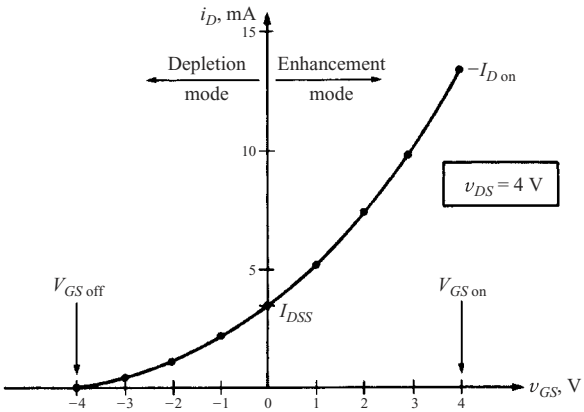


Fig. 4-27

4.23 A common-gate JFET amplifier is shown in Fig. 4-28. The JFET obeys (*4.2*). If $I_{DSS} = 10\,\text{mA}$, $V_{p0} = 4\,\text{V}$, $V_{DD} = 15\,\text{V}$, $R_1 = R_2 = 10\,\text{k}\Omega$, $R_D = 500\,\Omega$, and $R_S = 2\,\text{k}\Omega$, determine (*a*) V_{GSQ}, (*b*) I_{DQ}, and (*c*) V_{DSQ}. Assume $i_G = 0$.

(*a*) By KVL,

$$V_{GSQ} = \frac{R_2}{R_1 + R_2} V_{DD} - I_{DQ} R_S \tag{1}$$

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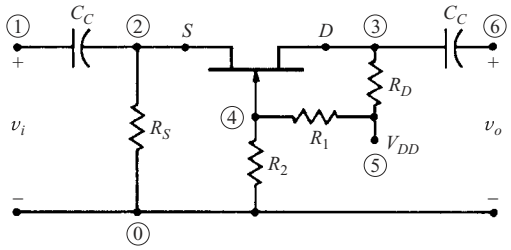


Fig. 4-28

Solving (*1*) for I_{DQ} and equating the result to the right side of (*4.2*) yield

$$\frac{\dfrac{R_2}{R_1+R_2}V_{DD}-V_{GSQ}}{R_S}=I_{DSS}\left(1+\frac{V_{GSQ}}{V_{p0}}\right)^2 \tag{2}$$

Rearranging leads to a quadratic in V_{GSQ},

$$V_{GSQ}^2+\left(2V_{p0}+\frac{V_{p0}^2}{I_{DSS}R_S}\right)V_{GSQ}+V_{p0}^2\left[1-\frac{R_2V_{DD}}{(R_1+R_2)I_{DSS}R_S}\right]=0 \tag{3}$$

or, with known values substituted,

$$V_{GSQ}^2+8.8V_{GSQ}+10=0 \tag{4}$$

Solving for V_{GSQ} and disregarding the extraneous root $V_{GSQ}=-7.46<-V_{p0}$, we determine that $V_{GSQ}=-1.34\,\text{V}$.

(*b*) By (*4.2*),

$$I_{DQ}=I_{DSS}\left(1+\frac{V_{GSQ}}{V_{p0}}\right)^2=(10\times10^{-3})\left(1+\frac{-1.34}{4}\right)^2=4.42\,\text{mA}$$

(*c*) By KVL,

$$V_{DSQ}=V_{DD}-I_{DQ}(R_S+R_D)=15-(4.42\times10^{-3})(2\times10^3+500)=3.95\,\text{V}$$

4.24 For a triode with plate characteristics given by Fig. 4-29, find (*a*) the perveance κ and (*b*) the amplification factor μ.

(*a*) The perveance can be evaluated at any point on the $v_G=0$ curve. Choosing the point with coordinates $i_P=15\,\text{mA}$ and $v_P=100\,\text{V}$, we have, from (*4.9*),

$$\kappa=\frac{i_P}{v_P^{3/2}}=\frac{15\times10^{-3}}{100^{3/2}}=15\,\mu\text{A/V}^{3/2}$$

(*b*) The amplification factor is most easily evaluated along the v_P axis. From (*4.9*), for the point $i_P=0$, $v_P=100\,\text{V}$, $v_G=-4\,\text{V}$, we obtain

$$\mu=-\frac{v_P}{v_G}=-\frac{100}{-4}=25$$

4.25 The amplifier of Example 4.7 has plate current

$$i_P=I_P+i_p=8+\cos\omega t \qquad \text{mA}$$

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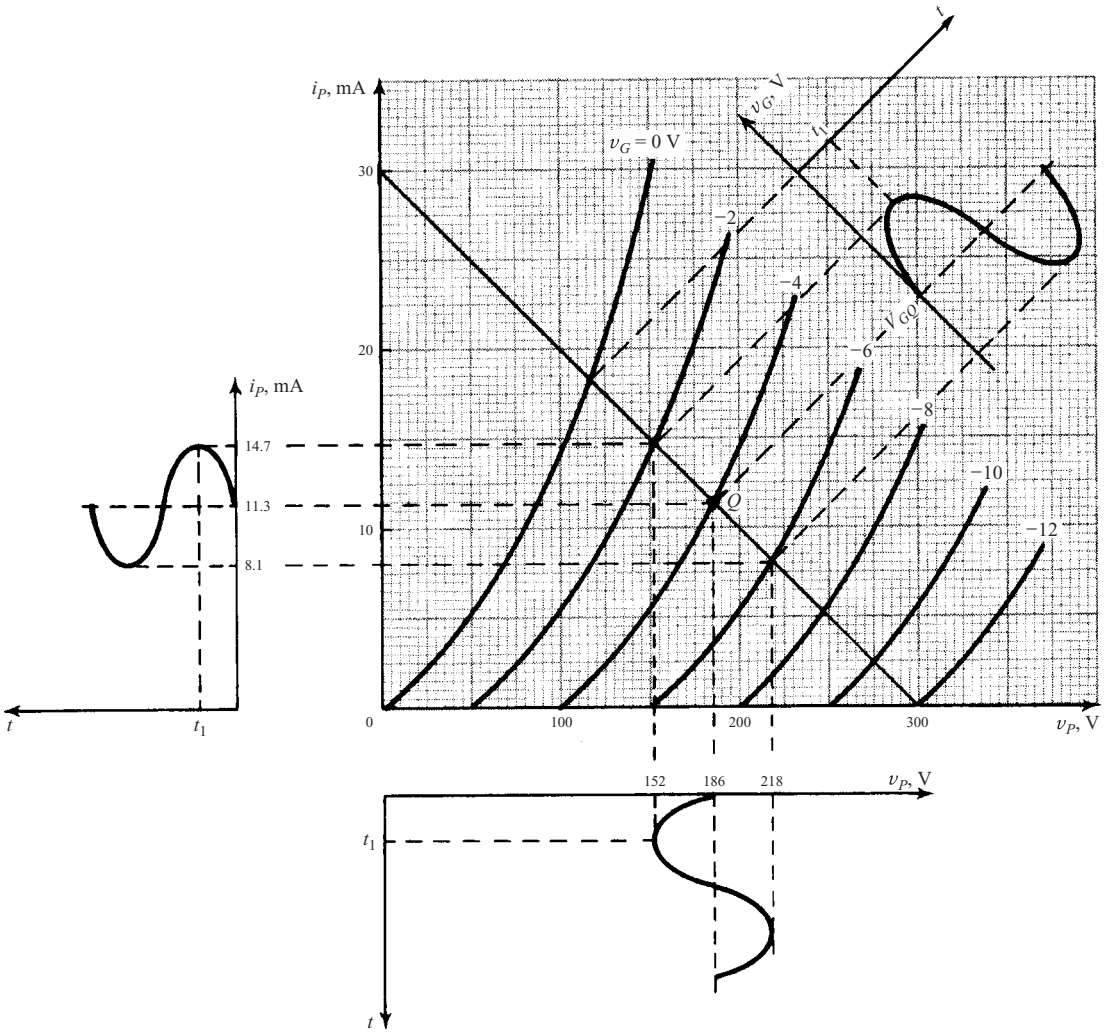


Fig. 4-29

Determine (*a*) the power delivered by the plate supply voltage V_{PP}, (*b*) the average power delivered to the load R_L, and (*c*) the average power dissipated by the plate of the triode. (*d*) If the tube has a plate rating of 2 W, is it being properly applied?

(*a*) The power supplied by the source V_{PP} is found by integration over a period of the ac waveform:

$$P_{PP} = \frac{1}{T}\int_0^T V_{PP} i_P \, dt = V_{PP} I_P = (300)(8 \times 10^{-3}) = 2.4\,\text{W}$$

(*b*) $$P_L = \frac{1}{T}\int_0^T i_P^2 R_L \, dt = R_L(I_P^2 + I_p^2) = 10 \times 10^3 \left[(8 \times 10^{-3})^2 + \left(\frac{1 \times 10^{-3}}{\sqrt{2}} \right)^2 \right] = 0.645\,\text{W}$$

(*c*) The average power dissipated by the plate is

$$P_P = P_{PP} - P_L = 2.4 - 0.645 = 1.755\,\text{W}$$

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(*d*) The tube is not properly applied. If the signal is removed (so that $i_P = 0$), then the plate dissipation increases to $P_P = P_{PP} = 2.4\,\text{W}$, which exceeds the power rating.

4.26 The *plate efficiency* of a vacuum-tube amplifier is defined as the ratio of ac signal power delivered to the load to plate supply power, or P_{Lac}/P_{PP}. (*a*) Calculate the plate efficiency of the amplifier of Problem 4.25. (*b*) What is the maximum possible plate efficiency for this amplifier without changing the Q point or clipping the signal?

(*a*) $$\eta = \frac{P_{\text{Lac}}}{P_{PP}}(100\%) = \frac{I_p^2 R_L}{V_{PP} I_P}(100\%) = \frac{(10^{-3}/\sqrt{2})^2(10 \times 10^3)}{2.4}(100\%) = 0.208\%$$

(*b*) Ideally, the input signal could be increased until i_P swings $\pm 8\,\text{mA}$; thus,

$$\eta_{\max} = \left(\frac{8}{1}\right)^2 (0.208\%) = 13.31\%$$

4.27 The triode amplifier of Fig. 4-30 utilizes *cathode bias* to eliminate the need for a grid power supply. The very large resistance R_G provides a path to ground for stray charge collected by the grid; this current is so small, however, that the voltage drop across R_G is negligible. It follows that the grid is maintained at a negative bias, so

$$v_G = -R_K i_P \tag{1}$$

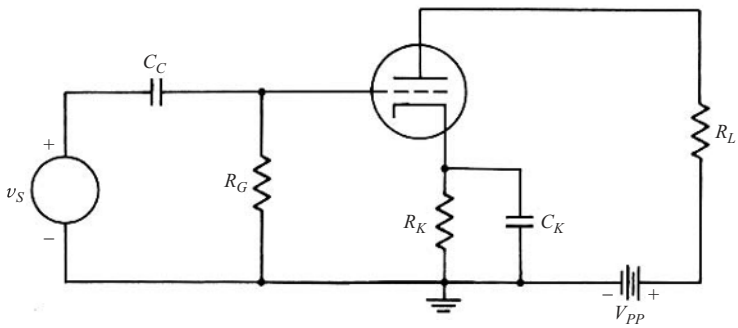


Fig. 4-30

A plot of (1) on the plate characteristics is called the *grid bias line*, and its intersection with the dc load line determines the Q point. Let $R_L = 11.6\,\text{k}\Omega$, $R_K = 400\,\Omega$, $R_G = 1\,\text{M}\Omega$, and $V_{PP} = 300\,\text{V}$. If the plate characteristics of the triode are given by Fig. 4-31, (*a*) draw the dc load line, (*b*) sketch the grid bias line, and (*c*) determine the Q-point quantities.

(*a*) The dc load line has horizontal intercept $V_{PP} = 300\,\text{V}$ and vertical intercept

$$\frac{V_{PP}}{R_{\text{dc}}} = \frac{V_{PP}}{R_L + R_K} = \frac{300}{(11.6 + 0.4) \times 10^3} = 25\,\text{mA}$$

as shown on the plate characteristics of Fig. 4-31.

(*b*) Points for the plot of (*1*) are found by selecting values of i_P and calculating the corresponding values of v_G. For example, if $i_P = 5\,\text{mA}$, then $v_G = -400(5 \times 10^{-3}) = -2\,\text{V}$, which plots as point 1 of the dashed grid bias line in Fig. 4-31. Note that this is not a straight line.

(*c*) From the intersection of the grid bias line with the dc load line, $I_{PQ} = 10\,\text{mA}$, $V_{PQ} = 180\,\text{V}$, and $V_{GQ} = -4\,\text{V}$.

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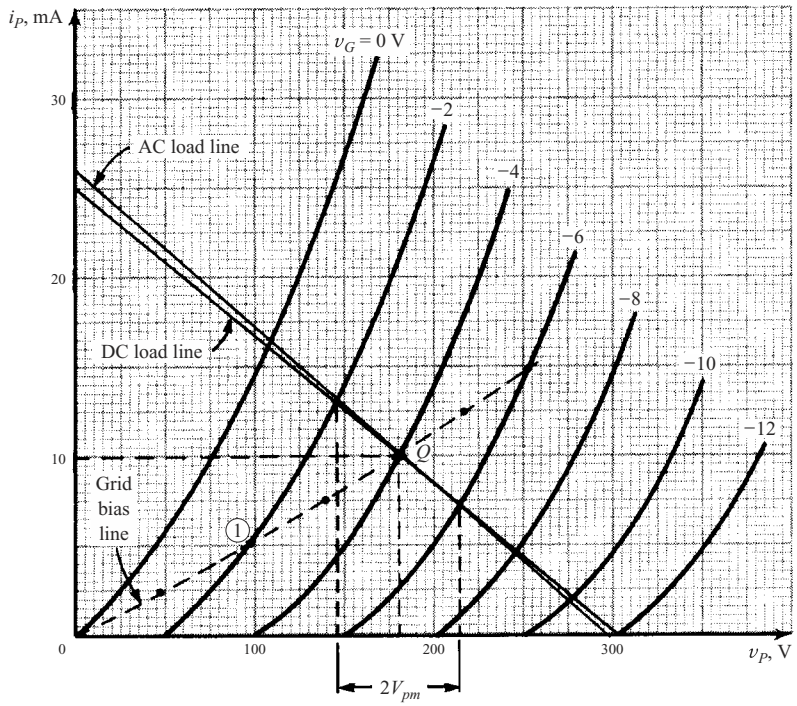


Fig. 4-31

Supplementary Problems

4.28 In the JFET amplifier of Example 4.2, R_1 is changed to 2 MΩ to increase the input impedance. If R_D, R_S, and V_{DD} are unchanged, what value of R_2 is needed to maintain the original Q point? *Ans.* 15.67 MΩ

4.29 Find the voltage across R_S in Example 4.2. *Ans.* 3 V

4.30 Find the input impedance as seen by source v_i of Example 4.2 if C_C is large. *Ans.* 940 kΩ

4.31 The method of *source bias*, illustrated in Fig. 4-32, can be employed for both JFETs and MOSFETs. For a JFET with characteristics given by Fig. 4-6 and with $R_D = 1\,\text{k}\Omega$, $R_S = 4\,\text{k}\Omega$, and $R_G = 10\,\text{M}\Omega$, determine V_{DD} and V_{SS} so that the amplifier has the same quiescent conditions as the amplifier of Example 4.2. *Ans.* $V_{SS} = 4\,\text{V}$, $V_{DD} = 16\,\text{V}$

4.32 In the drain-feedback-biased amplifier of Fig. 4-9(*a*), $V_{DD} = 15\,\text{V}$, $R_F = 5\,\text{M}\Omega$, $I_{DQ} = 0.7\,\text{mA}$, and $V_{GSQ} = 4.5\,\text{V}$. Find (*a*) V_{DSQ} and (*b*) R_L. *Ans.* (*a*) 4.5 V; (*b*) 14 kΩ

4.33 A JFET amplifier with the circuit arrangement of Fig. 4-5 is to be manufactured using devices as described in Problem 4.7. For the design, assume a nominal device and use $V_{DD} = 24\,\text{V}$, $V_{DSQ} = 15\,\text{V}$, $I_{DQ} = 2\,\text{mA}$, $R_1 = 2\,\text{M}\Omega$, and $R_2 = 30\,\text{M}\Omega$. (*a*) Determine the values of R_S and R_D for the amplifier. (*b*) Predict the range of I_{DQ} that can be expected. *Ans.* (*a*) $R_S = 1.475\,\text{k}\Omega$, $R_D = 3.03\,\text{k}\Omega$; (*b*) 1.8 to 2.2 mA

4.34 To see the effect of a source resistor on Q-point conditions, solve Problem 4.10 with $R_S = 500\,\Omega$ and all else unchanged. *Ans.* (*a*) $V_{GG} = -3.58\,\text{V}$; (*b*) $V_{DSQ} = -4\,\text{V}$

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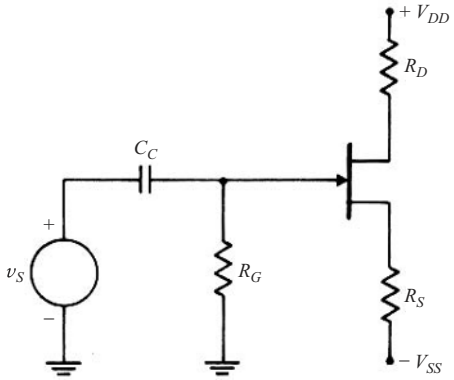


Fig. 4-32

4.35 Solve Problem 4.12 with a 200-Ω source resistor R_S added to the circuit, and all else unchanged.
Ans. (*a*) $R_2 = 190\,\text{k}\Omega$; (*b*) $R_D = 9.4\,R\Omega$

4.36 For the *n*-channel JFET circuit of Fig. 4-20, $I_{DSS} = 6\,\text{mA}$, $V_{p0} = 4\,\text{V}$, $R_D = 5\,\text{k}\Omega$, $R_S = 10\,\text{k}\Omega$, $V_{DD} = 15\,\text{V}$, and $V_{SS} = 10\,\text{V}$. The JFET is described by (*4.2*). (*a*) Find the value of V_G that renders $V_o = 0$, and (*b*) determine V_{DSQ} if $V_o = 0$. *Ans.* (*a*) 17.63 V; (*b*) 10 V

4.37 In the differential amplifier of Fig. 4-22, the identical JFETs are characterized by $I_{DSS} = 10\,\text{mA}$, $V_{p0} = 4\,\text{V}$, and $i_G = 0$. If $V_{DD} = 15\,\text{V}$, $V_{SS} = 5\,\text{V}$, $R_S = 3\,\text{k}\Omega$, and $R_D = 5\,\text{k}\Omega$, find I_{DQ1} and V_{DSQ1}.
Ans. 1.27 mA, 6.03 V

4.38 The differential amplifier of Fig. 4-22 has the circuit element values of Problem 4.37. The identical JFETs are described by the model of Example 4.1. Use SPICE methods to determine voltage $v_{o1} = v_{o2}$. (*Netlist code available from author website.*) *Ans.* 8.81 V

4.39 A voltage source is connected to the differential amplifier of Fig. 4-22 such that $V_{G1} = 0.5\,\text{V}$. Let $V_{DD} = 15\,\text{V}$, $V_{SS} = 2\,\text{V}$, $I_{DSS} = 10\,\text{mA}$, $V_{p0} = 4\,\text{V}$ for the identical JFETs, $R_D = 6\,\text{k}\Omega$, and $R_S = 1\,\text{k}\Omega$. Find (*a*) v_{o1} and (*b*) v_{o2}. *Ans.* (*a*) 2.53 V; (*b*) 8.42 V

4.40 For the series-connected, nonidentical JFETs of Fig. 4-23, $i_{G1} = i_{G2} = 0$, $I_{DSS1} = 8\,\text{mA}$, $I_{DSS2} = 10\,\text{mA}$, and $V_{p01} = V_{p02} = 4\,\text{V}$. Let $V_{DD} = 15\,\text{V}$, $R_G = 1\,\text{M}\Omega$, $R_D = 5\,\text{k}\Omega$, and $R_S = 2\,\text{k}\Omega$. Find (*a*) I_{DQ1}, (*b*) V_{GSQ1}, (*c*) V_{GSQ2}, (*d*) V_{DSQ1}, and (*e*) V_{DSQ2}.
Ans. (*a*) 1.22 mA; (*b*) − 2.44 V; (*c*) − 2.605 V; (*d*) 0.165 V; (*e*) 6.295 V

4.41 The series-connected, identical JFETs of Fig. 4-23 are characterized by $I_{DSS} = 8\,\text{mA}$, $V_{p0} = 4\,\text{V}$, and $i_G = 0.5\mu\text{A}$. If $V_{DD} = 15\,\text{V}$, $R_D = 5\,\text{k}\Omega$, $R_S = 2\,\text{k}\Omega$, and $R_G = 1\,\text{M}\Omega$, find (*a*) V_{GSQ1}, (*b*) V_{GSQ2}, (*c*) V_{DSQ1}, and (*d*) V_{DSQ2}. *Ans.* (*a*) = −3.44 V; (*b*) − 3.44 V; (*c*) 0 V; (*d*) 6.46 V

4.42 In the circuit of Fig. 4-24, the identical JFETs are described by $I_{DSS} = 8\,\text{mA}$, $V_{p0} = 4\,\text{V}$, and $i_G = 0.1\,\mu\text{A}$. If $R_D = 1\,\text{k}\Omega$, $R_S = 2\,\text{k}\Omega$, $R_G = 1\,\text{M}\Omega$, and $V_{DD} = 15\,\text{V}$, find (*a*) V_{GSQ1}, (*b*) V_{GSQ2}, (*c*) I_{DQ2}, (*d*) V_{DSQ2}, and (*e*) V_{DSQ1}.
Ans. (*a*) − 3.986 V; (*b*) − 1.65 V; (*c*) 2.76 mA; (*d*) 6.72 V; (*e*) 8.37 V

4.43 For the enhancement-mode MOSFET of Problem 4.20, determine the value of I_{Don}. *Ans.* 5.6 mA

4.44 Let $V_{DD} = 15\,\text{V}$, $R_D = 1\,\text{k}\Omega$, $R_S = 500\,\Omega$, and $R_2 = 10\,\text{k}\Omega$ for the circuit of Fig. 4-18. The MOSFET is a depletion enhancement mode device that can be characterized by the parameters of Example 4.2 except that Vto = −4 V. Use SPICE methods to determine the range of R_1 such that the MOSFET is (*a*) biased for

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depletion-mode operation ($V_{GSQ} < 0$) and (*b*) enhancement-mode operation ($V_{GSQ} > 0$). (*Netlist code available from author website.*) *Ans.* (*a*) $R_1 > 2.71\,\text{k}\Omega$; (*b*) $R_1 < 2.71\,\text{k}\Omega$

4.45 The common-gate JFET amplifier of Problem 4.23 is not biased for maximum symmetrical swing. Shift the bias point by letting $R_1 = 10\,\text{k}\Omega$ and $R_2 = 5\,\text{k}\Omega$ while all else is unchanged. Does the amplifier bias point move closer to the condition of maximum symmetrical swing? *Ans.* Yes; $V_{DSQ} = 6.59\,\text{V}$

4.46 In the circuit of Fig. 4-33, $R_G \gg R_{S1}, R_{S2}$. The JFET is described by (*4.2*), $I_{DSS} = 10\,\text{mA}$, $V_{p0} = 4\,\text{V}$, $V_{DD} = 15\,\text{V}$, $V_{DSQ} = 10\,\text{V}$, and $V_{GSQ} = -2\,\text{V}$. Find (*a*) R_{S1}, (*b*) R_{S2}, and (*c*) v_S.
Ans. (*a*) $800\,\Omega$; (*b*) $1.2\,\text{k}\Omega$; (*c*) $5\,\text{V}$

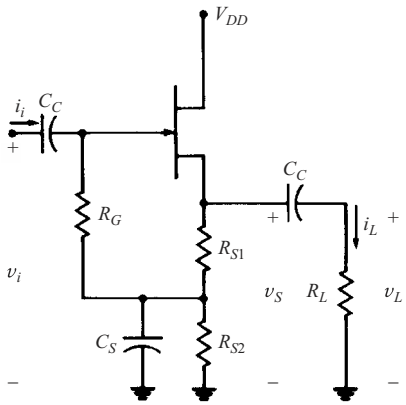


Fig. 4-33

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CHAPTER 5

Transistor Bias Considerations

5.1. INTRODUCTION

In the initial design of transistor circuits, the quiescent operating point is carefully established to ensure that the transistor will operate within specified limits. Completion of the design requires a check of quiescent-point variations due to temperature changes and unit-to-unit parameter differences, to ensure that such variations are within an acceptable range. As the principles of operation of the BJT and FET differ greatly, so do the associated methods of Q-point stabilization.

5.2. β UNCERTAINTY AND TEMPERATURE EFFECTS IN THE BJT

Uncertainty as to the value of β may be due either to unit-to-unit variation (which may reach 200 percent or more) or to temperature variation (1 percent/°C or less); however, since unit-to-unit variation has the greater effect, a circuit that has been desensitized to such variation is also insensitive to the effect of temperature on β. The design must, however, directly compensate for the effects of temperature on leakage current I_{CBO} (which doubles for each 10°C rise in temperature) and base-to-emitter voltage V_{BEQ} (which decreases approximately 1.6 mV for each 1°C temperature increase in Ge devices, and approximately 2 mV for each 1°C rise in Si devices).

Constant-Base-Current Bias

The constant-base-current bias arrangement of Fig. 3-14 has the advantage of high current gain; however, the sensitivity of its Q point to changes in β limits is usage.

Example 5.1. The Si transistor of Fig. 3-14 is biased for constant base current. Neglect leakage current I_{CBO}, and let $V_{CC} = 15\,\text{V}$, $R_B = 500\,\text{k}\Omega$, and $R_C = 5\,\text{k}\Omega$. Find I_{CQ} and V_{CEQ} (*a*) if $\beta = 50$, and (*b*) if $\beta = 100$.

(*a*) By KVL,

$$V_{CC} = V_{BEQ} + I_{BQ}R_B \tag{5.1}$$

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Since $I_{BQ} = I_{CQ}/\beta$, we may write, using (*5.1*),

$$I_{CQ} = \beta I_{BQ} = \frac{\beta(V_{CC} - V_{BEQ})}{R_B} = \frac{50(15 - 0.7)}{500 \times 10^3} = 1.43\,\text{mA} \tag{5.2}$$

so that, by KVL,

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 15 - (1.43)(5) = 7.85\,\text{V} \tag{5.3}$$

(*b*) With β changed to 100, (*5.2*) gives

$$I_{CQ} = \frac{100(15 - 0.7)}{500 \times 10^3} = 2.86\,\text{mA}$$

and, from (*5.3*),

$$V_{CEQ} = 15 - (2.86)(5) = 0.7\,\text{V}$$

Note that, in this example, the collector current I_{CQ} doubled with the doubling of β, and the Q point moved from near the middle of the dc load line to near the saturation region.

Example 5.2. Show that, in the circuit of Fig. 3-14, I_{CQ} varies linearly with β even if leakage current is not neglected, provided $\beta \gg 1$.

Using the result of Problem 3.36(*a*) and KVL, we have

$$I_{BQ}R_B = \frac{I_{CQ} - (\beta + 1)I_{CBO}}{\beta} R_B = V_{CC} - V_{BEQ}$$

Rearranging and assuming $\beta \gg 1$ lead to the desired result:

$$I_{CQ} = \frac{\beta(V_{CC} - V_{BEQ})}{R_B} + \frac{\beta + 1}{\beta} I_{CBO} \approx \frac{\beta(V_{CC} - V_{BEQ})}{R_B} + I_{CBO}$$

Constant-Emitter-Current Bias

In the CE amplifier circuit of Fig. 5-1, the leakage current is explicitly modeled as a current source.

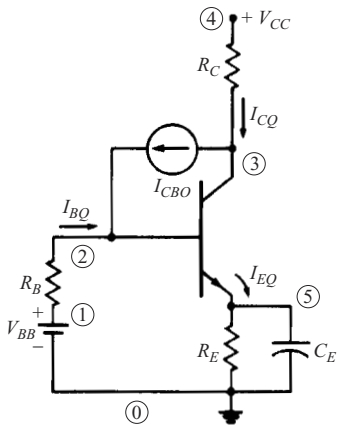


Fig. 5-1

Example 5.3. Use the circuit of Fig. 5-1 to show that (*3.8*) is the condition for β-independent bias even when leakage current is not neglected.

By KVL,

$$V_{BB} = I_{BQ}R_B + V_{BEQ} + I_{EQ}R_E \tag{5.4}$$

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Using the results of Problem 3.36 and assuming that $\beta \gg 1$, we may write

$$I_{EQ} = \frac{\beta+1}{\beta}(I_{CQ} - I_{CBO}) \approx I_{CQ} - I_{CBO} \tag{5.5}$$

and

$$I_{BQ} = \frac{I_{CQ}}{\beta} - \frac{\beta+1}{\beta} I_{CBO} \approx \frac{I_{CQ}}{\beta} - I_{CBO} \tag{5.6}$$

Substituting (5.5) and (5.6) into (5.4) and rearranging then give

$$I_{CQ} = \frac{V_{BB} - V_{BEQ} + I_{CBO}(R_B + R_E)}{R_B/\beta + R_E} \tag{5.7}$$

From (5.7) it is apparent that leakage current I_{CBO} increases I_{CQ}. However, I_{CQ} is relatively independent of β only when $R_B/\beta \ll R_E$.

Shunt-Feedback Bias

A compromise between constant-base-current bias and constant-emitter-current bias is offered by the shunt-feedback-bias circuit of Fig. 3-17, as the following example shows.

Example 5.4. In the shunt-feedback-bias circuit of Fig. 3-17, $V_{CC} = 15\,\text{V}$, $R_C = 2\,\text{k}\Omega$, $R_F = 150\,\text{k}\Omega$, and $I_{CBO} \approx 0$. The transistor is a Si device. Find I_{CQ} and V_{CEQ} if (*a*) $\beta = 50$ and (*b*) $\beta = 100$.

(*a*) By KVL,

$$V_{CC} = (I_{CQ} + I_{BQ})R_C + I_{BQ}R_F + V_{BEQ} = \left(I_{CQ} + \frac{I_{CQ}}{\beta}\right)R_C + \frac{I_{CQ}}{\beta} R_F + V_{BEQ}$$

so that

$$I_{CQ} = \frac{\beta(V_{CC} - V_{BEQ})}{R_F + (\beta+1)R_C} = \frac{50(15 - 0.7)}{150 \times 10^3 + (51)(2 \times 10^3)} = 2.84\,\text{mA}$$

Now KVL gives

$$V_{CEQ} = V_{CC} - (I_{BQ} + I_{CQ})R_C = V_{CC} - \left(\frac{1}{\beta} + 1\right) I_{CQ} R_C$$

$$= 15 - \left(\frac{1}{50} + 1\right)(2.84 \times 10^{-3})(2 \times 10^3) = 9.21\,\text{V}$$

(*b*) For $\beta = 100$,

$$I_{CQ} = \frac{100(15 - 0.7)}{150 \times 10^3 + (101)(2 \times 10^3)} = 4.06\,\text{mA}$$

and

$$V_{CEQ} = 15 - \left(\frac{1}{100} + 1\right)(4.06 \times 10^{-3})(2 \times 10^3) = 6.80\,\text{V}$$

With shunt-feedback bias the increase in I_{CQ} is appreciable (here, 43 percent); this case lies between the β-insensitive case of constant-emitter-current bias and the directly sensitive case of constant-base-current bias.

Example 5.5. Neglecting leakage current in the shunt-feedback-bias amplifier of Fig. 3-17, find a set of conditions that will render the collector current I_{CQ} insensitive to small variations in β. Is the condition practical?

From Example 5.4, if $\beta \gg 1$,

$$I_{CQ} = \frac{V_{CC} - V_{BEQ}}{\dfrac{R_F}{\beta} + \dfrac{\beta+1}{\beta} R_C} \approx \frac{V_{CC} - V_{BEQ}}{\dfrac{R_F}{\beta} + R_C}$$

The circuit would be insensitive to β variations if $R_F/\beta \ll R_C$. However, since $0.3 \le V_{BEQ} \le 0.7$, that would lead to $I_{CQ}R_C \to V_{CC}$; hence, V_{CEQ} would come close to 0 and the transistor would operate near the saturation region.

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5.3. STABILITY-FACTOR ANALYSIS

Stability-factor or *sensitivity* analysis is based on the assumption that, for small changes, the variable of interest is a linear function of the other variables, and thus its differential can be replaced by its increment. In a study of BJT Q-point stability, we examine changes in quiescent collector current I_{CQ} due to variations in transistor quantities and/or elements of the surrounding circuit. Specifically, if

$$I_{CQ} = f(\beta, I_{CBO}, V_{BEQ}, \ldots) \tag{5.8}$$

then, by the chain rule, the total differential is

$$dI_{CQ} = \frac{\partial I_{CQ}}{\partial \beta}\, d\beta + \frac{\partial I_{CQ}}{\partial I_{CBO}}\, dI_{CBO} + \frac{\partial I_{CQ}}{\partial V_{BEQ}}\, dV_{BEQ} + \cdots \tag{5.9}$$

We may define a set of *stability factors* or *sensitivity factors* as follows:

$$S_\beta = \left.\frac{\Delta I_{CQ}}{\Delta \beta}\right|_Q \approx \left.\frac{\partial I_{CQ}}{\partial \beta}\right|_Q \tag{5.10}$$

$$S_I = \left.\frac{\Delta I_{CQ}}{\Delta I_{CBO}}\right|_Q \approx \left.\frac{\partial I_{CQ}}{\partial I_{CBO}}\right|_Q \tag{5.11}$$

$$S_V = \left.\frac{\Delta I_{CQ}}{\Delta V_{BEQ}}\right|_Q \approx \left.\frac{\partial I_{CQ}}{V_{BEQ}}\right|_Q \tag{5.12}$$

and so on. Then replacing the differentials with increments in (5.9) yields a first-order approximation to the total change in I_{CQ}:

$$\Delta I_{CQ} \approx S_\beta\, \Delta\beta + S_I\, \Delta I_{CBO} + S_V\, \Delta V_{BEQ} + \cdots \tag{5.13}$$

Example 5.6. For the CE amplifier of Fig. 5-1, use stability-factor analysis to find an expression for the change in I_{CQ} due to variations in β, I_{CBO}, and V_{BEQ}.

The quiescent collector current I_{CQ} is expressed as a function of β, I_{CBO}, and V_{BEQ} in (5.7). Thus, by (5.13),

$$\Delta I_{CQ} \approx S_\beta\, \Delta\beta + S_I\, \Delta I_{CBO} + S_V\, \Delta V_{BEQ} \tag{5.14}$$

where the stability factors, according to (5.10) through (5.12), are

$$S_\beta = \frac{\partial I_{CQ}}{\partial \beta} = \frac{\partial}{\partial \beta}\left\{\frac{\beta[V_{BB} - V_{BEQ} + I_{CBO}(R_B + R_E)]}{R_B + \beta R_E}\right\} = \frac{R_B[V_{BB} - V_{BEQ} + I_{CBO}(R_B + R_E)]}{(R_B + \beta R_E)^2} \tag{5.15}$$

$$S_I = \frac{\partial I_{CQ}}{\partial I_{CBO}} = \frac{R_B + R_E}{R_B/\beta + R_E} \tag{5.16}$$

$$S_V = \frac{\partial I_{CQ}}{\partial V_{BEQ}} = -\frac{\beta}{R_B + \beta R_E} \tag{5.17}$$

5.4. NONLINEAR-ELEMENT STABILIZATION OF BJT CIRCUITS

Nonlinear changes in quiescent collector current due to temperature variation can, in certain cases, be eliminated or drastically reduced by judicious insertion of nonlinear devices (such as diodes) into transistor circuits.

Example 5.7. In the CE amplifier circuit of Fig. 5-1, assume that the Si device has negligible leakage current and (3.8) holds to the point that R_B/β can be neglected. Also, V_{BEQ} decreases by 2 mV/°C from its value of 0.7 V at 25°C. Find the change in I_{CQ} as the temperature increases from 25°C to 125°C.

Let the subscript 1 denote "at $T = 25$°C," and 2 denote "at $T = 125$°C." Under the given assumptions, (5.7) reduces to

$$I_{CQ} = \frac{V_{BB} - V_{BEQ}}{R_E}$$

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The change in I_{CQ} is then

$$\Delta I_{CQ} = I_{CQ2} - I_{CQ1} = \frac{0.002(T_2 - T_1)}{R_E} = \frac{0.2}{R_E}$$

Example 5.8. Assume that the amplifier circuit of Fig. 5-2 has been designed so it is totally insensitive to variations of β. Further, $R_B \gg R_D$. As in Example 5.7, V_{BEQ} is equal to 0.7 V at 25°C and decreases by 2 mV/°C. Also assume that V_D varies with temperature exactly as V_{BEQ} does. Find the change in I_{CQ} as the temperature increases from 25°C to 125°C.

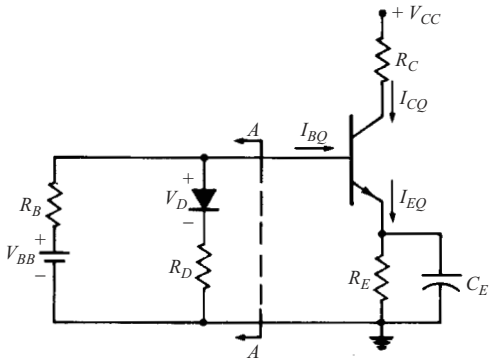


Fig. 5-2

A Thévenin equivalent circuit can be found for the network to the left of terminals A, A, under the assumption that the diode can be modeled by a voltage source V_D. The result is

$$R_{TH} = R_D \| R_B \approx R_D$$

$$V_{Th} = V_D + \frac{V_{BB} - V_D}{R_B + R_D} R_D = \frac{V_{BB} R_D + V_D R_B}{R_D + R_B}$$

With the Thévenin equivalent in place, KVL and the assumption $I_{BQ} = I_{CQ}/\beta \approx I_{EQ}/\beta$ give

$$I_{CQ} \approx I_{EQ} = \frac{(V_{BB} R_D + V_D R_B)/(R_D + R_B) - V_{BEQ}}{R_D/\beta + R_E}$$

Now if there is total independence of β, then R_D/β must be negligible compared with R_E. Further, since only V_D and V_{BEQ} are dependent on temperature,

$$\frac{\partial I_{CQ}}{\partial T} \approx \frac{\dfrac{R_B}{R_B + R_D}\dfrac{\partial V_D}{\partial T} - \dfrac{\partial V_{BEQ}}{\partial T}}{R_E} = \frac{0.002 R_D}{R_E(R_B + R_D)} \approx \frac{0.002}{R_E}\frac{R_D}{R_B}$$

Hence,

$$\Delta I_{CQ} \approx \frac{\partial I_{CQ}}{\partial T}\Delta T = \frac{0.002}{R_E}\frac{R_D}{R_B} 100 = \frac{0.2}{R_E}\frac{R_D}{R_B}$$

Because $R_D \ll R_B$ here, the change in I_{CQ} has been reduced appreciably from what it was in the circuit of Example 5.7.

5.5. *Q*-POINT-BOUNDED BIAS FOR THE FET

Just as β may vary in the BJT, the FET shorted-gate parameters I_{DSS} and V_{p0} can vary widely within devices of the same classification. It is, however, possible to set the gate-source bias so that, in spite of this variation, the Q point (and hence the quiescent drain current) is confined within fixed limits.

The extremes of FET parameter variation are usually specified by the manufacturer, and (*4.2*) may be used to establish upper and lower (worst-case) transfer characteristics (Fig. 5-3). The upper and

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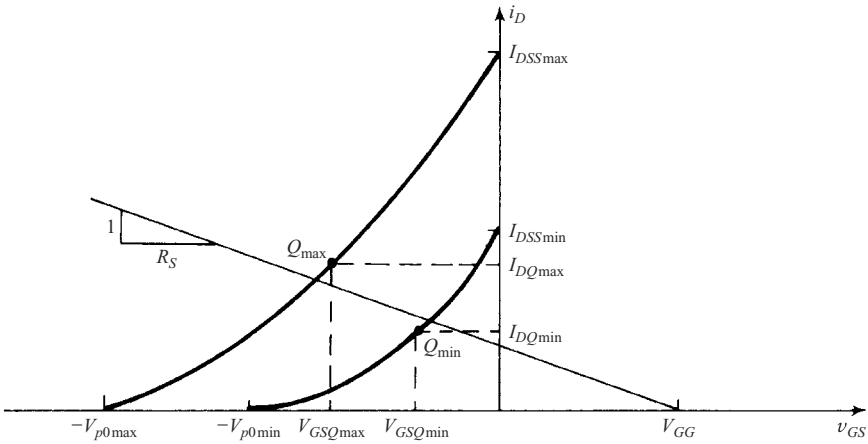


Fig. 5-3

lower quiescent points $Q_{\max}$ and $Q_{\min}$ are determined by their ordinates $I_{DQ\max}$ and $I_{DQ\min}$; we assign $I_{DQ\max}$ and $I_{DQ\min}$ as the limits of allowable variation of I_{DQ} along a dc load line superimposed on the family of nominal drain characteristics. (These in turn establish $V_{DSQ\max}$ and $V_{DSQ\min}$, respectively.) This dc load line is established by choosing $R_D + R_S$ in a circuit like that of Fig. 4-5 so that v_{DS} remains within a desired region of the nominal drain characteristics.

If now a value of R_S is selected such that

$$R_S \geq \frac{|V_{GSQ\max} - V_{GSQ\min}|}{I_{DQ\max} - I_{DQ\min}} \tag{5.18}$$

Then the transfer bias line with slope $-1/R_S$ and v_{GS} intercept $V_{GG} \geq 0$ is located as shown in Fig. 5-3, and the nominal Q point is forced to lie beneath $Q_{\max}$ and above $Q_{\min}$, so that, as desired,

$$I_{DQ\min} \leq I_{DQ} \leq I_{DQ\max}$$

With R_S, R_D, and V_{GG} already assigned, R_G is chosen large enough to give a satisfactory input impedance, and then R_1 and R_2 are determined from (*4.3*). Generally, R_S will be comparable in magnitude to R_D. To obtain desirable ac gains, a bypass capacitor must be used with R_S, and an ac load line introduced; they are analyzed with techniques similar to those of Section 3.7.

5.6. PARAMETER VARIATION ANALYSIS WITH SPICE

PSpice offers two features that allow direct study of circuit performance change due to parameter variation. The first of these features is simply called *sensitivity analysis*. It is invoked by a control statement of the following format:

.SENS *sensitive variable*

The *sensitive variable* can be any node voltage or the current through any independent voltage source. A table is generated in the output file that gives the sensitivity of the sensitive variable to each parameter (specified or default) in the model of all BJTs and diodes that are directly comparable with (*5.11*) and (*5.12*).

Example 5.9. For the amplifier of Fig. 5-1, use SPICE methods to determine the sensitivity of I_{CQ} to changes in β (*a*) if $R_B/\beta \ll R_E$ and (*b*) if $R_B/\beta \geq R_E$. Bias the transistor such that V_{CEQ} has approximately the same value for both cases.

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(*a*) The generic *npn* transistor of Example 3.2 is used. It is not necessary to add the current source I_{CBO} of Fig. 5-1 as the parameter *Isc* of the transistor model specifies the collector-base leakage current. Set $V_{BB} = -1\,\text{V}$, $V_{CC} = -15\,\text{V}$, $R_B = 2\,\text{k}\Omega$, $R_C = 5\,\text{k}\Omega$, and $R_E = 200\,\Omega$. The netlist code below describes the resulting circuit.

```
Ex5_9.CIR
VBB 0 1 -1V
VCC 0 4 -15V
RB  1 2 2kohm
RC  3 4 5kohm
RE  5 0 200ohm
Q 3 2 5 QNPNG
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=75V Cjc=10pF Cje=15pF)
.SENS I(VCC)
.PRINT DC IC(Q) IB(Q)
.END
```

Execute ⟨Ex5_9.CIR⟩ and examine the output file to find values for calculation of β.

$$\beta = \frac{\text{I(VCC)}}{\text{I(VBB)}} = \frac{1.568 \times 10^{-3}}{9.751 \times 10^{-6}} = 160.8$$

Hence,

$$\frac{R_B}{\beta} = \frac{2 \times 10^3}{160.8} = 12.4\,\Omega \ll R_B = 200\,\Omega$$

From the sensitivity output table, find $S_\beta = 6.127 \times 10^{-7}\,\text{A/unit}$.

(*b*) Edit ⟨Ex5_9.CIR⟩ to set $V_{BB} = -1.32$ and $R_B = 35\,\text{k}\Omega$. Leave other values unchanged. Execute ⟨Ex5_9.CIR⟩ to see that V(3, 5) = $V_{CEQ} = 6.86\,\text{V}$ [V(3) − V(5) from small signal bias solution in output file] which is approximately equal to the value of 6.84 V in part (*a*). With the same quiescent point, β is unchanged and

$$\frac{R_B}{\beta} = \frac{35 \times 10^3}{156.3} = 223.9\,\Omega > R_E = 200\,\Omega$$

From the sensitivity table in the output file, find $S_\beta = 4.945 \times 10^{-6}\,\text{A/unit}$. Thus, the sensitivity of I_{CQ} to variation in β has increased by a factor of 8 over the case of part (*a*) where $R_B/\beta \ll R_E$.

The second PSpice feature for convenient study of circuit performance change due to parameter variation is known as *worst-case analysis*. It is implemented by a control statement of the following format:

.WCASE *analysis type sensitive variable* YMAX DEVICES *device type*

The *analysis type* may be ac, dc, or transient as specified in the netlist code. The *sensitive variable* can be any current or voltage. The *device type* can be any element of the circuit that has a model explicitly appearing in the netlist code. The percentage deviation (DEV) for the parameter of interest must be specified within the model parameter list.

The worst-case analysis actually calculates the circuit performance at the extremes of operation rather than giving a projected change as results from the sensitivity analysis. Owing to the nonlinear nature of many device parameter changes, the worst-case analysis should be used if other than a small change in the operating point is anticipated to give a better accuracy than would result from sensitivity analysis.

Example 5.10. For the circuit of Fig. 5-1, let $V_{BB} = -1.32\,\text{V}$, $V_{CC} = -15\,\text{V}$, $R_B = 35\,\text{k}\Omega$, $R_C = 5\,\text{k}\Omega$, and $R_E = 200\,\Omega$. Use the *npn* transformer of Example 5.9, where the current source I_{CBO} is modeled by the parameter *Isc* = 10 fA. As in part (*b*) of Example 5.9, the transistor is biased for near-maximum symmetrical swing, but with

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$R_B/\beta > R_E$ so that its collector current I_{CQ} is significantly sensitive to changes in the value of β. Use SPICE methods to determine the worst-case change in I_{CQ} due to a 50 percent change in the value of β.

The transistor parameter list in the .MODEL statement must be modified from that of Example 5.9 to add the DEV = 50% immediately following Bf = 150 as shown in the netlist code that follows:

```
Ex5_10.CIR
VBB 0 1 -1.32V
VCC 0 4 -15V
RB  1 2 35kohm
RC  3 4 5kohm
RE  5 0 200ohm
Q 3  2 5 QNPNG
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ DEV 50% Br=3 RB=1ohm Rc=1ohm Va=75V Cjc=10pF Cje=15pF)
.DC VCC -15V -15V 1V
.WCASE DC IC(Q) YMAX DEVICES Q
.END
```

Execute ⟨Ex5_10.CIR⟩ and poll the output file to find the worst-case deviation is a 495 μA reduction of I_{CQ} which occurs for $\beta = 75$ or for 50 percent of the nominal value of β. Due to the nonlinear nature about the point of operation, the deviation for $\beta = 225$ or for 150% of the nominal value of β was the lesser deviation. The particular value of I_{CQ} for $\beta = 225$ can be determined by changing YMAX to MIN in the .WCASE statement, executing ⟨Ex5_10.CIR⟩, and examining the output file.

Solved Problems

5.1 Leakage current approximately doubles for every 10°C increase in the temperature of a transistor. If a Si transistor has $I_{CBO} = 500$ nA at 25°C, find its leakage current at 90°C.

$$I_{CBO} = (500 \times 10^{-9})2^{(90-25)/10} = (500 \times 10^{-9})(90.51) = 45.25\,\mu\text{A}$$

5.2 Sketch a set of common-emitter output characteristics for each of two different temperatures, indicating which set is for the higher temperature.

The CE collector characteristics of Fig. 3-3(*c*) are obtained as sets of points (I_C, V_{CE}) from the ammeter and voltmeter readings of Fig. 3-3(*a*). For each fixed value of I_B, $I_C = \beta I_B + (\beta + 1)I_{CBO}$ must increase with temperature, since I_{CBO} increases with temperature (Problem 5.1) and β is much less temperature sensitive than I_{CBO}. The resultant shift in the collector characteristics is shown in Fig. 5-4.

5.3 In the circuit of Fig. 3-13, a transistor that has $\beta = \beta_1$ is replaced with a transistor that has $\beta = \beta_2$. (*a*) Find an expression for the percentage change in collector current. (*b*) Will collector current increase or decrease in magnitude if $\beta_2 > \beta_1$? Neglect leakage current.

(*a*) By KVL,

$$V_{CC} = I_{BQ}R_B + V_{BEQ} + I_{EQ}R_E \tag{1}$$

Using (*3.2*) and (*3.4*) in (*1*) and rearranging lead to

$$V_{CC} - V_{BEQ} = (R_B + R_E)\frac{I_{CQ}}{\beta} + R_E I_{CQ} \tag{2}$$

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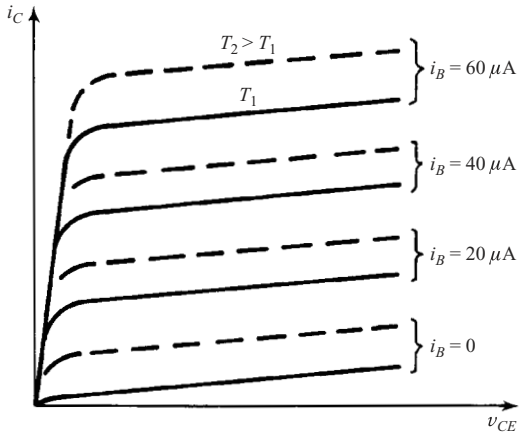


Fig. 5-4

This equation may be written for the original transistor (with $\beta = \beta_1$ and $I_{CQ} = I_{CQ1}$) and for the replacement transistor (with β_2 and I_{CQ2}). Subtracting the former from the latter then gives

$$0 = (R_B + R_E)\left(\frac{I_{CQ2}}{\beta_2} - \frac{I_{CQ1}}{\beta_1}\right) + R_E(I_{CQ2} - I_{CQ1}) \tag{3}$$

If we define $I_{CQ2} = I_{CQ1} + \Delta I_{CQ}$, then (3) can be rewritten as

$$0 = (R_B + R_E)\,\frac{\beta_1(I_{CQ1} + \Delta I_{CQ}) - \beta_2 I_{CQ1}}{\beta_1 \beta_2} + R_E\,\Delta I_{CQ}$$

which, when rearranged, gives the desired ratio:

$$\frac{\Delta I_{CQ}}{I_{CQ1}} = \frac{(\beta_2 - \beta_1)(R_B + R_E)}{\beta_1[R_B + (\beta_2 + 1)R_E]}\,(100\%) \tag{4}$$

(*b*) By inspection of (*4*), it is apparent that ΔI_{CQ} is positive for an increase in β ($\beta_2 > \beta_1$).

5.4 Use SPICE methods to show the sensitivity of β and V_{BEQ} as the operating temperature ranges from 0 to 125°C if the transistor is the *npn* device of Example 5.9.

The netlist code that follows establishes the desired sweep of temperature with $I_{BEQ} = \text{Ib}$ set at a reasonable value of 150 μA.

```
Prb5_4.CIR
Ib 0 1 150uA
Q 2 1 0 QNPNG
VC 2 0 15V
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=75V Cjc=10pF Cje=15pF)
.DC TEMP 0 125 5
.PROBE
.END
```

After executing ⟨Prb5_4.CIR⟩, use of the Probe feature of PSpice allows plotting of β versus temperature and V_{BEQ} versus temperature as shown by Fig. 5-5. Inspection of the plot shows that the variation of β with temperature is significantly less than 1%/°C, supporting the implication of Section 5.2 that it is the unit-to-

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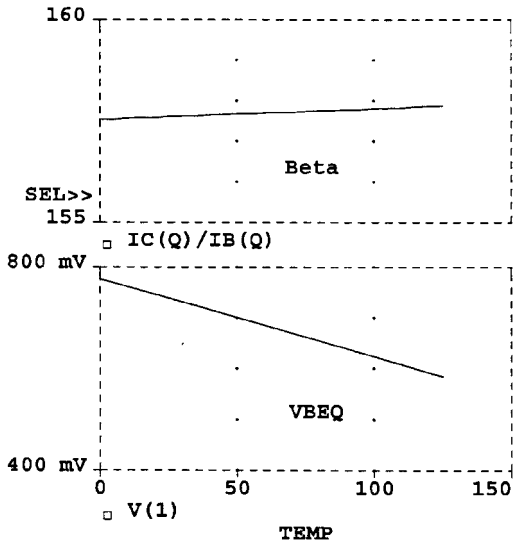


Fig. 5-5

unit variation of β rather than temperature that is of concern. However, the plot shows that the value of V_{BEQ} does change significantly with temperature as claimed in Section 5.2.

5.5 If the transistor of Problem 5.4 is supplied by a constant base current $I_{BEQ} = 75\,\mu$A, use SPICE methods to let β range from 50 to 200 and plot the resulting collector characteristics to show the impact of unit-to-unit variations in β.

The netlist code below sets β as a parameter to range from 50 to 200 in increments of 50.

```
Prb5_5.CIR
.PARAM Beta=0
Ib 0 1 75uA
Q 2 1 0 QNPNG
VC 2 0 0V
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf={Beta}
+ Br=3 Rb=1ohm Rc=1ohm Va=75V Cjc=10pF Cje=15pF)
.DC VC 0V 15V 1V PARAM Beta 50 200 50
.PROBE
.END
```

After executing ⟨Prb5_5.CIR⟩, the plot of Fig. 5-6 is made using the Probe feature of PSpice. Inspection of the resulting plot shows that for a particular value of V_{CEQ} and I_{BQ}, the collector current I_{CQ} varies nearly directly with β; thus, the conclusion of Example 5.2 is substantiated by numerical example.

5.6 The transistor in the circuit of Fig. 3-19 is a Si device with $I_{CEO} \approx 0$. Let $V_{CC} = 18\,\text{V}$, $V_{EE} = 4\,\text{V}$, $R_E = 2\,\text{k}\Omega$, $R_C = 6\,\text{k}\Omega$, and $R_B = 25\,\text{k}\Omega$. Find I_{CQ} and V_{CEQ} (*a*) for $\beta = 50$ and (*b*) for $\beta = 100$.

(*a*) By KVL around the base-emitter loop,

$$V_{EE} - V_{BEQ} = I_{BQ}R_B + I_{EQ}R_E \tag{1}$$

We let $I_{BQ} = I_{CQ}/\beta$ and $I_{EQ} = I_{CQ}(\beta + 1)/\beta$ in (*1*) and rearrange to obtain

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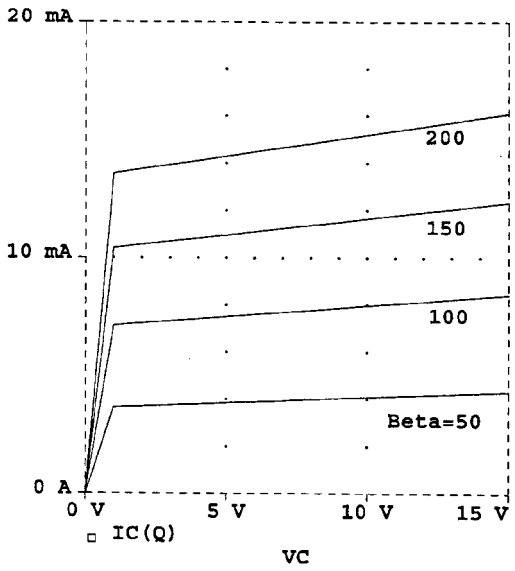


Fig. 5-6

$$I_{CQ} = \frac{V_{EE} - V_{BEQ}}{\frac{R_B}{\beta} + \frac{\beta+1}{\beta} R_E} = \frac{4 - 0.7}{\frac{25 \times 10^3}{50} + \frac{51}{50}(2 \times 10^3)} = 1.3\,\text{mA}$$

Then KVL around the collector loop with $I_{EQ} = I_{CQ}(\beta + 1)/\beta$ yields

$$V_{CEQ} = V_{CC} + V_{EE} - \left(R_C + \frac{\beta+1}{\beta} R_E\right) I_{CQ} = 18 + 4 - \left(6 + \frac{51}{50} 2\right)(1.3) = 11.55\,\text{V}$$

(*b*) For $\beta = 100$,

$$I_{CQ} = \frac{4 - 0.7}{25 \times 10^3/100 + (101/100)(2 \times 10^3)} = 1.45\,\text{mA}$$

$$V_{CEQ} = 18 + 4 - \left(6 + \frac{101}{100} 2\right)(1.45) = 10.37\,\text{V}$$

5.7 In the circuit of Fig. 3-19, under what condition will the bias current I_{CQ} be practically independent of β if $I_{CEO} \approx 0$?

With $\beta \gg 1$, the expression for I_{CQ} from Problem 5.6 gives

$$I_{CQ} = \frac{V_{EE} - V_{BEQ}}{\frac{R_B}{\beta} + \frac{\beta+1}{\beta} R_E} \approx \frac{V_{EE} - V_{BEQ}}{\frac{R_B}{\beta} + R_E}$$

It is apparent that I_{CQ} is practically independent of β if $R_B/\beta \ll R_E$. The inequality is generally considered to be satisfied if $R_B \leq \beta R_E/10$.

5.8 In the circuit of Fig. 3-23, the Si transistor has negligible leakage current, $V_{CC} = 15\,\text{V}$, $V_{EE} = 5\,\text{V}$, $R_E = 3\,\text{k}\Omega$, and $R_C = 7\,\text{k}\Omega$. Find I_{CQ}, I_{BQ}, and V_{CEQ} if (*a*) $\beta = 50$ and (*b*) $\beta = 100$.

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(*a*) KVL around the base loop yields

$$I_{EQ} = \frac{V_{EE} - V_{BEQ}}{R_E} = \frac{4 - 0.7}{3 \times 10^3} = 1.1\,\text{mA}$$

Now,
$$I_{CQ} = \frac{\beta}{\beta + 1} I_{EQ} = \frac{50}{51} 1.1 = 1.078\,\text{mA}$$

and
$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1.078 \times 10^{-3}}{50} = 21.56\,\mu\text{A}$$

and KVL around the collector loop gives

$$V_{CEQ} = V_{CC} + V_{EE} - I_{EQ}R_E - I_{CQ}R_C = 15 + 5 - (1.1)(3) - (1.078)(7) = 9.154\,\text{V}$$

(*b*) For $\beta = 100$, I_{EQ} is unchanged. However,

$$I_{CQ} = \frac{100}{101} 1.1 = 1.089\,\text{mA}$$

$$I_{BQ} = \frac{1.089 \times 10^{-3}}{100} = 10.89\,\mu\text{A}$$

and
$$V_{CEQ} = 15 + 5 - (1.1)(3) - (1.089)(7) = 9.077\,\text{V}$$

5.9 In the circuit of Fig. 3-14, let $V_{CC} = 15\,\text{V}$, $R_B = 500\,\text{k}\Omega$, and $R_C = 5\,\text{k}\Omega$. Assume a Si transistor with $I_{CBO} \approx 0$. (*a*) Find the β sensitivity factor S_β and use it to calculate the change in I_{CQ} when β changes from 50 to 100. (*b*) Compare your result with that of Example 5.1.

(*a*) By KVL,

$$V_{CC} = V_{BEQ} + I_{BQ}R_B = V_{BEQ} + \frac{I_{CQ}}{\beta} R_B$$

so that
$$I_{CQ} = \frac{\beta(V_{CC} - V_{BEQ})}{R_B}$$

and by (*5.10*),

$$S_\beta = \frac{\partial I_{CQ}}{\partial \beta} = \frac{V_{CC} - V_{BEQ}}{R_B} = \frac{15 - 0.7}{500 \times 10^3} = 28.6 \times 10^{-6}$$

According to (*5.13*), the change in I_{CQ} due to β alone is

$$\Delta I_{CQ} \approx S_\beta \Delta_\beta = (28.6 \times 10^{-6})(100 - 50) = 1.43\,\text{mA}$$

(*b*) From Example 5.1, we have

$$\Delta I_{CQ} = I_{CQ}|_{\beta=100} - I_{CQ}|_{\beta=50} = 2.86 - 1.43 = 1.43\,\text{mA}$$

Because I_{CQ} is of the first degree in β, (*5.13*) produces the exact change.

5.10 For the amplifier of Fig. 3-8, (*a*) find the β sensitivity factor and (*b*) show that the condition under which the β sensitivity factor is reduced to zero is identical to the condition under which the emitter current bias is constant.

(*a*) Since

$$I_{EQ} = \frac{I_{CQ}}{\alpha} = \frac{\beta + 1}{\beta} I_{CQ}$$

we have, from (*3.6*),

$$V_{BB} = I_{CQ} \frac{R_B}{\beta} + V_{BEQ} + \frac{\beta + 1}{\beta} I_{CQ}R_E$$

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Rearranging gives

$$I_{CQ} = \frac{V_{BB} - V_{BEQ}}{\dfrac{R_B}{\beta} + \dfrac{\beta + 1}{\beta} R_E} = \frac{\beta(V_{BB} - V_{BEQ})}{R_B + (\beta + 1)R_E} \tag{1}$$

and, from (*5.10*),

$$S_\beta = \frac{\partial I_{CQ}}{\partial \beta} = \frac{(R_B + R_E)(V_{BB} - V_{BEQ})}{[R_B + (\beta + 1)R_E]^2} \tag{2}$$

(*b*) Note in (*2*) that $\lim_{\beta \to \infty} S_\beta = 0$. Now if $\beta \to \infty$ in (*1*), then $I_{CQ} \approx (V_{BB} - V_{BEQ})/R_E = \text{constant}$.

5.11 Temperature variations can shift the quiescent point by affecting leakage current and base-to-emitter voltage. In the circuit of Fig. 5-1, $V_{BB} = 6\,\text{V}$, $R_B = 50\,\text{k}\Omega$, $R_E = 1\,\text{k}\Omega$, $R_C = 3\,\text{k}\Omega$, $\beta = 75$, $V_{CC} = 15\,\text{V}$, and the transistor is a Si device. Initially, $I_{CBO} = 0.5\,\mu\text{A}$ and $V_{BEQ} = 0.7\,\text{V}$, but the temperature of the device increases by 20°C. (*a*) Find the exact change in I_{CQ}. (*b*) Predict the new value of I_{CQ} using stability-factor analysis.

(*a*) Let the subscript 1 denote quantities at the original temperature T_1, and 2 denote quantities at $T_1 + 20°\text{C} = T_2$. By (*5.7*),

$$I_{CQ1} = \frac{V_{BB} - V_{BEQ1} + I_{CBO1}(R_B + R_E)}{R_B/\beta + R_E} = \frac{6 - 0.7 + (0.5 \times 10^{-6})(51 \times 10^3)}{50 \times 10^3/75 + 1 \times 10^3} = 3.1953\,\text{mA}$$

Now, according to Section 5.2,

$$I_{CBO2} = I_{CBO1} 2^{\Delta T/10} = 0.5 \times 10^{-6} 2^{20/10} = 2\,\mu\text{A}$$

$$\Delta V_{BEQ} = -2 \times 10^{-3}\,\Delta T = (-2 \times 10^{-3})(20) = -0.04\,\text{V}$$

so

$$V_{BEQ2} = V_{BEQ1} + \Delta V_{BEQ} = 0.7 - 0.04 = 0.66\,\text{V}$$

Again by (*5.7*),

$$I_{CQ2} = \frac{V_{BB} - V_{BEQ2} + I_{CBO2}(R_B + R_E)}{R_B/\beta + R_E} = \frac{6 - 0.66 + (2 \times 10^{-6})(51 \times 10^3)}{50 \times 10^3/75 + 1 \times 10^3} = 3.2652\,\text{mA}$$

Thus,

$$\Delta I_{CQ} = I_{CQ2} - I_{CQ1} = 3.2652 - 3.1953 = 0.0699\,\text{mA}$$

(*b*) By (*5.16*) and (*5.17*),

$$S_I = \frac{R_B + R_E}{R_B/\beta + R_E} = \frac{50 + 1}{50/75 + 1} = 30.6$$

$$S_V = \frac{-\beta}{R_B + \beta R_E} = \frac{-75}{50 \times 10^3 + (75)(1 \times 10^3)} = -0.6 \times 10^{-3}$$

Then, according to (*5.13*),

$$\Delta I_{CQ} \approx S_I\,\Delta I_{CBO} + S_V\,\Delta V_{BEQ} = (30.6)(1.5 \times 10^{-6}) + (-0.6 \times 10^{-3})(-0.04) = 0.0699\,\text{mA}$$

and

$$I_{CQ2} = I_{CQ1} + \Delta I_{CQ} = 3.1953 + 0.0699 = 3.2652\ \text{mA}$$

5.12 In Problem 5.11, assume that the given values of I_{CBO} and V_{BEQ} are valid at 25°C (that is, that $T_1 = 25°\text{C}$). (*a*) Use stability-factor analysis to find an expression for the change in collector current resulting from a change to any temperature T_2. (*b*) Use that expression to find ΔI_{CQ} when $T_2 = 125°\text{C}$. (*c*) What percentage of the change in I_{CQ} is attributable to a change in leakage current?

(*a*) Recalling that leakage current I_{CBO} doubles for each 10°C rise in temperature, we have

$$\Delta I_{CBO} = I_{CBO}|_{T_2} - I_{CBO}|_{T_1} = I_{CBO}|_{25°\text{C}}(2^{(T_2 - 25)/10} - 1)$$

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Since V_{BEQ} for a Si device decreases by 2 mV/°C, we have

$$\Delta V_{BEQ} = -0.002(T_2 - 25)$$

Now, substituting S_I and S_V as determined in Problem 5.11 into (*5.13*), we obtain

$$\begin{aligned}\Delta I_{CQ} &= S_I \Delta I_{CBO} + S_V \Delta V_{BEQ} \\ &= \frac{\beta(R_B + R_E)}{R_B + \beta R_E} I_{CBO}|_{25^\circ C}(2^{(T_2-25)/10} - 1) + \frac{\beta}{R_B + \beta R_E}(0.002)(T_2 - 25)\end{aligned}$$

(*b*) At $T_2 = 125$°C, with the values of Problem 5.11, this expression for ΔI_{CQ} gives

$$\begin{aligned}\Delta I_{CQ} &= (30.6)(0.5 \times 10^{-6})(2^{(125-25)/10} - 1) + (0.0006)(0.002)(125 - 25) \\ &= 15.65\,\text{mA} + 0.12\,\text{mA} = 15.77\,\text{mA}\end{aligned}$$

(*c*) From part *b*, the percentage of ΔI_{CQ} due to I_{CBO} is (15.65/15.77)(100) = 99.24 percent.

5.13 In the constant-base-current-bias circuit arrangement of Fig. 5-7, the leakage current is explicitly modeled as a current source I_{CBO}. (*a*) Find I_{CQ} as a function of I_{CBO}, V_{BEQ}, and β. (*b*) Determine the stability factors that should be used in (*5.13*) to express the influence of I_{CBO}, V_{BEQ}, and β on I_{CQ}.

(*a*) By KVL,

$$V_{CC} = I_{BQ}R_b + I_{EQ}R_E \tag{1}$$

Substitution of (*5.5*) and (*5.6*) into (*1*) and rearrangement give

$$I_{CQ} \approx \frac{V_{CC} - V_{BEQ} + I_{CBO}(R_b + R_E)}{R_b/\beta + R_E} \tag{2}$$

(*b*) Based on the symmetry between (*2*) and (*5.7*) we have, from Example 5.6,

$$S_I = \frac{R_b + R_E}{R_b/\beta + R_E} \qquad S_V = \frac{-\beta}{R_b + \beta R_E} \qquad S_\beta = \frac{R_b[V_{CC} - V_{BEQ} + I_{CBO}(R_b + R_E)]}{(R_b + \beta R_E)^2}$$

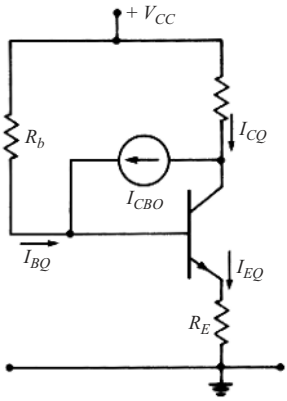


Fig. 5-7

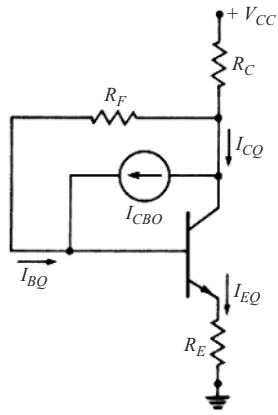


Fig. 5-8

5.14 In the shunt-feedback bias arrangement of Fig. 5-8, the leakage current is explicitly shown as a current source I_{CBO}. (*a*) Find I_{CQ} as a function of I_{CBO}, V_{BEQ}, and β. (*b*) Determine the stability factors that should be used in (*5.13*) to express the influence of I_{CBO}, V_{BEQ}, and β on I_{CQ}.

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(*a*) By KVL,

$$V_{CC} = I_{CQ}R_C + I_{BQ}(R_C + R_F) + V_{BEQ} + I_{EQ}R_E \tag{1}$$

Substituting (*5.5*) and (*5.6*) into (*1*), rearranging, and then assuming $\beta \gg 1$, we obtain

$$I_{CQ} \approx \frac{V_{CC} - V_{BEQ} + I_{CBO}(R_C + R_F + R_E)}{\dfrac{\beta+1}{\beta}R_C + \dfrac{R_F}{\beta} + R_E} \approx \frac{V_{CC} - V_{BEQ} + I_{CBO}(R_C + R_F + R_E)}{R_F/\beta + R_C + R_E} \tag{2}$$

(*b*) Based on the symmetry between (*2*) and (*5.7*) we have, from Example 5.6,

$$S_I = \frac{R_C + R_F + R_E}{R_F/\beta + R_C + R_E} \qquad S_V = \frac{-\beta}{R_F + \beta(R_C + R_E)}$$
$$S_\beta = \frac{R_F[V_{CC} - V_{BEQ} + I_{CBO}(R_C + R_F + R_E)]}{[R_F + \beta(R_C + R_E)]^2}$$

5.15 In the CB amplifier of Fig. 5-9, the transistor leakage current is shown explicitly as a current source I_{CBO}. (*a*) Find I_{CQ} as a function of I_{CBO}, V_{BEQ}, and β. (*b*) Determine the stability factors that should be used in (*5.13*) to express the influence of I_{CBO}, V_{BEQ}, and β on I_{CQ}.

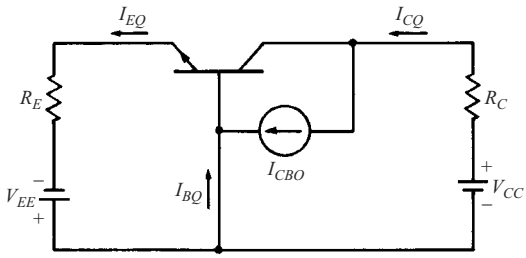


Fig. 5-9

(*a*) By KVL,

$$V_{EE} = V_{BEQ} + I_{EQ}R_E \tag{1}$$

Substituting (*5.5*) into (*1*) and rearranging yield

$$I_{CQ} = \frac{\beta+1}{\beta}\frac{V_{EE} - V_{BEQ}}{R_E} + I_{CBO} \tag{2}$$

(*b*) Direct application of (*5.10*) through (*5.12*) to (*2*) gives the desired stability factors as

$$S_\beta = \frac{\partial I_{CQ}}{\partial \beta} = -\frac{1}{\beta^2}\frac{V_{EE} - V_{BEQ}}{R_E} \qquad S_I = \frac{\partial I_{CQ}}{\partial I_{CBO}} = 1 \qquad S_V = \frac{\partial I_{CQ}}{\partial V_{BEQ}} = -\frac{\beta+1}{\beta R_E}$$

5.16 The CB amplifier of Fig. 5-9 has $V_{CC} = 15\,\text{V}$, $V_{EE} = 5\,\text{V}$, $R_E = 3\,\text{k}\Omega$, $R_C = 7\,\text{k}\Omega$, and $\beta = 50$. At a temperature of 25°C, the Si transistor has $V_{BEQ} = 0.7\,\text{V}$ and $I_{CBO} = 0.5\,\mu\text{A}$. (*a*) Find an expression for I_{CQ} at any temperature. (*b*) Evaluate that expression at $T = 125°\text{C}$.

(*a*) Let the subscript 1 denote quantities at $T_1 = 25°\text{C}$, and 2 denote them at any other temperature T_2. Then, according to Section 5.2,

$$I_{CBO2} = 2^{(T_2-25)/10} I_{CBO1}$$
$$V_{BEQ2} = V_{BEQ1} + \Delta V_{BEQ} = V_{BEQ1} - 0.002(T_2 - 25)$$

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Hence, by (*2*) of Problem 5.15,

$$I_{CQ2} = \frac{\beta + 1}{\beta} \frac{V_{EE} - V_{BEQ1} + 0.002(T_2 - 25)}{R_E} + 2^{(T_2 - 25)/10} I_{CBO1} \tag{1}$$

(*b*) At $T_2 = 125°C$, (*1*) gives us

$$I_{CQ2} = \frac{51}{50} \frac{5 - 0.7 + (0.002)(125 - 25)}{3 \times 10^3} + (2^{(125-25)/10})(0.5 \times 10^{-6}) = 1.53 + 0.512 = 2.042\,\text{mA}$$

5.17 For the Darlington-pair emitter-follower of Fig. 5-10, find I_{CQ1} as a function of the six temperature-sensitive variables $I_{CBO1}, I_{CBO2}, V_{BEQ1}, V_{BEQ2}, \beta_1$, and β_2.

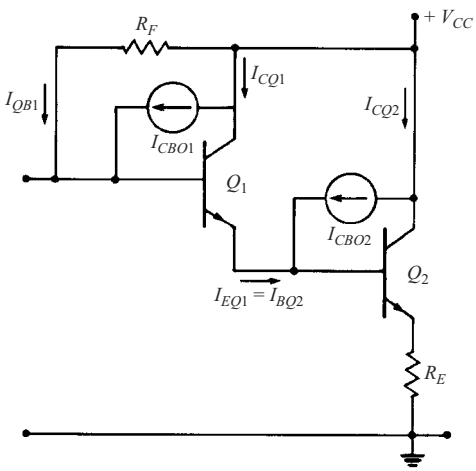


Fig. 5-10

By KVL,

$$V_{CC} = I_{BQ1} R_F + V_{BEQ1} + V_{BEQ2} + I_{EQ2} R_E \tag{1}$$

By KCL,

$$I_{EQ2} = I_{EQ1} + I_{CQ2} \tag{2}$$

Using the result of Problem 3.36 in (*2*) and then substituting $I_{BQ2} = I_{EQ1}$, we obtain

$$I_{EQ2} = I_{EQ1} + \beta_2 I_{BQ2} + (\beta_2 + 1) I_{CBO2} = (\beta_2 + 1) I_{EQ1} + (\beta_2 + 1) I_{CBO2}$$

Assuming $\beta_1, \beta_2 \gg 1$ and substituting for I_{EQ1} according to (*5.5*), we obtain

$$I_{EQ2} \approx (\beta_2 + 1) I_{CQ1} + (\beta_2 + 1)(I_{CBO2} - I_{CBO1}) \tag{3}$$

Also, from (*5.6*),

$$I_{BQ1} \approx \frac{I_{CB1}}{\beta_1} - I_{CBO1} \tag{4}$$

Now we substitute (*3*) and (*4*) into (*1*) and rearrange to get

$$I_{CQ1} = \frac{V_{CC} - V_{BEQ1} - V_{BEQ2} + I_{CBO1}(R_F + \beta_2 R_E) - I_{CBO2} \beta_2 R_E}{R_F/\beta_1 + \beta_2 R_E} \tag{5}$$

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5.18 (*a*) Determine a first-order approximation for the change in I_{CQ1} in the circuit of Fig. 5-10, in terms of the six variables $I_{CBO1}, I_{CBO2}, V_{BEQ1}, V_{BEQ2}, \beta_1$, and β_2. (*b*) Use I_{CQ1} as found in Problem 5.17 to evaluate the sensitivity factors (that is, the coefficients) in the expression determined in part *a*.

(*a*) Since $I_{CQ1} = f(I_{CBO1}, I_{CBO2}, V_{BEQ1}, V_{BEQ2}, \beta_1, \beta_2)$, its total differential is given by

$$dI_{CQ1} = \frac{\partial I_{CQ1}}{\partial I_{CBO1}} dI_{CBO1} + \frac{\partial I_{CQ1}}{\partial I_{CBO2}} dI_{CBO2} + \frac{\partial I_{CQ1}}{\partial V_{BEQ1}} dV_{BEQ1} + \frac{\partial I_{CQ1}}{\partial V_{BEQ2}} dV_{BEQ2} + \frac{\partial I_{CQ1}}{\partial \beta_1} d\beta_1 + \frac{\partial I_{CQ1}}{\partial \beta_2} d\beta_2 \tag{1}$$

Using the method of Section 5.3, we may write this as

$$\Delta I_{CQ1} \approx S_{I1}\,\Delta I_{CBO1} + S_{I2}\,\Delta I_{CBO2} + S_{V1}\,\Delta V_{BEQ1} + S_{V2}\,\Delta V_{BEQ2} + S_{\beta 1}\,\Delta\beta_1 + S_{\beta 2}\,\Delta\beta_2 \tag{2}$$

(*b*) The sensitivity factors in (*1*) may be evaluated with the use of (*5*) of Problem 5.17:

$$S_{I1} = \frac{\partial I_{CQ1}}{\partial I_{CBO1}} = \frac{R_F + \beta_2 R_E}{R_F/\beta_1 + \beta_2 R_E}$$

$$S_{I2} = \frac{\partial I_{CQ1}}{\partial I_{CBO2}} = \frac{-\beta_2 R_E}{R_F/\beta_1 + \beta_2 R_E}$$

$$S_{V1} = \frac{\partial I_{CQ1}}{\partial V_{BEQ1}} = \frac{-1}{R_F/\beta_1 + \beta_2 R_E} = S_{V2} = \frac{\partial I_{CQ1}}{\partial V_{BEQ2}}$$

$$S_{\beta 1} = \frac{\partial I_{CQ1}}{\partial \beta_1} = \frac{R_F[V_{CC} - V_{BEQ1} - V_{BEQ2} + I_{CBO1}(R_F + \beta_2 R_E) - I_{CBO2}\beta_2 R_E]}{(R_F + \beta_1\beta_2 R_E)^2}$$

$$S_{\beta 2} = \frac{\partial I_{CQ2}}{\partial \beta_2} = \frac{\beta_1 R_E[R_F(I_{CBO1} - I_{CBO2}) - \beta_1(V_{CC} - V_{BEQ1} - V_{BEQ2} + I_{CBO1}R_F)]}{(R_F + \beta_1\beta_2 R_E)^2}$$

5.19 It is possible that variations in passive components will have an effect on transistor bias. In the circuit of Fig. 3-8(*a*), let $R_1 = R_C = 500\,\Omega$, $R_2 = 5\,\text{k}\Omega$, $R_E = 100 \pm 10\,\Omega$, $\beta = 75$, $I_{CBO} = 0.2\,\mu\text{A}$, $V_{CC} = 20\,\text{V}$. (*a*) Find an expression for the change in I_{CQ} due to a change in R_E alone. (*b*) Predict the change that will occur in I_{CQ} as R_E changes from the minimum to the maximum allowable value.

(*a*) We seek a stability factor

$$S_{RE} = \frac{\partial I_{CQ}}{\partial R_E} \qquad \text{such that} \qquad \Delta I_{CQ} \approx S_{RE}\,\Delta R_E$$

Starting with I_{CQ} as given by (*5.7*), we find

$$S_{RE} = \frac{\partial I_{CQ}}{\partial R_E} = \frac{\beta(R_B + \beta R_E)I_{CBO} - \beta^2[V_{BB} - V_{BEQ} + I_{CBO}(R_B + R_E)]}{(R_B + \beta R_E)^2}$$

$$= \frac{\beta R_B I_{CBO} - \beta^2(V_{BB} - V_{BEQ} + I_{CBO}R_B)}{(R_B + \beta R_E)^2}$$

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(*b*) We first need to evaluate S_{RE} at $R_E = 100 - 10 = 90\,\Omega$:

$$R_B = R_1 \| R_2 = 454.5\,\Omega$$

$$V_{BB} = \frac{R_1}{R_1 + R_2} V_{CC} = \frac{500}{5500} 20 = 1.818\,\text{V}$$

and

$$S_{RE} = \frac{75(454.5)(0.2 \times 10^{-6}) - (75)^2[1.818 - 0.7 + (0.2 \times 10^{-6})(454.5)]}{(454.5 + 75 \times 90)^2}$$

$$= -1.212 \times 10^{-4}\,\text{A}/\Omega$$

Then

$$\Delta I_{CQ} = S_{RE}\,\Delta R_E = (-1.212 \times 10^{-4})(110 - 90) = -2.424\,\text{mA}$$

5.20 The circuit of Fig. 5-11 includes nonlinear diode compensation for variations in V_{BEQ}. (*a*) Neglecting I_{CBO}, find an expression for I_{CQ} that is a function of the temperature-sensitive variables β, V_{BEQ}, and V_D. (*b*) Show that if V_{BEQ} and V_D are equal, then the sensitivity of I_{CQ} to changes in V_{BEQ} is zero. (*c*) Show that it is not necessary that $V_{BEQ} = V_D$, but only (and less restrictively) that $dV_{BEQ}/dT = dV_D/dT$, to ensure the insensitivity of I_{CQ} to temperature T.

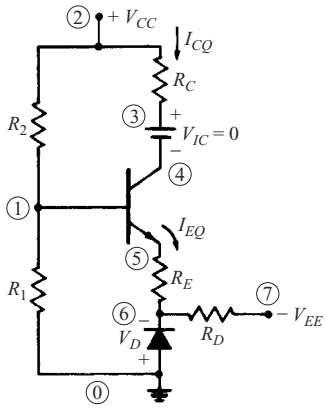


Fig. 5-11

(*a*) The usual Thévenin equivalent can be used to replace the R_1-R_2 voltage divider. Then, by KVL,

$$V_{BB} = R_B I_{BQ} + V_{BEQ} + I_{EQ} R_E - V_D \tag{1}$$

Substitution of $I_{BQ} = I_{CQ}/\beta$ and $I_{EQ} = I_{CQ}(\beta + 1)/\beta$ into (*1*) and rearranging yield

$$I_{CQ} = \frac{\beta[V_{BB} - (V_{BEQ} - V_D)]}{R_B + (\beta + 1)R_E} \tag{2}$$

(*b*) From (*2*) it is apparent that if $V_D = V_{BEQ}$, then I_{DQ} is independent of variations in V_{BEQ}.

(*c*) If β is independent of temperature, differentiation of (*2*) with respect to T results in

$$\frac{dI_{CQ}}{dT} = \frac{\beta}{R_B + (\beta + 1)R_E}\left(\frac{dV_D}{dT} - \frac{dV_{BEQ}}{dT}\right)$$

Hence, if $dV_D/dT = dV_{BEQ}/dT$, I_{CQ} is insensitive to temperature.

5.21 For the diode compensated circuit of Fig. 5-11, $V_{CC} = 15\,\text{V}$, $V_{EE} = 4\,\text{V}$, $R_1 = 100\,\Omega$, $R_2 = 20\,\text{k}\Omega$, $R_C = 15\,\Omega$, $R_E = 200\,\Omega$, and $R_D = 2\,\text{k}\Omega$. Use SPICE methods to show that the collector current I_{CQ} is reasonably insensitive to change in operating point temperature. Assume that the transistor is the device of Example 5.9 and that the diode is adequately described by the SPICE default model.

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Netlist code for the circuit is shown below:

```
Prb5_21.CIR
VCC 2 0 15V
VEE 0 7 4V
VIC 3 4 0V
R1  1 0 100ohm
R2  2 1 20kohm
RC  2 3 15kohm
RE  5 6 200ohm
RD  6 7 2kohm
D   0 6 DMOD
Q 4  1 5 QNPNG
.MODEL DMOD D()
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=75V Cjc=10pF Cje=15pF)
.DC TEMP 25 125 5
.PROBE
.END
```

After executing ⟨Prb5_21.CIR⟩, the plots of Fig. 5-12 can be generated showing that over the temperature range of 25 to 125°C, the quiescent collector current I_{CQ} changes by only 7.1 percent. Over the same temperature range, V_{BEQ} changes by 42.2 percent. To fully appreciate the temperature stabilization attained, one can edit the netlist code to replace the diode D by a 400 Ω resistor. This change results in approximately the same quiescent point for normal operating temperature but will show that I_{CQ} increases by more than 130 percent over the temperature range of 0 to 125°C.

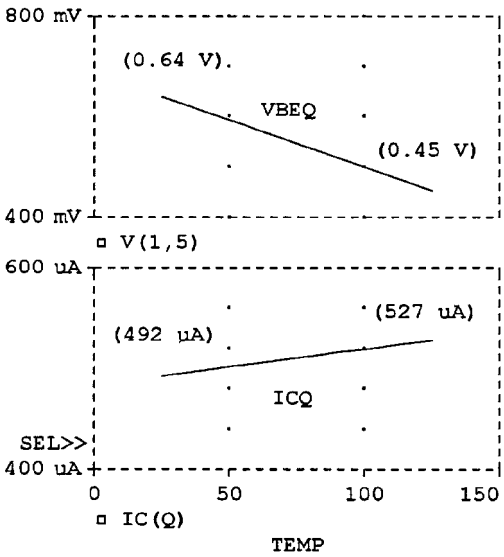


Fig. 5-12

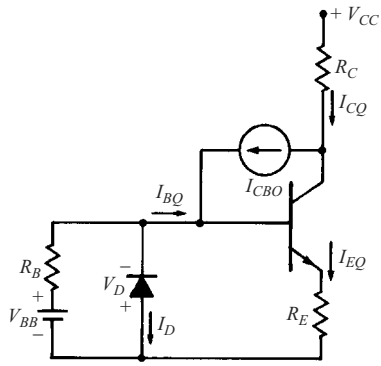


Fig. 5-13

5.22 The circuit of Fig. 5-13 includes nonlinear diode compensation for variations in I_{CBO}. (*a*) Find an expression for I_{CQ} as a function of the temperature-sensitive variables V_{BEQ}, β, I_{CBO}, and V_D. (*b*) What conditions will render I_{CQ} insensitive to changes in I_{CBO}?

(*a*) By KVL,

$$V_{BB} = (I_{BQ} + I_D)R_B + V_{BEQ} + I_{EQ}R_E$$

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Substitution for I_{EQ} and I_{BQ} via (*5.5*) and (*5.6*) and rearranging give

$$I_{CQ} = \frac{V_{BB} - V_{BEQ} + I_{CBO}(R_B + R_E) - I_D R_B}{R_B/\beta + R_E} \tag{1}$$

(*b*) According to (*1*), if $R_B \gg R_E$ and $I_D = I_{CBO}$, then I_{CQ} is, in essence, independent of I_{CBO}.

5.23 Show that if a second identical diode is placed in series with the diode of Example 5.8 (see Fig. 5-2), and if R_D is made equal in value to R_B, then the collector current ($I_{CQ} \approx I_{EQ}$) displays zero sensitivity to temperature changes that affect V_{BEQ}. Make the reasonable assumption that $\partial V_D/\partial T = \partial V_{BEQ}/\partial T$.

The equation we found for I_{CQ} in Example 5.8 describes I_{CQ} in this problem if V_D is replaced by $2V_D$; that gives

$$I_{CQ} \approx \frac{(V_{BB}R_D + 2V_D R_B)/(R_D + R_B) - V_{BEQ}}{(2R_D \| R_B)/\beta + R_E} \tag{1}$$

Assuming that only V_{BEQ} and V_D are temperature dependent, we have

$$\frac{\partial I_{CQ}}{\partial T} = \frac{\dfrac{2R_B}{R_D + R_B}\dfrac{\partial V_D}{\partial T} - \dfrac{\partial V_{BEQ}}{\partial T}}{(2R_D \| R_B)/\beta + R_E} \tag{2}$$

With $\partial V_D/\partial T = \partial V_{BEQ}/\partial T$ and $R_B = R_D$, (*2*) reduces to zero, indicating that I_{CQ} is not a function of temperature.

5.24 A JFET for which (*4.2*) holds is biased by the voltage-divider arrangement of Fig. 4-5. (*a*) Find I_{DQ} as a function of I_{DSS}, V_{p0}, and V_{GG}. (*b*) Find the total differential of I_{DQ}, and make reasonable linearity assumptions that allow you to replace differentials with increments so as to find an expression analogous to (*5.13*) for the JFET.

(*a*) We use (*4.4*) to find an expression for V_{GSQ} and then use (*4.2*) to obtain

$$I_{DQ} = I_{DSS}\left(1 + \frac{V_{GG} - I_{DQ}R_S}{V_{p0}}\right)^2 \tag{1}$$

which we can solve for I_{DQ}:

$$I_{DQ} = \frac{V_{GG} + V_{p0}}{R_S} + \frac{V_{p0}^2}{2R_S^2 I_{DSS}} \pm \frac{V_{p0}}{2R_S^2}\sqrt{\left(\frac{V_{p0}}{I_{DSS}}\right)^2 + \frac{4(V_{GG} + V_{p0})R_S}{I_{DSS}}} \tag{2}$$

(*b*) Since V_{GSQ} depends upon the bias network chosen, our result will have more general application if we take the differential of (*4.2*) and then specialize it to the case at hand, instead of taking the differential of (*2*). Assuming that I_{DSS}, V_{p0}, and V_{GSQ} are the independent variables, we have, for the total differential of (*4.2*),

$$dI_{DQ} = \frac{\partial I_{DQ}}{\partial I_{DSS}}\,dI_{DSS} + \frac{\partial I_{DQ}}{\partial V_{p0}}\,dV_{p0} + \frac{\partial I_{DQ}}{\partial V_{GSQ}}\,dV_{GSQ} \tag{3}$$

For the case at hand, V_{GSQ} is given by (*4.4*), from which

$$dV_{GSQ} = -R_S dI_{DQ} \tag{4}$$

Substituting (*4*) into (*3*) and rearranging, we find

$$dI_{DQ} = \frac{\partial I_{DQ}/\partial I_{DSS}}{1 + R_S \partial I_{DQ}/\partial V_{GSQ}}\,dI_{DSS} + \frac{\partial I_{DQ}/\partial V_{p0}}{1 + R_S \partial I_{DQ}/\partial V_{GSQ}}\,dV_{p0} \tag{5}$$

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The assumption of linearity allows us to replace the differentials in (*5*) with increments and define appropriate stability factors:

$$\Delta I_{DQ} \approx S_I \, \Delta I_{DSS} + S_V \, \Delta V_{p0} \tag{6}$$

$$S_I = \frac{\partial I_{DQ}/\partial I_{DSS}}{1 + R_S \partial I_{DQ}/\partial V_{GSQ}} = \frac{(1 + V_{GSQ}/V_{p0})^2}{1 + (2R_S I_{DSS}/V_{p0})(1 + V_{GSQ}/V_{p0})} \tag{7}$$

$$S_V = \frac{\partial I_{DQ}/\partial I_{DSS}}{1 + R_S \partial I_{DQ}/\partial V_{GSQ}} = \frac{-2I_{DSS}(1 + V_{GSQ}/V_{p0})(V_{GSQ}/V_{p0}^2)}{1 + (2R_S I_{DSS}/V_{p0})(1 + V_{GSQ}/V_{p0})} \tag{8}$$

5.25 The JFET of Fig. 4-5(*b*) is said to have *fixed bias* if $R_S = 0$. The worst-case shorted-gate parameters are given by the manufacturer of the device as

Value	I_{DSS}, mA	V_{p0}, V
maximum	8	6
minimum	4	3

Let $V_{DD} = 15\,\text{V}$, $V_{GG} = -1\,\text{V}$, and $R_D = 2.5\,\text{k}\Omega$. (*a*) Find the range of values of I_{DQ} that could be expected in using this FET. (*b*) Find the corresponding range of V_{DSQ}. (*c*) Comment on the desirability of this bias arrangement.

(*a*) The maximum and minimum transfer characteristics are plotted in Fig. 5-14, based on (*4.2*). Because $V_{GSQ} = V_{GG} = -1\,\text{V}$ is a fixed quantity unaffected by I_{DQ} and V_{DSQ}, the transfer bias line extends vertically at $V_{GS} = -1$, as shown. Its intersections with the two transfer characteristics give $I_{DQ\,\max} \approx 5.5\,\text{mA}$ and $I_{DQ\,\min} \approx 1.3\,\text{mA}$.

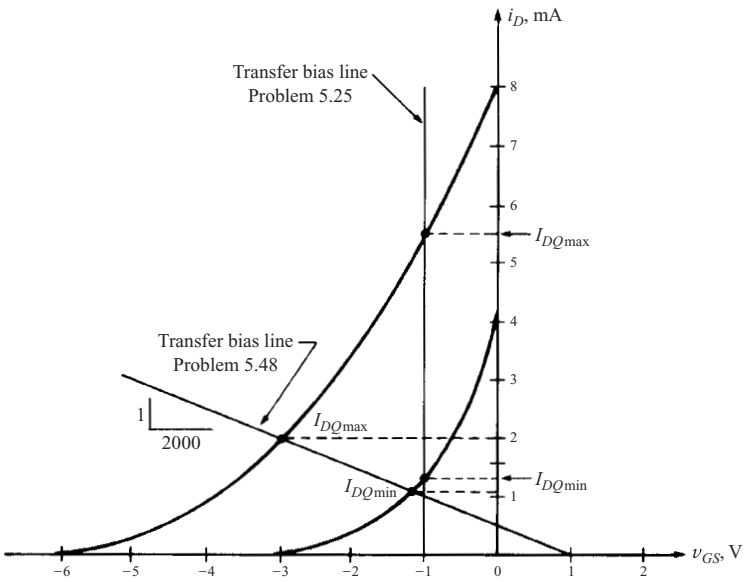


Fig. 5-14

(*b*) For $I_{DQ} = I_{DQ\,\max}$, KVL requires that

$$V_{DSQ\,\max} = V_{DD} - I_{DQ\,\max} R_D = 15 - (5.5)(2.5) = 1.25\,\text{V}$$

And, for $I_{DQ\,\min}$,

$$V_{DSQ\,\min} = V_{DD} - I_{DQ\,\min} R_D = 15 - (1.3)(2.5) = 11.75\,\text{V}$$

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(*c*) The spread in FET parameters (and thus in transfer characteristics) makes the fixed-bias technique an undesirable one: The value of the *Q*-point drain current can vary from near the ohmic region to near the cutoff region.

5.26 The self-biased JFET of Fig. 4-19 has a set of worst-case shorted-gate parameters that yield the plots of Fig. 5-15. Let $V_{DD} = 24\,\text{V}$, $R_D = 3\,\text{k}\Omega$, $R_S = 1\,\text{k}\Omega$, and $R_G = 10\,\text{M}\Omega$. (*a*) Find the range of I_{DQ} that can be expected. (*b*) Find the range of V_{DSQ} that can be expected. (*c*) Discuss the idea of reducing I_{DQ} variation by increasing the value of R_S.

(*a*) Since $V_{GG} = 0$, the transfer bias line must pass through the origin of the transfer characteristics plot, and its slope is $-1/R_S$ (solid line in Fig. 5-15). From the intersections of the transfer bias line and the transfer characteristics, we see that $I_{DQ\,\text{max}} \approx 2.5\,\text{mA}$ and $I_{DQ\,\text{min}} \approx 1.2\,\text{mA}$.

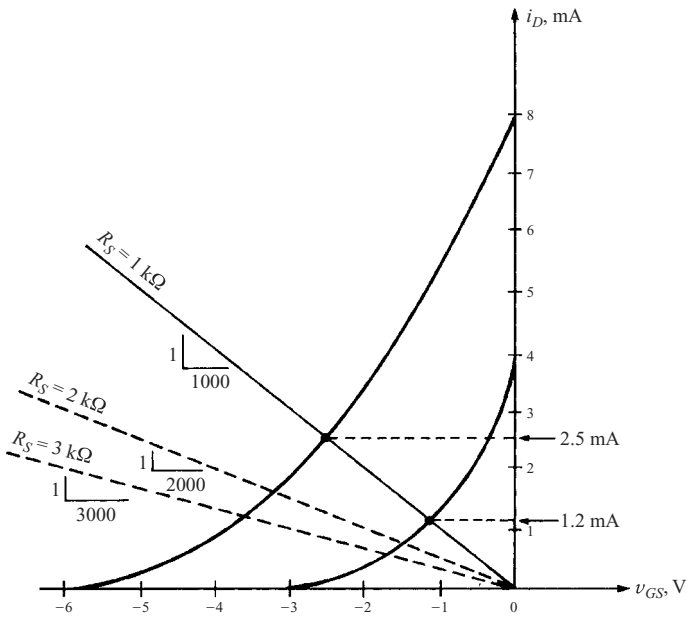


Fig. 5-15

(*b*) For $I_{DQ} = I_{DQ\,\text{max}}$, KVL requires that

$$V_{DSQ\,\text{max}} = V_{DD} - I_{DQ\,\text{max}}(R_S + R_D) = 24 - (2.5)(1 + 3) = 14\,\text{V}$$

And, for $I_{DQ\,\text{min}}$,

$$V_{DSQ\,\text{min}} = V_{DD} - I_{DQ\,\text{min}}(R_S + R_D) = 24 - (1.2)(1 + 3) = 19.2\,\text{V}$$

(*c*) The transfer bias lines for $R_S = 2\,\text{k}\Omega$ and $3\,\text{k}\Omega$ are also plotted on Fig. 5-15 (dashed lines). An increase in R_S obviously does decrease the difference between $I_{DQ\,\text{max}}$ and $I_{DQ\,\text{min}}$; however, in the process I_{DQ} is reduced to quite low values, so that operation is on the nonlinear portion of the drain characteristics near the ohmic region where appreciable signal distortion results. But if self-bias with an external source is utilized (see Problems 5.27 and 5.48), the transfer bias line can be given a small negative slope without forcing I_{DQ} to approach zero.

5.27 In the JFET circuit of Fig. 4-5(*a*), using self-bias with an external source, $V_{DD} = 24\,\text{V}$ and $R_S = 3\,\text{k}\Omega$. The JFET is characterized by worst-case shorted-gate parameters that result in

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the transfer characteristics of Fig. 5-16. (*a*) Find the range of I_{DQ} that can be expected if $R_1 = 1\,\text{M}\Omega$ and $R_2 = 3\,\text{M}\Omega$. (*b*) Find the range of I_{DQ} that can be expected if $R_1 = 1\,\text{M}\Omega$ and $R_2 = 7\,\text{M}\Omega$. (*c*) Discuss the significance of the results of parts *a* and *b*.

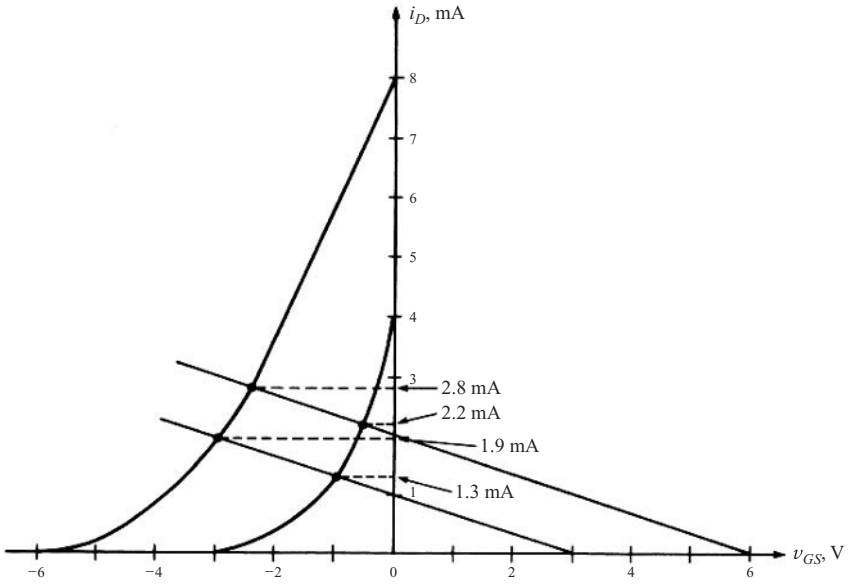


Fig. 5-16

(*a*) By (*4.3*),

$$V_{GG} = \frac{R_1}{R_1 + R_2} V_{DD} = \frac{1}{1+3} 24 = 6\,\text{V}$$

In this case the transfer bias line, shown on Fig. 5-16, has abscissa intercept $v_{GS} = V_{GG} = 6\,\text{V}$ and slope $-1/R_S$. The range of I_{DQ} is determined by the intersections of the transfer bias line and the transfer characteristics: $I_{DQ\,\text{max}} \approx 2.8\,\text{mA}$ and $I_{DQ\,\text{min}} \approx 2.2\,\text{mA}$.

(*b*) Again by (*4.3*),

$$V_{GG} = \frac{1}{1+7} 24 = 3\,\text{V}$$

The transfer bias line for this case is also drawn on Fig. 5-16; it has abscissa intercept $v_{GS} = V_{GG} = 3\,\text{V}$ and slope $-1/R_S$. Here $I_{DQ\,\text{max}} \approx 1.9\,\text{mA}$ and $I_{DQ\,\text{min}} \approx 1.3\,\text{mA}$.

(*c*) We changed V_{GG} by altering the R_1-R_2 voltage divider. This allowed us to maintain a small negative slope on the transfer bias line (and, thus, a small difference $I_{DQ\,\text{max}} - I_{DQ\,\text{min}}$) while shifting the range of I_{DQ}.

5.28 The MOSFET of Fig. 4-18 is an enhancement-mode device with worst-case shorted-gate parameters as follows:

Value	$I_{D(\text{on})}$, mA	V_T, V
maximum	8	4
minimum	4	2

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These parameter values lead to the transfer characteristics of Fig. 5-17 because the device may be assumed to obey (*4.6*). Let $V_{DD} = 24\,\text{V}$, $R_1 = 2\,\text{M}\Omega$, $R_2 = 2\,\text{M}\Omega$, $R_D = 1\,\text{k}\Omega$, and $R_S = 2\,\text{k}\Omega$. (*a*) Find the range of I_{DQ} that can be expected. (*b*) Find the range of V_{DSQ} to be expected. (*c*) Discuss a technique, suggested by parts *a* and *b*, for minimizing the range of I_{DQ} for this model of MOSFET.

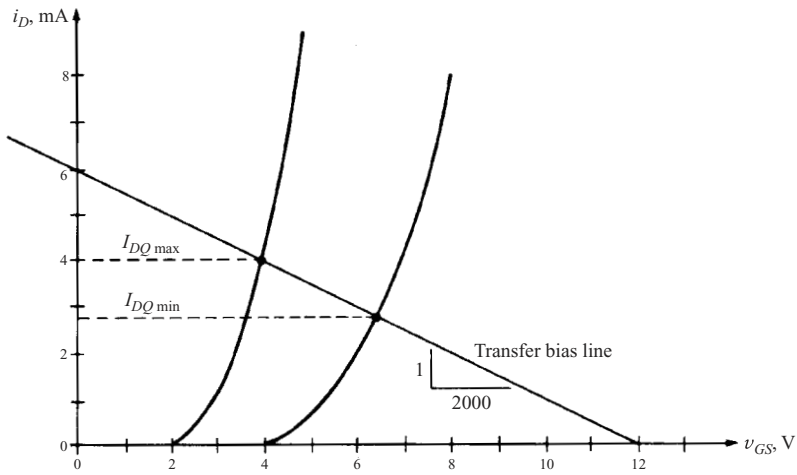


Fig. 5-17

(*a*) By (*4.3*),

$$V_{GG} = \frac{R_1}{R_1 + R_2} V_{DD} = \frac{2}{2+2} 24 = 12\,\text{V}$$

The transfer bias line, with abscissa intercept $v_{GS} = V_{GG} = 12\,\text{V}$ and slope $-1/R_S$, is drawn on Fig. 5-17. From the intersections of the transfer bias line with the transfer characteristics, we see that $I_{DQ\,\max} \approx 4\,\text{mA}$ and $I_{DQ\,\min} \approx 2.8\,\text{mA}$.

(*b*)
$$V_{DSQ\,\max} = V_{DD} - I_{DQ\,\max}(R_S + R_D) = 24 - (4)(2+1) = 12\,\text{V}$$
$$V_{DSQ\,\min} = V_{DD} - I_{DQ\,\min}(R_S + R_D) = 24 - (2.8)(2+1) = 15.6\,\text{V}$$

(*c*) As in the case of the JFET, the range of I_{DQ} can be decreased by increasing R_S. However, to avoid undesirably small values for I_{DQ}, it is also necessary to increase V_{GG} by altering the R_1-R_2 voltage-divider ratio.

Supplementary Problems

5.29 In the constant-base-current-biased amplifier of Fig. 3-13, $V_{CC} = 15\,\text{V}$, $R_C = 2.5\,\text{k}\Omega$, $R_E = 500\,\Omega$, and $R_B = 500\,\text{k}\Omega$. $I_{CBO} \approx 0$ for the Si device. Find I_{CQ} and V_{CEQ} if (*a*) $\beta = 100$ and (*b*) $\beta = 50$.
Ans. (*a*) 2.6 mA, 7.19 V; (*b*) 1.36 mA, 11.09 V

5.30 Under what condition will the bias current I_{CQ} of the amplifier in Fig. 3-14 be practically independent of β? Is this condition practical?
Ans. $R_B/\beta \ll R_E$. It is not practical, as a value of R_B large enough to properly limit I_{BQ} leads, through the condition, to a value of R_E so large that it forces cutoff.

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5.31 The amplifier of Fig. 5-13 uses a Si transistor for which $I_{CBO} \approx 0$. Let $V_{CC} = 15\,\text{V}$, $R_C = 2.5\,\text{k}\Omega$, $R_E = 500\,\Omega$, and $R_B = 500\,\text{k}\Omega$. (*a*) Find the value of the β sensitivity factor $S_\beta = \partial I_{CQ}/\partial\beta$ for $\beta = 50$. (*b*) Use S_β to predict I_{CQ} when $\beta = 100$.

Ans. (*a*) $(R_B + R_E)(V_{CC} - V_{BEQ})/[R_B + (\beta + 1)R_E]^2$; (*b*) 2.65 mA (compare with the result of Problem 5.29)

5.32 (*a*) Solve Problem 3.28(*a*) if $\beta = 75$ and all else is unchanged. (*b*) Use the β sensitivity factor found in Problem 5.10 to predict the change in I_{CQ} when β changes from 110 to 75.

Ans. (*a*) $I_{CQ} = 4.77\,\text{mA}$; (*b*) $S_\beta = 3.643 \times 10^{-6}$, $\Delta I_{CQ} = -0.127\,\text{mA}$

5.33 In the shunt-feedback-biased amplifier of Fig. 3-17, $V_{CC} = 15\,\text{V}$, $R_C = 2\,\text{k}\Omega$, $R_F = 150\,\text{k}\Omega$, $I_{CEO} \approx 0$, and the transistor is a Si device. (*a*) Find an expression for the β sensitivity factor S_β. (*b*) Use S_β to predict the change in quiescent collector current due to a change in β from 50 to 100.

Ans. (*a*) $S_\beta = (R_F + R_C)(V_{CC} - V_{BEQ})/[R_F + (\beta + 1)R_C]^2$; (*b*) $S_\beta = 3.432 \times 10^{-5}$, $\Delta I_{CQ} = 1.71\,\text{mA}$ (compare with Example 5.4)

5.34 In the CB amplifier of Fig. 3-23, $V_{CC} = 15\,\text{V}$, $V_{EE} = 5\,\text{V}$, $R_E = 3\,\text{k}\Omega$, $R_C = 7\,\text{k}\Omega$, and $\beta = 50$. (*a*) Find an expression for the β sensitivity factor S_β. (*b*) Evaluate S_β assuming the transistor is a Si device.

Ans. (*a*) $S_\beta = (V_{EE} - V_{BEQ})/(\beta + 1)^2 R_E$; (*b*) $S_\beta = 5.51 \times 10^{-7}$ (very low sensitivity, but see Problem 5.8)

5.35 The circuit of Fig. 5-1 has the values given in Problem 5.11; assume that the initial values of I_{CBO} and V_{BEQ} are for 25°C. (*a*) Find an expression for the value of I_{CQ} at any temperature $T_2 \geq 25°\text{C}$ if the transistor is a Si device. (*b*) Evaluate the expression for I_{CQ} at $T_2 = 125°\text{C}$.

Ans. (*a*) $$I_{CQ} = \frac{V_{BB} - 0.7 + 0.002(T_2 - 25) + (0.5 \times 10^{-6})(R_B + R_E)2^{(T_2-25)/10}}{(R_B/\beta + R_E)};$$

(*b*) $I_{CQ} = 18.97\,\text{mA}$

5.36 The constant-base-current-biased amplifier of Fig. 5-7 contains a Si transistor. Let $V_{CC} = 15\,\text{V}$, $R_C = 2.5\,\text{k}\Omega$, $R_E = 500\,\Omega$, $R_b = 500\,\text{k}\Omega$, and $\beta = 100$. At 25°C, $I_{CBO} = 0.5\,\mu\text{A}$ and $V_{BEQ} = 0.7\,\text{V}$. (*a*) Find the exact change in I_{CQ} if the temperature changes to 100°C. (*b*) Use the stability factors developed in Problem 5.13 to predict ΔI_{CQ} for a temperature increase to 100°C.

Ans. (*a*) $\Delta I_{CQ} = I_{CQ2} - I_{CQ1} = 10.864 - 2.645 = 8.219\,\text{mA}$; (*b*) $\Delta I_{CQ} = 8.22\,\text{mA}$

5.37 In the constant-base-current-biased amplifier of Fig. 5-7, the Si transistor is characterized by $I_{CBO} = 0.5\,\mu\text{A}$ and $V_{BEQ} = 0.7\,\text{V}$ at 25°C. (*a*) Find an expression for I_{CQ} at any temperature $T_2 \geq 25°\text{C}$. (*b*) Evaluate I_{CQ} at 100°C if $V_{CC} = 15\,\text{V}$, $R_C = 2.5\,\text{k}\Omega$, $R_E = 500\,\Omega$, $R_b = 500\,\text{k}\Omega$, and $\beta = 100$.

Ans. (*a*) $$I_{CQ} = \frac{V_{CC} - 0.7 + 0.002(T_2 - 25) + (0.5 \times 10^{-6})(R_b + R_E)2^{(T_2-25)/10}}{R_b/\beta + R_E};$$

(*b*) $I_{CQ} = 10.864\,\text{mA}$

5.38 In the current-feedback-biased amplifier of Fig. 5-8, $V_{CC} = 15\,\text{V}$, $R_C = 1.5\,\text{k}\Omega$, $R_F = 150\,\text{k}\Omega$, $R_E = 500\,\Omega$, and $\beta = 100$. $I_{CBO} = 0.2\,\mu\text{A}$ and $V_{BEQ} = 0.7\,\text{V}$ at 25°C for this Si transistor. (*a*) Find the exact change in I_{CQ} when the temperature changes to 125°C. (*b*) Use the stability factors developed in Problem 5.14 to predict ΔI_{CQ} when the temperature is 125°C. *Ans.* (*a*) $\Delta I_{CQ} = 8.943\,\text{mA}$; (*b*) $\Delta I_{CQ} = 8.943\,\text{mA}$

5.39 The shunt-feedback-biased amplifier of Fig. 5-8 uses a Si transistor for which $I_{CBO} = 0.2\,\mu\text{A}$ and $V_{BEQ} = 0.7\,\text{V}$ at 25°C. (*a*) Find an expression for I_{CQ} at any temperature $T_2 \geq 25°\text{C}$. (*b*) Evaluate I_{CQ} at $T_2 = 125°\text{C}$ if $V_{CC} = 15\,\text{V}$, $R_C = 1.5\,\text{k}\Omega$, $R_F = 150\,\text{k}\Omega$, $R_E = 500\,\Omega$, and $\beta = 100$.

Ans. (*a*) $$I_{CQ} = \frac{V_{CC} - 0.7 + 0.002(T_2 - 25) + (0.2 \times 10^{-6})(R_C + R_F + R_E)2^{(T_2-25)/10}}{R_F/\beta + R_C + R_E};$$

(*b*) $I_{CQ} = 13.037\,\text{mA}$

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5.40 In the CB amplifier of Fig. 5-9, $V_{CC} = 15\,\text{V}$, $V_{EE} = 5\,\text{V}$, $R_E = 3\,\text{k}\Omega$, $R_C = 7\,\text{k}\Omega$, and $\beta = 50$. For the Si transistor, $I_{CBO} = 0.5\,\mu\text{A}$ and $V_{BEQ} = 0.7\,\text{V}$ at 25°C. (*a*) Find the exact change in I_{CQ} when the temperature changes to 125°C. (*b*) Use the stability factors developed in Problem 5.15 to predict ΔI_{CQ} for the same temperature change. *Ans.* (*a*) $\Delta I_{CQ} = 2.042 - 1.4625 = 0.5795\,\text{mA}$; (*b*) $\Delta I_{CQ} = 0.5769\,\text{mA}$

5.41 Sensitivity analysis can be extended to handle uncertainties in power-supply voltage. In the circuit of Fig. 3-8(*a*), let $R_1 = R_C = 500\,\Omega$, $R_2 = 5\,\text{k}\Omega$, $R_E = 100\,\Omega$, $\beta = 75$, $V_{BEQ} = 0.7\,\text{V}$, $I_{CBO} = 0.2\,\mu\text{A}$, and $V_{CC} = 20 \pm 2\,\text{V}$. (*a*) Find an expression for the change in I_{CQ} due to changes in V_{CC} alone. (*b*) Predict the change in I_{CQ} as V_{CC} changes from its minimum to its maximum value.
Ans. (*a*) $\Delta I_{CQ} = S_{VCC}\,\Delta V_{CC}$, where $S_{VCC} = [\beta R_1/(R_1 + R_2)]/[R_B + (\beta + 1)R_E]$; (*b*) $\Delta I_{CQ} = 3.428\,\text{mA}$

5.42 In the circuit of Fig. 5-11, $R_1 = R_C = 500\,\Omega$, $R_2 = 5\,\text{k}\Omega$, $R_E = 100\,\Omega$, $\beta = 75$, and $V_{CC} = 20\,\text{V}$. Leakage current is negligible. At 25°C, $V_{BEQ} = 0.7\,\text{V}$ and $V_D = 0.65\,\text{V}$; however, both change at a rate of $-2\,\text{mV/°C}$. (*a*) Find the exact change in I_{CQ} due to an increase in temperature to 125°C. (*b*) Use sensitivity-analysis to predict the change in I_{CQ} when the temperature increases to 125°C.
Ans. (*a*) $\Delta I_{CQ} = 0$; (*b*) $\Delta I_{CQ} = 0$

5.43 In Problem 5.24, it was assumed that V_{GG}, and hence V_{DD}, was constant. Suppose now that the power-supply voltage does vary, and find an expression for ΔI_{DQ} using stability factors.
Ans. $\Delta I_{DQ} \approx S_I\,\Delta I_{DSS} + S_V\,\Delta V_{p0} + S_{VGG}\,\Delta V_{GG}$, where

$$S_{VGG} = \frac{\partial I_{DQ}/\partial V_{GSQ}}{1 + R_S\,\partial I_{DQ}/\partial V_{GSQ}} = \frac{(2I_{DSS}/V_{p0})(1 + V_{GSQ}/V_{p0})}{1 + (2R_S I_{DSS}/V_{p0})(1 + V_{GSQ}/V_{p0})}$$

and S_I and S_V are given by (*7*) and (*8*) of Problem 5.24.

5.44 The MOSFET of Fig. 4-18 is characterized by $V_T = 4\,\text{V}$ and $I_{D(\text{on})} = 10\,\text{mA}$. The device obeys (*4.6*). Let $i_G \approx 0$, $R_1 = 0.4\,\text{M}\Omega$, $R_2 = 5\,\text{k}\Omega$, $R_S = 0$, $R_D = 2\,\text{k}\Omega$, and $V_{DD} = 20\,\text{V}$. (*a*) Find the exact change in I_{DQ} when the MOSFET is replaced with a new device characterized by $V_T = 3.8\,\text{V}$ and $I_{D(\text{on})} = 9\,\text{mA}$. (*b*) Find the change in I_{DQ} predicted by sensitivity analysis when the original device is replaced as in part *a*.
Ans. (*a*) $\Delta I_{DQ} = 2.836 - 3.402 = -0.566\,\text{mA}$; (*b*) $\Delta I_{DQ} = -0.548\,\text{mA}$

5.45 The circuit of Fig. 4-18 uses MOSFETs characterized by the device model of Example 4.6 except that V_T can vary ±10 percent from the nominal value of 4 V among different batches of MOSFETs. Use SPICE methods to determine the maximum change of I_{DQ} from the nominal value that can be expected. (*Netlist code available at author website.*) *Ans.* $\Delta I_{DQ} = 0.689\,\text{mA}$ for $V_T = 3.6\,\text{V}$

5.46 In the JFET amplifier of Fig. 4-5, $V_{DD} = 20\,\text{V}$, $R_1 = 1\,\text{M}\Omega$, $R_2 = 15.7\,\text{M}\Omega$, $R_D = 3\,\text{k}\Omega$, $R_S = 2\,\text{k}\Omega$, and $i_G \approx 0$. The JFET obeys (*4.2*) and is characterized by $I_{DSS} = 5\,\text{mA}$ and $V_{p0} = 5\,\text{V}$. Due to aging, the resistance of R_1 increases by 20 percent. (*a*) Find the exact change in I_{DQ} due to the increase in resistance. (*b*) Predict the change in I_{DQ} due to the increase in resistance, using sensitivity analysis.
Ans. (*a*) $\Delta I_{DQ} = 1.735 - 1.658 = 0.077\,\text{mA}$; (*b*) $\Delta I_{DQ} = S_{VGG}\,\Delta V_{GG} = 0.0776\,\text{mA}$

5.47 For a FET, the temperature dependence of V_{GSQ} is very small when I_{DQ} is held constant. Moreover, for constant V_{DSQ}, the temperature dependency of V_{GSQ} is primarily due to changes in the shorted-gate current; those changes are given by

$$I_{DSS} = I_{DSSO}(k\,\Delta T + 1.1) \tag{1}$$

where I_{DSSO} = value of I_{DSS} at 0°C
ΔT = change in temperature from 0°C
k = constant (typically $0.003^{\circ}\text{C}^{-1}$)

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For the JFET of Fig. 4-5; $V_{DD} = 20\,\text{V}$, $R_1 = 1\,\text{M}\Omega$, $R_2 = 15.7\,\text{M}\Omega$, $R_D = 3\,\text{k}\Omega$, $R_S = 2\,\text{k}\Omega$, $i_G \approx 0$, $I_{DSSO} = 5\,\text{mA}$, and $V_{p0} = 5\,\text{V}$ (and is temperature-independent). (*a*) Find the exact value of I_{DQ} at 100°C. (*b*) Use sensitivity analysis to predict I_{DQ} at 100°C.
Ans. (*a*) $I_{DQ} = 1.82\,\text{mA}$; (*b*) $I_{DQ} = 1.84\,\text{mA}$

5.48 Solve parts *a* and *b* of Problem 5.25 if $R_S = 2\,\text{k}\Omega$, $V_{GG} = 1\,\text{V}$, and all else remains unchanged.
Ans. (*a*) The transfer bias line is drawn on Fig. 5-14: $I_{DQ\,\text{max}} \approx 2\,\text{mA}$, $I_{DQ\,\text{min}} \approx 1.1\,\text{mA}$; (*b*) $V_{DSQ\,\text{max}} \approx 6\,\text{V}$, $V_{DSQ\,\text{min}} \approx 10.05\,\text{V}$

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CHAPTER 6

Small-Signal Midfrequency BJT Amplifiers

6.1. INTRODUCTION

For sufficiently small emitter-collector voltage and current excursions about the quiescent point (*small signals*), the BJT is considered linear; it may then be replaced with any of several two-port networks of impedances and controlled sources (called *small-signal equivalent-circuit models*), to which standard network analysis methods are applicable. Moreover, there is a range of signal frequencies which are large enough so that coupling or bypass capacitors (see Section 3.7) can be considered short circuits, yet low enough so that inherent capacitive reactances associated with BJTs can be considered open circuits. In this chapter, all BJT voltage and current signals are assumed to be in this *midfrequency range*.

In practice, the design of small-signal amplifiers is divided into two parts: (1) setting the dc bias or Q point (Chapters 3 and 5), and (2) determining voltage- or current-gain ratios and impedance values at signal frequencies.

6.2. HYBRID-PARAMETER MODELS

General hybrid-parameter analysis of two-port networks was introduced in Section 1.7. Actually, different sets of h parameters are defined, depending on which element of the transistor (E, B, or C) shares a common point with the amplifier input and output terminals.

Common-Emitter Transistor Connection

From Fig. 3-3(b) and (c), we see that if i_C and v_{BE} are taken as dependent variables in the CE transistor configuration, then

$$v_{BE} = f_1(i_B, v_{CE}) \tag{6.1}$$

$$i_C = f_2(i_B, v_{CE}) \tag{6.2}$$

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If the total emitter-to-base voltage v_{BE} goes through only *small* excursions (ac signals) about the Q point, then $\Delta v_{BE} = v_{be}$, $\Delta i_C = i_c$, and so on. Therefore, after applying the chain rule to (*6.1*) and (*6.2*), we have, respectively,

$$v_{be} = \Delta v_{BE} \approx dv_{BE} = \left.\frac{\partial v_{BE}}{\partial i_B}\right|_Q i_b + \left.\frac{\partial v_{BE}}{\partial v_{CE}}\right|_Q v_{ce} \tag{6.3}$$

$$i_c = \Delta i_C \approx di_C = \left.\frac{\partial i_C}{\partial i_B}\right|_Q i_b + \left.\frac{\partial i_C}{\partial v_{CE}}\right|_Q v_{ce} \tag{6.4}$$

The four partial derivatives, evaluated at the Q point, that occur in (*6.3*) and (*6.4*) are called *CE hybrid parameters* and are denoted as follows:

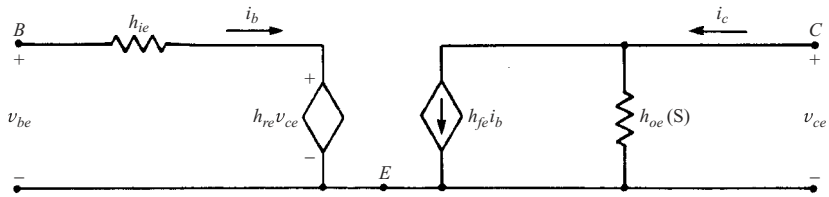
$$\textit{Input resistance} \qquad h_{ie} \equiv \left.\frac{\partial v_{BE}}{\partial i_B}\right|_Q \approx \left.\frac{\Delta v_{BE}}{\Delta i_B}\right|_Q \tag{6.5}$$

$$\textit{Reverse voltage ratio} \qquad h_{re} \equiv \left.\frac{\partial v_{BE}}{\partial v_{CE}}\right|_Q \approx \left.\frac{\Delta v_{BE}}{\Delta v_{CE}}\right|_Q \tag{6.6}$$

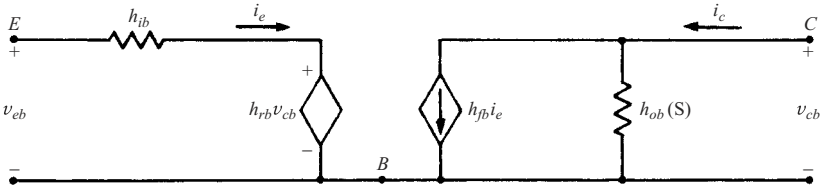
$$\textit{Forward current gain} \qquad h_{fe} \equiv \left.\frac{\partial i_C}{\partial i_B}\right|_Q \approx \left.\frac{\Delta i_C}{\Delta i_B}\right|_Q \tag{6.7}$$

$$\textit{Output admittance} \qquad h_{oe} \equiv \left.\frac{\partial i_C}{\partial v_{CE}}\right|_Q \approx \left.\frac{\partial \Delta i_C}{\Delta v_{CE}}\right|_Q \tag{6.8}$$

The equivalent circuit for (*6.3*) and (*6.4*) is shown in Fig. 6-1(*a*). The circuit is valid for use with signals whose excursion about the Q point is sufficiently small so that the h parameters may be treated as constants.



(*a*) CE small-signal equivalent circuit



(*b*) CB small-signal equivalent circuit

Fig. 6-1

Common-Base Transistor Connection

If v_{EB} and i_C are taken as the dependent variables for the CB transistor characteristics of Fig. 3-2(*b*) and (*c*), then, as in the CE case, equations can be found specifically for small excursions about the Q point. The results are

$$v_{eb} = h_{ib}i_e + h_{rb}v_{cb} \tag{6.9}$$

$$i_c = h_{fb}i_e + h_{ob}v_{cb} \tag{6.10}$$

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The partial-derivative definitions of the CB h-parameters are:

$$\textit{Input resistance} \qquad h_{ib} \equiv \left.\frac{\partial v_{EB}}{\partial i_E}\right|_Q \approx \left.\frac{\Delta v_{EB}}{\Delta i_E}\right|_Q \tag{6.11}$$

$$\textit{Reverse voltage ratio} \qquad h_{rb} \equiv \left.\frac{\partial v_{EB}}{\partial v_{CB}}\right|_Q \approx \left.\frac{\Delta v_{EB}}{\Delta v_{CB}}\right|_Q \tag{6.12}$$

$$\textit{Forward current gain} \qquad h_{fb} \equiv \left.\frac{\partial i_C}{\partial i_E}\right|_Q \approx \left.\frac{\Delta i_C}{\Delta i_E}\right|_Q \tag{6.13}$$

$$\textit{Output admittance} \qquad h_{ob} \equiv \left.\frac{\partial i_C}{\partial v_{CB}}\right|_Q \approx \left.\frac{\Delta i_C}{\Delta v_{CB}}\right|_Q \tag{6.14}$$

A small-signal, h-parameter equivalent circuit satisfying (6.9) and (6.10) is shown in Fig. 6-1(b)

Common-Collector Amplifier

The *common-collector* (CC) or *emitter-follower* (EF) amplifier, with the universal bias circuitry of Fig. 6-2(a), can be modeled for small-signal ac analysis by replacing the CE-connected transistor with its h-parameter model, Fig. 6-1(a). Assuming, for simplicity, that $h_{re} = h_{oe} = 0$, we obtain the equivalent circuit of Fig. 6-2(b).

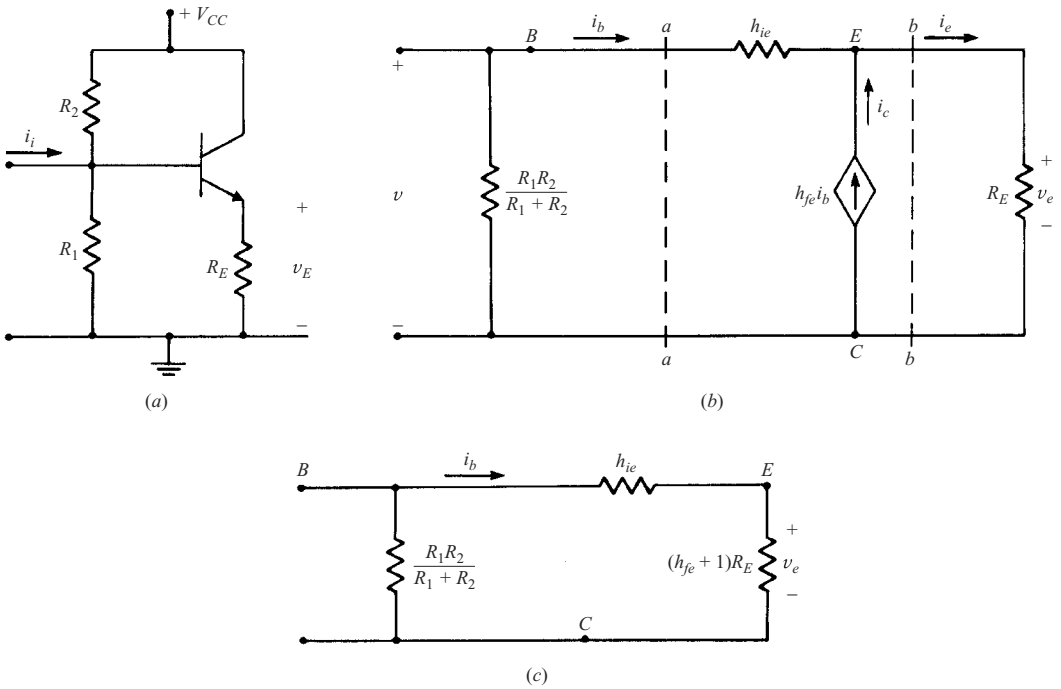


Fig. 6-2 CC amplifier

An even simpler model can be obtained by finding a Thévenin equivalent for the circuit to the right of a, a in Fig. 6-2(b). Application of KVL around the outer loop gives

$$v = i_b h_{ie} + i_e R_E + i_b h_{ie} + (h_{fe} + 1) i_b R_E \tag{6.15}$$

The Thévenin impedance is the driving-point impedance:

$$R_{Th} = \frac{v}{i_b} = h_{ie} + (h_{fe} + 1) R_E \tag{6.16}$$

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The Thévenin voltage is zero (computed with terminals a, a open); thus, the equivalent circuit consists only of R_{Th}. This is shown, in a base-current frame of reference, in Fig. 6-2(c). (See Problem 6.13 for a development of the CC h-parameter model.)

6.3. TEE-EQUIVALENT CIRCUIT

The *tee-equivalent circuit* or *r-parameter model* is a circuit realization based on the z parameters of Chapter 1. Applying the z-parameter definitions of (*1.10*) to (*1.13*) to the CB small-signal equivalent circuit of Fig. 6-1(b) leads to

$$z_{11} = h_{ib} - \frac{h_{rb}h_{fb}}{h_{ob}} \tag{6.17}$$

$$z_{12} = \frac{h_{rb}}{h_{ob}} \tag{6.18}$$

$$z_{21} = -\frac{h_{fb}}{h_{ob}} \tag{6.19}$$

$$z_{22} = \frac{1}{h_{ob}} \tag{6.20}$$

(See Problem 6.17.) Substitution of these z parameters into (*1.8*) and (*1.9*) yields

$$v_{eb} = \left(h_{ib} - \frac{h_{rb}h_{fb}}{h_{ob}}\right) i_e + \frac{h_{rb}}{h_{ob}} (-i_c) \tag{6.21}$$

$$v_{cb} = -\frac{h_{fb}}{h_{ob}} i_e + \frac{1}{h_{ob}} (-i_c) \tag{6.22}$$

If we now define

$$r_b = \frac{h_{rb}}{h_{ob}} \tag{6.23}$$

$$r_e = h_{ib} - \frac{h_{rb}}{h_{ob}} (1 + h_{fb}) \tag{6.24}$$

$$r_c = \frac{1 - h_{rb}}{h_{ob}} \tag{6.25}$$

$$\alpha' = -\frac{h_{fb} + h_{rb}}{1 - h_{rb}} \tag{6.26}$$

then (*6.21*) and (*6.22*) can be written

$$v_{eb} = (r_e + r_b)i_e - r_b i_c \tag{6.27}$$

and

$$v_{cb} = (\alpha' r_c + r_b)i_e - (r_b + r_c)i_c \tag{6.28}$$

Typically, $-0.9 > h_{fb} > -1$ and $0 \leq h_{rb} \ll 1$. Letting $h_{rb} \approx 0$ in (*6.26*), comparing (*6.13*) with (*3.1*) while neglecting thermally generated leakage currents, and assuming that $h_{FB} = h_{fb}$ (which is a valid assumption *except* near the boundary of active-region operation) result in

$$\alpha' \approx -h_{fb} = \alpha \tag{6.29}$$

Then the tee-equivalent circuit or r-parameter model for CB operation is that shown in Fig. 6-3. (See Problems 6.3 and 6.5 for r-parameter models for the CE and CC configurations, respectively.)

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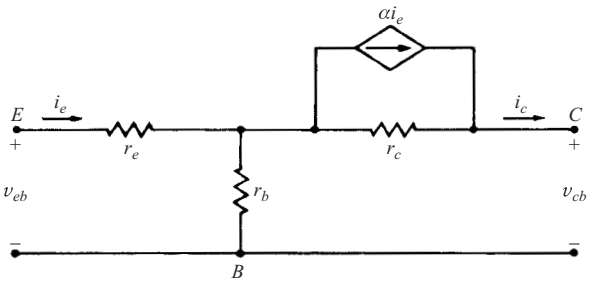


Fig. 6-3

6.4. CONVERSION OF PARAMETERS

Transistor manufacturers typically specify h_{FE} ($\approx h_{fe}$) and a set of input characteristics and collector characteristics for either CE or CB connection. Thus the necessity arises for conversion of h parameters among the CE, CB, and CC configurations or for calculation of r parameters from h parameters. Formulas can be developed to allow ready conversion from a known parameter set to a desired parameter set.

Example 6.1. Apply KVL and KCL to Fig. 6-1(a) to obtain $v_{eb} = g_1(i_e, v_{cb})$ and $i_c = g_2(i_e, v_{eb})$. Compare these equations with (*6.9*) and (*6.10*) to find the CB h parameters in terms of the CE h parameters. Use the typically reasonable approximations $h_{re} \ll 1$ and $h_{fe} + 1 \gg h_{ie}h_{oe}$ to simplify the computations and results.

KVL around the E, B loop of Fig. 6-1(a) (with assumed current directions reversed) yields

$$v_{eb} = -h_{ie}i_b - h_{re}v_{ce} \tag{6.30}$$

But KCL at node E requires that

$$i_b = -i_e - i_c = -i_e - h_{fe}i_b - h_{oe}v_{ce}$$

or

$$-i_b = \frac{1}{h_{fe}+1}\, i_e + \frac{h_{oe}}{h_{fe}+1}\, v_{ce} \tag{6.31}$$

In addition, KVL requires that

$$v_{ce} = v_{cb} - v_{eb} \tag{6.32}$$

Substituting (*6.31*) and (*6.32*) into (*6.30*) and rearranging give

$$\frac{(1-h_{re})(h_{fe}+1)+h_{ie}h_{oe}}{h_{fe}+1}\, v_{eb} = \frac{h_{ie}}{h_{fe}+1}\, i_e + \left(\frac{h_{ie}h_{oe}}{h_{fe}+1} - h_{re}\right) v_{cb} \tag{6.33}$$

Use of the given approximations reduces the coefficient of v_{eb} in (*6.33*) to unity, so that

$$v_{eb} \approx \frac{h_{ie}}{h_{fe}+1}\, i_e + \left(\frac{h_{ie}h_{oe}}{h_{fe}+1} - h_{re}\right) v_{cb} \tag{6.34}$$

Now KCL at node C of Fig. 6-1(a) (again with assumed current directions reversed) yields

$$i_c = h_{fe}i_b + h_{oe}v_{ce} \tag{6.35}$$

Substituting (*6.31*), (*6.32*), and (*6.34*) into (*6.35*) and solving for i_c give

$$i_c = -\left[\frac{h_{fe}}{h_{fe}+1} + \frac{h_{oe}h_{ie}}{(h_{fe}+1)^2}\right] i_e - h_{oe}\left[\frac{h_{ie}h_{oe}}{(h_{fe}+1)^2} - \frac{h_{re}+1}{h_{fe}+1}\right] v_{cb} \tag{6.36}$$

Use of the given approximations then leads to

$$i_c \approx -\frac{h_{fe}}{h_{fe}+1}\, i_e + \frac{h_{oe}}{h_{fe}+1}\, v_{cb} \tag{6.37}$$

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Comparing (*6.34*) with (*6.9*) and (*6.37*) with (*6.10*), we see that

$$h_{ib} = \frac{h_{ie}}{h_{fe} + 1} \tag{6.38}$$

$$h_{rb} = \frac{h_{ie}h_{oe}}{h_{fe} + 1} - h_{re} \tag{6.39}$$

$$h_{fb} = -\frac{h_{fe}}{h_{fe} + 1} \tag{6.40}$$

$$h_{ob} = \frac{h_{oe}}{h_{fe} + 1} \tag{6.41}$$

6.5. MEASURES OF AMPLIFIER GOODNESS

Amplifiers are usually designed to emphasize one or more of the following interrelated performance characteristics, whose quantitative measures of goodness are defined in terms of the quantities of Fig. 6-4:

1. *Current amplification*, measured by the current-gain ratio $A_i = i_o/i_{\text{in}}$.
2. *Voltage amplification*, measured by the voltage-gain ratio $A_v = v_o/v_{\text{in}}$.
3. *Power amplification*, measured by the ratio $A_p = A_v A_i = v_o i_o / i_o i_{\text{in}}$.
4. *Phase shift of signals*, measured by the phase angle of the frequency-domain ratio $A_v(j\omega)$ or $A_i(j\omega)$.
5. *Impedance match or change*, measured by the input impedance Z_{in} (the driving-point impedance looking into the input port).
6. *Power transfer ability*, measured by the output impedance Z_o (the driving-point impedance looking into the output port with the load removed). If $Z_o = Z_L$, the maximum power transfer occurs.

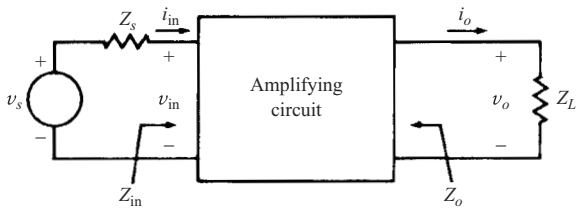


Fig. 6-4

6.6. CE AMPLIFIER ANALYSIS

A simplified (bias network omitted) CE amplifier is shown in Fig. 6-5(*a*), and the associated small-signal equivalent circuit in Fig. 6-5(*b*).

Example 6.2. In the CE amplifier of Fig. 6-5(*b*), let $h_{ie} = 1\,\text{k}\Omega$, $h_{re} = 10^{-4}$, $h_{fe} = 100$, $h_{oe} = 12\,\mu\text{S}$, and $R_L = 2\,\text{k}\Omega$. (These are typical CE amplifier values.) Find expressions for the (*a*) current-gain ratio A_i, (*b*) voltage-gain ratio A_v, (*c*) input impedance Z_{in}, and (*d*) output impedance Z_o. (*e*) Evaluate this typical CE amplifier.

(*a*) By current division at node C,

$$i_L = \frac{1/h_{oe}}{1/h_{oe} + R_L}(-h_{fe} i_b) \tag{6.42}$$

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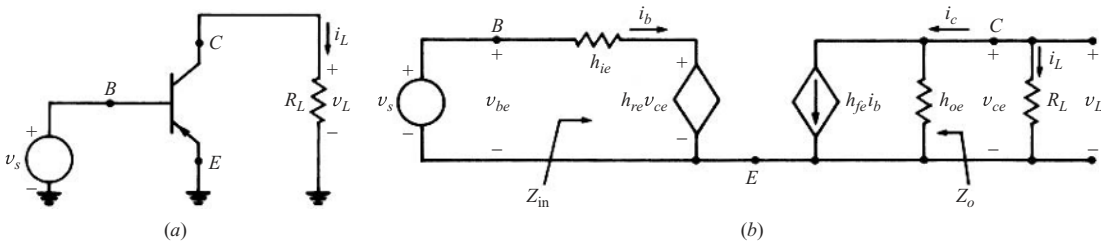


Fig. 6-5

and
$$A_i = \frac{i_L}{i_b} = -\frac{h_{fe}}{1 + h_{oe}R_L} = -\frac{100}{1 + (12 \times 10^{-6})(2 \times 10^3)} = -97.7 \tag{6.43}$$

Note that $A_i \approx -h_{fe}$, where the minus sign indicates a 180° phase shift between input and output currents.

(*b*) By KVL around B, E mesh,

$$v_s = v_{be} = h_{ie}i_b + h_{re}v_{ce} \tag{6.44}$$

Ohm's law applied to the output network requires that

$$v_{ce} = -h_{fe}i_b\left(\frac{1}{h_{oe}} \| R_L\right) = \frac{-h_{fe}R_L i_b}{1 + h_{oe}R_L} \tag{6.45}$$

Solving (*6.45*) for i_b, substituting the result into (*6.44*), and rearranging yield

$$\begin{aligned} A_v = \frac{v_s}{v_{ce}} &= -\frac{h_{fe}R_L}{h_{ie} + R_L(h_{ie}h_{oe} - h_{fe}h_{re})} \\ &= -\frac{(100)(2 \times 10^3)}{1 \times 10^3 + (2 \times 10^3)[(1 \times 10^3)(12 \times 10^{-6}) - (100)(1 \times 10^{-4})]} = -199.2 \end{aligned} \tag{6.46}$$

Observe that $A_v \approx -h_{fe}R_L/h_{ie}$, where the minus sign indicates a 180° phase shift between input and output voltages.

(*c*) Substituting (*6.45*) into (*6.44*) and rearranging yield

$$Z_{\text{in}} = \frac{v_s}{i_b} = h_{ie} - \frac{h_{re}h_{fe}R_L}{1 + h_{oe}R_L} = 1 \times 10^3 - \frac{(1 \times 10^{-4})(100)(2 \times 10^3)}{1 + (12 \times 10^{-6})(2 \times 10^3)} = 980.5\,\Omega \tag{6.47}$$

Note that for typical CE amplifier values, $Z_{\text{in}} \approx h_{ie}$.

(*d*) We deactivate (short) v_s and replace R_L with a driving-point source so that $v_{dp} = v_{ce}$. Then, for the input mesh, Ohm's law requires that

$$i_b = -\frac{h_{re}}{h_{ie}}v_{dp} \tag{6.48}$$

However, at node C (with, now, $i_c = i_{dp}$), KCL yields

$$i_c = i_{dp} = h_{fe}i_b + h_{oe}v_{dp} \tag{6.49}$$

Using (*6.48*) in (*6.49*) and rearranging then yield

$$Z_o = \frac{v_{dp}}{i_{dp}} = \frac{1}{h_{oe} - h_{fe}h_{re}/h_{ie}} = \frac{1}{12 \times 10^{-6} - (100)(1 \times 10^{-4})/(1 \times 10^3)} = 500\,\text{k}\Omega \tag{6.50}$$

The output impedance is increased by feedback due to the presence of the controlled source $h_{re}v_{ce}$.

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(*e*) Based on the typical values of this example, the characteristics of the CE amplifier can be summarized as follows:

1. Large current gain
2. Large voltage gain
3. Large power gain ($A_i A_v$)
4. Current and voltage phase shifts of 180°
5. Moderate input impedance
6. Moderate output impedance

6.7. CB AMPLIFIER ANALYSIS

A simplified (bias network omitted) CB amplifier is shown in Fig. 6-6(*a*), and the associated small-signal equivalent circuit in Fig. 6-6(*b*).

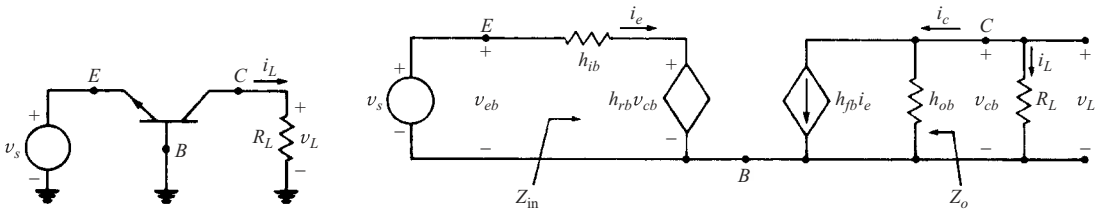


Fig. 6-6 CB amplifier

Example 6.3. In the CB amplifier of Fig. 6-6(*b*), let $h_{ib} = 30\,\Omega$, $h_{rb} = 4 \times 10^{-6}$, $h_{fb} = -0.99$, $h_{ob} = 8 \times 10^{-7}$ S, and $R_L = 20\,\text{k}\Omega$. (These are typical CB amplifier values.) Find expressions for the (*a*) current-gain ratio A_i, (*b*) voltage-gain ratio A_v, (*c*) input impedance Z_{in}, and (*d*) output impedance Z_o. (*e*) Evaluate this typical CE amplifier.

(*a*) By direct analogy with Fig. 6-5(*b*) and (*6.43*)

$$A_i = -\frac{h_{fb}}{1 + h_{ob}R_L} = -\frac{-0.99}{1 + (8 \times 10^{-7})(20 \times 10^3)} = 0.974 \tag{6.51}$$

Note that $A_i \approx -h_{fb} < 1$, and that the input and output currents are in phase because $h_{fb} < 0$.

(*b*) By direct analogy with Fig. 6-5(*b*) and (*6.46*),

$$A_v = -\frac{h_{fb}R_L}{h_{ib} + R_L(h_{ib}h_{oc} - h_{fb}h_{rb})} = -\frac{(-0.99)(20 \times 10^3)}{30 + (20 \times 10^3)[(30)(8 \times 10^{-7}) - (-0.99)(4 \times 10^{-6})]} = 647.9 \tag{6.52}$$

Observe that $A_v \approx -h_{fb}R_L/h_{ib}$, and the output and input voltages are in phase because $h_{fb} < 0$.

(*c*) By direct analogy with Fig. 6-5(*b*) and (*6.47*)

$$Z_{\text{in}} = h_{ib} - \frac{h_{rb}h_{fb}R_L}{1 + h_{ob}R_L} = 30 - \frac{(4 \times 10^{-6})(-0.99)(20 \times 10^3)}{1 + (8 \times 10^{-7})(20 \times 10^3)} = 30.08\,\Omega \tag{6.53}$$

It is apparent that $Z_{\text{in}} \approx h_{ib}$.

(*d*) By analogy with Fig. 6-5(*b*) and (*6.50*),

$$Z_o = \frac{1}{h_{ob} - h_{fb}h_{rb}/h_{ib}} = \frac{1}{8 \times 10^{-7} - (-0.99)(4 \times 10^{-6})/30} = 1.07\,\text{M}\Omega \tag{6.54}$$

Note that Z_o is decreased because of the feedback from the output mesh to the input mesh through $h_{rb}v_{cb}$.

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(*e*) Based on the typical values of this example, the characteristics of the CB amplifier can be summarized as follows:

1. Current gain of less than 1
2. High voltage gain
3. Power gain approximately equal to voltage gain
4. No phase shift for current or voltage
5. Small input impedance
6. Large output impedance

6.8. CC AMPLIFIER ANALYSIS

Figure 6-7(*a*) shows a CC amplifier with the bias network omitted. The small-signal equivalent circuit is drawn in Fig. 6-7(*b*).

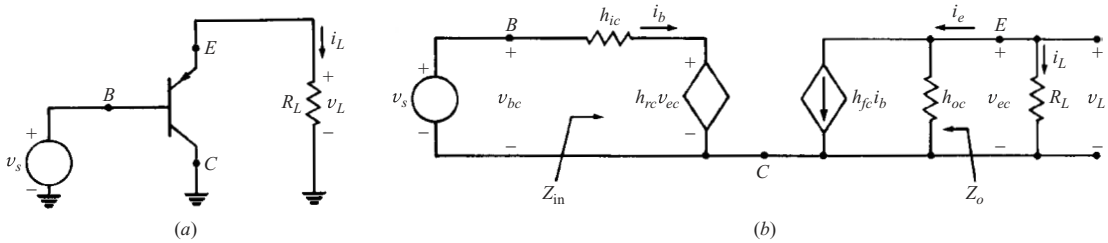


Fig. 6-7 CC amplifier

Example 6.4. In the CC amplifier of Fig. 6-7(*b*), let $h_{ic} = 1\,\text{k}\Omega$, $h_{rc} = 1$, $h_{fc} = -101$, $h_{oc} = 12\,\mu\text{S}$, and $R_L = 2\,\text{k}\Omega$. Drawing direct analogies with the CE amplifier of Example 6.2, find expressions for the (*a*) current-gain ratio A_i, (*b*) voltage-gain ratio A_v, (*c*) input impedance Z_{in}, and (*d*) output impedance Z_o. (*e*) Evaluate this typical CC amplifier.

(*a*) In parallel with (*6.43*),

$$A_i = \frac{h_{fc}}{1 + h_{oc}R_L} = -\frac{-101}{1 + (12 \times 10^{-6})(2 \times 10^3)} = 98.6 \tag{6.55}$$

Note that $A_i \approx -h_{fc}$, and that the input and output currents are in phase because $h_{fc} < 0$.

(*b*) In parallel with (*6.46*),

$$A_v = -\frac{h_{fc}R_L}{h_{ic} + R_L(h_{ic}h_{oc} - h_{fc}h_{rc})} = -\frac{(-101)(2 \times 10^3)}{1 \times 10^3 + (2 \times 10^3)[(1 \times 10^3)(12 \times 10^{-6}) - (-101)(1)]} = 0.995 \tag{6.56}$$

Observe that $A_v \approx 1/(1 - h_{ic}h_{oc}/h_{fc}) \approx 1$. Since the gain is approximately 1 and the output voltage is in phase with the input voltage, this amplifier is commonly called a *unity follower*.

(*c*) In parallel with (*6.47*),

$$Z_{\text{in}} = h_{ic} - \frac{h_{rc}h_{fc}R_L}{1 + h_{oc}R_L} = 1 \times 10^3 - \frac{(1)(-101)(2 \times 10^3)}{1 + (12 \times 10^{-6})(2 \times 10^3)} = 8.41\,\text{M}\Omega \tag{6.57}$$

Note that $Z_{\text{in}} \approx -h_{fc}/h_{oc}$.

(*d*) In parallel with (*6.50*),

$$Z_o = \frac{1}{h_{oc} - h_{fc}h_{rc}/h_{ic}} = \frac{1}{12 \times 10^{-6} - (-101)(1)/(1 \times 10^3)} = 9.9\,\Omega$$

Note that $Z_o \approx -h_{ic}/h_{fc}$.

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(*e*) Based on the typical values of this example, the characteristics of the CB amplifier can be summarized as follows:

1. High current gain
2. Voltage gain of approximately unity
3. Power gain approximately equal to current gain
4. No current or voltage phase shift
5. Large input impedance
6. Small output impedance

6.9. BJT AMPLIFIER ANALYSIS WITH SPICE

Since SPICE models of the BJT (see Chapter 3) provide the device terminal characteristics, a transistor amplifier can be properly biased and a time-varying input signal can be directly applied to the completely modeled amplifier circuit. Any desired signal that results can be measured directly in the time domain to form signal ratios that yield current and voltage gains. With such modeling, any signal distortion that results from nonlinear operation of the BJT is readily apparent from inspection of signal-time plots. Such an analysis approach is the analytical equivalent of laboratory operation of the amplifier where the time plot of signals is analogous to oscilloscope observation of the amplifier circuit signals.

SPICE capabilities also lend themselves to BJT amplifier analysis using the small-signal equivalent circuits. In such case, the voltage-controlled voltage source (VCVS) and the current-controlled current source (CCCS) introduced in Section 1.3 find obvious application in the small-signal equivalent circuits of the type shown in Fig. 6-1. Either time-varying analysis (.TRAN command statement) or sinusoidal steady-state analysis (.AC command statement) can be performed on the small-signal equivalent circuit.

Example 6.5. For the amplifier of Fig. 3-10(*a*), let $v_i = 0.25\sin(2000\pi t)$ V, $V_{CC} = 15$ V, $CC_1 = CC_2 = CC = 100\,\mu$F, $R_1 = 6\,\text{k}\Omega$, $R_2 = 50\,\text{k}\Omega$, $R_C = R_L = 1\,\text{k}\Omega$, and $R_i = R_E = 100\,\Omega$. The transistor is characterized by the model of Problem 5.4. Use SPICE methods to determine the CE hybrid parameters of (6.5) through (6.8) for this transistor at the point of operation.

The netlist code below describes the circuit.

```
EX6_5.CIR
vi  1 0 SIN(0V 250mV 10kHz)
Ri  1 2 100ohm
CC1 2 3 1000uF
CC2 4 7 1000uF
R1  3 0 6kohm
R2  3 6 50kohm
RC  6 4 1kohm
RE  5 0 100ohm
RL  7 0 1kohm
VCC 6 0 15V
Q 4  3 5 QNPNG
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=75V Cjc=10pF Cje=15pF)
.TRAN 1us 0.1ms
.PROBE
.END
```

After executing ⟨Ex6_5.CIR⟩, the plots of Fig. 6-8 can be generated by use of the Probe feature of PSpice. The resulting *h*-parameter value is indicated on each of the four plots of Fig. 6-8.

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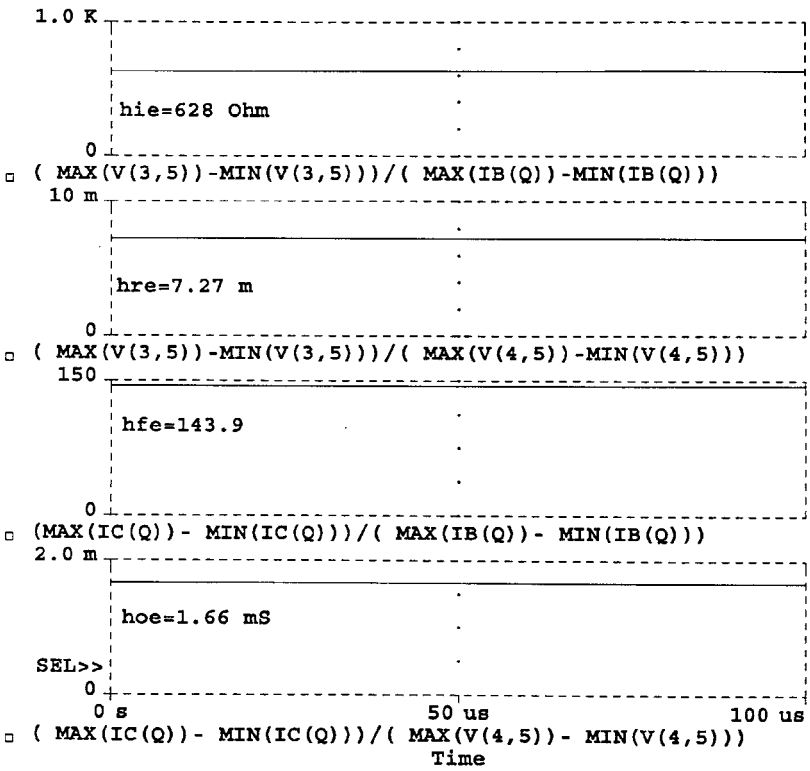


Fig. 6-8

Example 6.6. For the amplifier of Example 6.5, use SPICE methods to determine (*a*) the input impedance Z_{in}, (*b*) the current gain A_i, and (*c*) the voltage gain A_v.

Netlist code that describes the amplifier circuit follows:

```
Ex6_6.CIR
vi  1 0 AC 1V
Ri  1 2 100ohm
CC1 2 3 1000uF
CC2 4 7 1000uF
R1  3 0 6kohm
R2  3 6 50kohm
RC  6 4 1kohm
RE  5 0 100ohm
RL  7 0 1kohm
VCC 6 0 15V
Q 4  3 5 QNPNG
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=75V Cjc=10pF Cje=15pF)
.AC LIN 1 100Hz 100Hz
.PRINT AC Vm(1)  Vp(1)  Vm(7)  Vp(7)
.PRINT AC Im(Ri) Ip(Ri) Im(RL) IP(RL)
.END
```

(*a*) Execute ⟨Ex6_6.CIR⟩ and poll the output file to find the values of input voltage and current. Thus,

$$Z_{in} = \frac{V(1)}{I(vi)} = \frac{1}{2.465 \times 10^{-4}} = 4.056\,k\Omega$$

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(*b*) The output file contains the magnitudes and phase angles of the input and output voltages. Hence,

$$A_v = -\frac{\text{Vm}(7)}{\text{Vm}(1)} = -\frac{4.649}{1} = -4.649$$

The negative sign accounts for the 180° phase shift [see Vp(7)] of V(7) with respect to V(1).

(*c*) The output file values of Ip(Ri) and Ip(RL) show the two signals to be 180° out of phase. The current gain is found as

$$A_i = -\frac{\text{Im}(\text{RL})}{\text{Im}(\text{Ri})} = -\frac{4.649 \times 10^{-3}}{2.465 \times 10^{-4}} = -18.86$$

Solved Problems

6.1 For the CB amplifier of Fig. 3-23, find the voltage-gain ratio $A_v = v_L/v_S$ using the tee-equivalent small-signal circuit of Fig. 6-3.

The small-signal circuit for the amplifier is given by Fig. 6-9. By Ohm's law,

$$i_c = \frac{v_{cb}}{R_C \| R_L} = \frac{(R_C + R_L)\, v_L}{R_C R_L} \tag{1}$$

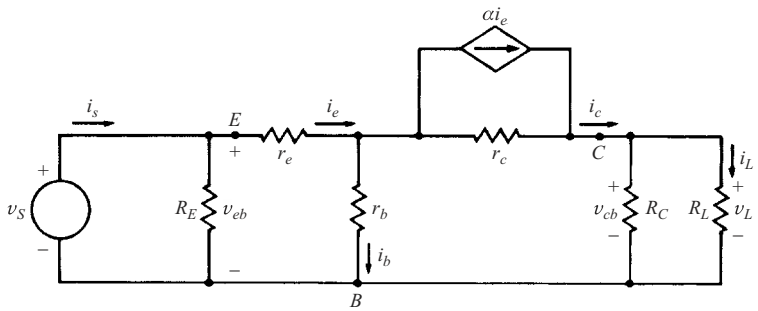


Fig. 6-9

Substituting (*1*) into (*6.27*) and (*6.28*) gives, respectively,

$$v_S = v_{eb} = (r_e + r_b) i_e - r_b \frac{(R_C + R_L) v_L}{R_C R_L} \tag{2}$$

$$v_L = v_{cb} = (\alpha r_c + r_b) i_e - (r_b + r_c) \frac{(R_C + R_L) v_L}{R_C R_L} \tag{3}$$

where we also made use of (*6.29*). Solving (*2*) for i_e and substituting the result into (*3*) yield

$$v_L = (\alpha r_c + r_b) \frac{v_S + \dfrac{r_b (R_C + R_L)}{R_C + R_L} v_L}{r_e + r_b} - (r_b + r_c) \frac{R_C + R_L}{R_C R_L} v_L \tag{4}$$

The voltage-gain ratio follows directly from (*4*) as

$$A_v = \frac{v_L}{v_S} = \frac{(\alpha r_c + r_b) R_C R_L}{R_C R_L (r_e + r_b) + (R_C + R_L)[(1 - \alpha) r_c r_b + r_e (r_b + r_c)]}$$

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6.2 Assume that r_c is large enough so that $i_c \approx \alpha i_e$ for the CB amplifier of Fig. 3-23, whose small-signal circuit is given by Fig. 6-9. Find an expression for the current-gain ratio $A_i = i_L/i_s$ and evaluate it if $r_e = 30\,\Omega$, $r_b = 300\,\Omega$, $r_c = 1\,\text{M}\Omega$, $R_E = 5\,\text{k}\Omega$, $R_C = R_L = 4\,\text{k}\Omega$, and $\alpha = 0.99$.

Letting $i_c \approx \alpha i_e$ in (*6.27*) allows us to determine the input resistance R_{in}:

$$v_{eb} = (r_e + r_b)i_e - r_b(\alpha i_e)$$

from which

$$R_{\text{in}} = \frac{v_{eb}}{i_e} = r_e + (1-\alpha)r_b$$

By current division at node E,

$$i_e = \frac{R_E}{R_E + R_{\text{in}}}\, i_s$$

Solving for i_s gives

$$i_s = \frac{R_E + R_{\text{in}}}{R_E}\, i_e = \frac{R_E + r_e + (1-\alpha)r_b}{R_E}\, i_e \tag{1}$$

Current division at node C, again with $i_c \approx \alpha i_e$, yields

$$i_L = \frac{R_C}{R_C + R_L}\, i_c = \frac{R_C \alpha i_e}{R_C + R_L} \tag{2}$$

The current gain is now the ratio of (*2*) to (*1*):

$$A_i = \frac{i_L}{i_s} = \frac{\alpha R_C/(R_C + R_L)}{[R_E + r_e + (1-\alpha)r_b]/R_E} = \frac{\alpha R_C R_E}{(R_C + R_L)[R_E + r_e + (1-\alpha)r_b]}$$

Substituting the given values results in

$$A_i = \frac{(0.99)(4 \times 10^3)(5 \times 10^3)}{(4 \times 10^3 + 4 \times 10^3)[5 \times 10^3 + 30 + (1 - 0.99)(300)]} = 0.492$$

6.3 The transistor of a CE amplifier can be modeled with the tee-equivalent circuit of Fig. 6-3 if the base and emitter terminals are interchanged, as shown by Fig. 6-10(*a*); however, the controlled source is no longer given in terms of a port current—an analytical disadvantage. Show that the circuits of Fig. 6-10(*b*) and (*c*), where the controlled variable of the dependent source is the input current i_b, can be obtained by application of Thévenin's and Norton's theorems to the circuit of Fig. 6-10(*a*).

The Thévenin equivalent for the circuit above terminals 1,2 of Fig. 6-10(*a*) has

$$v_{th} = \alpha r_c ie \qquad Z_{th} = r_c$$

By KCL, $i_e = i_c + i_b$, so that

$$v_{th} = \alpha r_c i_c + \alpha r_c i_b \tag{1}$$

We recognize that if the Thévenin elements are placed in the network, the first term on the right side of (*1*) must be modeled by using a "negative resistance." The second term represents a controlled voltage source. Thus, a modified Thévenin equivalent can be introduced, in which the "negative resistance" is combined with Z_{th} to give

$$v'_{th} = \alpha r_c i_b = r_m i_b \qquad Z'_{th} = (1-\alpha)r_c \tag{2}$$

With the modified Thévenin elements of (*2*) in position, we obtain Fig. 6-10(*b*).

The elements of the Norton equivalent circuit can be determined directly from (*2*) as

$$Z_N = \frac{1}{Y_N} = Z'_{th} = (1-\alpha)r_c \qquad I_N = \frac{v'_{th}}{Z'_{th}} = \frac{\alpha r_c i_b}{(1-\alpha)r_c} = \beta i_b \tag{3}$$

The elements of (*3*) give the circuit of Fig. 6-10(*c*).

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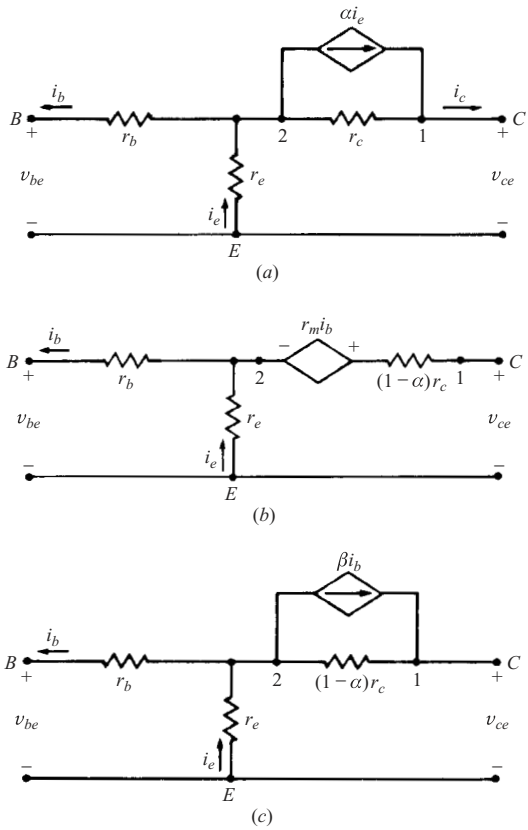


Fig. 6-10

6.4 Utilize the *r*-parameter equivalent circuit of Fig. 6-10(*b*) to find the voltage gain ratio $A_v = v_L/v_i$ for the CE amplifier circuit of Fig. 3-10.

The small-signal equivalent circuit for the amplifier is drawn in Fig. 6-11. After finding the Thévenin equivalent for the network to the left of terminals B, E, we may write

$$v_{be} = \frac{R_B}{R_B + R_i} v_i + \frac{R_B R_i}{R_B + R_i} i_b \tag{1}$$

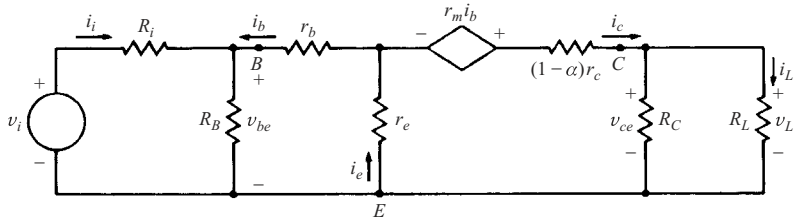


Fig. 6-11

Ohm's law at the output requires that

$$v_{ce} = v_L = \frac{R_C R_L}{R_C + R_L} i_c \tag{2}$$

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Applying KVL around the B, E mesh and around the C, E mesh while noting that $i_e = i_c + i_b$ yields, respectively,

$$v_{be} = -r_b i_b - r_e i_e = -(r_b + r_e) i_b - r_e i_c \tag{3}$$

and

$$v_{ce} = -r_e i_e + r_m i_b - (1-\alpha) r_c i_c = -(r_e - r_m) i_b - [(1-\alpha) r_c + r_e] i_c \tag{4}$$

Equating (*1*) to (*3*) and (*2*) to (*4*) allows formulation of the system of linear equations

$$\begin{bmatrix} -\left(r_b + r_e + \dfrac{R_B R_i}{R_B + R_i}\right) \dfrac{R_B + R_i}{R_B} & -\dfrac{r_e (R_B + R_i)}{R_B} \\ -(r_e - r_m) & -\left[(1-\alpha) r_c + r_e + \dfrac{R_C R_L}{R_C + R_L}\right] \end{bmatrix} \begin{bmatrix} i_b \\ i_c \end{bmatrix} = \begin{bmatrix} v_i \\ 0 \end{bmatrix}$$

from which, by Cramer's rule, $i_c = \Delta_2 / \Delta$, where

$$\Delta = \frac{R_B + R_i}{R_B} \left\{ \left(r_b + r_e + \frac{R_B R_i}{R_B + R_i} \right) \left[(1-\alpha) r_c + r_e + \frac{R_C R_L}{R_C + R_L} \right] - r_e (r_e - r_m) \right\}$$

$$\Delta_2 = (r_e - r_m) v_i$$

Then

$$A_v = \frac{v_L}{v_i} = \frac{(R_L \| R_C) i_c}{v_i} = \frac{R_L R_C}{R_L + R_C} \frac{r_e - r_m}{\Delta}$$

6.5 The CE tee-equivalent circuit of Fig. 6-10(*b*) is suitable for use in the analysis of an EF amplifier if the collector and emitter branches are interchanged. Use this technique to calculate (*a*) the voltage-gain ratio $A_v = v_L / v_B$ and (*b*) the input impedance for the amplifier of Fig. 3-26(*a*).

(*a*) The appropriate small-signal equivalent circuit is given in Fig. 6-12. By KVL around the B, C loop, with $r_m = \alpha r_c$ (from Problem 6.3),

$$v_B = r_b i_b + r_m i_b + (1-\alpha) r_c (i_b - i_e) = (r_b + r_c) i_b - (1-\alpha) r_c i_e \tag{1}$$

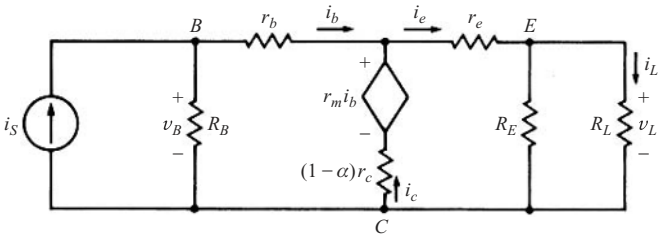


Fig. 6-12

Application of KVL around the C, E loop, again with $r_m = \alpha r_c$, gives

$$0 = r_e i_e - r_m i_b - (1-\alpha) r_c (i_b - i_e) + \frac{R_E R_L}{R_E + R_L} i_e = -r_c i_b + \left[r_e + (1-\alpha) r_c + \frac{R_E R_L}{R_E + R_L} \right] i_e \tag{2}$$

By Cramer's rule applied to the system consisting of (*1*) and (*2*), $i_e = \Delta_2 / \Delta$, where

$$\Delta = r_b \left[r_e + (1-\alpha) r_c + \frac{R_E R_L}{R_E + R_L} \right] + r_c \left(r_e + \frac{R_E R_L}{R_E + R_L} \right)$$

$$\Delta_2 = r_c v_B$$

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Now, by Ohm's law,

$$v_L = (R_E \| R_L) i_e = \frac{R_E R_L}{R_E + R_L} \frac{\Delta_2}{\Delta}$$

Then
$$A_v = \frac{v_L}{v_B} = \frac{R_E R_L r_c/(R_E + R_L)}{r_b[r_e + (1-\alpha)r_c + R_E R_L/(R_E + R_L)] + r_c[r_e + R_E R_L/(R_E + R_L)]}$$

(*b*) The input impedance can be found as $Z_{\text{in}} = R_B \| (v_B/i_b)$. Now, in the system consisting of (*1*) and (*2*), by Cramer's rule, $i_b = \Delta_1/\Delta$, where

$$\Delta_1 = \left[r_e + (1-\alpha)r_c + \frac{R_E R_L}{R_E + R_L} \right] v_B$$

Hence,
$$Z_{\text{in}} = R_B \| \left(\frac{\Delta}{\Delta_1} v_B \right) = \frac{R_B r_b \left[r_e + (1-\alpha)r_c + \dfrac{R_E R_L}{R_E + R_L} \right] + R_B r_c \left(r_e + \dfrac{R_E R_L}{R_E + R_L} \right)}{(R_B + r_b) \left[r_e + (1-\alpha)r_c + \dfrac{R_E R_L}{R_E + R_L} \right] + r_c \left(r_e + \dfrac{R_E R_L}{R_E + R_L} \right)}$$

6.6 Answer the following questions relating to a CE-connected transistor: (*a*) How are the input characteristics (i_B versus v_{BE}) affected if there is negligible feedback of v_{CE}? (*b*) What might be the effect of a too-small emitter-base junction bias? (*c*) Suppose the transistor has an infinite output impedance; how would that affect the output characteristics? (*d*) With reference to Fig. 3-9(*b*), does the current gain of the transistor increase or decrease as the mode of operation approaches saturation from the active region?

(*a*) The family of input characteristics degenerates to a single curve—one that is frequently used to approximate the family.

(*b*) If I_{BQ} were so small that operation occurred near the knee of an input characteristic curve, distortion would result.

(*c*) The slope of the output characteristic curves would be zero in the active region.

(*d*) Δi_C decreases for constant Δi_B; hence, the current gain decreases.

6.7 Use a small-signal *h*-parameter equivalent circuit to analyze the amplifier of Fig. 3-10(*a*), given $R_C = R_L = 800\,\Omega$, $R_i = 0$, $R_1 = 1.2\,\text{k}\Omega$, $R_2 = 2.7\,\text{k}\Omega$, $h_{re} \approx 0$, $h_{oe} = 100\,\mu\text{S}$, $h_{fe} = 90$, and $h_{ie} = 200\,\Omega$. Calculate (*a*) the voltage gain A_v and (*b*) the current gain A_i.

(*a*) The small-signal circuit is shown in Fig. 6-13, where $R_B = R_1 R_2/(R_1 + R_2) = 831\,\Omega$. By current division in the collector circuit,

$$-i_L = \frac{R_C(1/h_{oe})}{R_C(1/h_{oe}) + R_L(1/h_{oe}) + R_L R_C} h_{fe} i_b$$

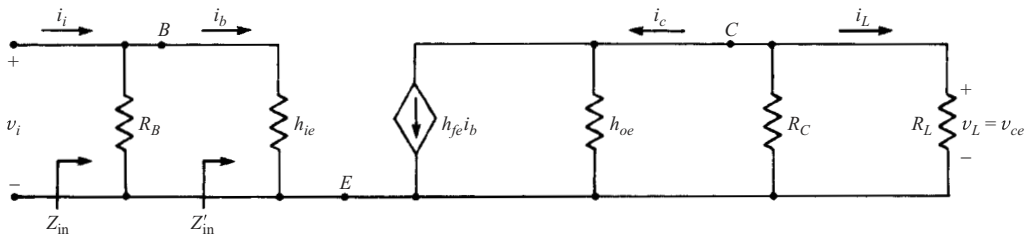


Fig. 6-13

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The voltage gain is then

$$A_v \equiv \frac{v_L}{v_i} = \frac{R_L i_L}{h_{ie} i_b} = -\frac{h_{fe} R_L R_C}{h_{ie}(R_C + R_L + h_{oe} R_L R_C)} = -\frac{(90)(800)^2}{200[1600 + (100 \times 10^{-6})(800)^2]} = -173.08 \qquad (1)$$

(*b*) By current division,

$$i_b = \frac{R_B}{R_B + h_{ie}}\, i_i$$

so

$$A_i \equiv \frac{i_L}{i_i} = \frac{R_B}{R_B + h_{ie}} \frac{i_L}{i_b} = \frac{R_B h_{ie}}{R_L(R_B + h_{ie})}\, A_v = \frac{(831)(200)(-173.08)}{(800)(1031)} = -34.87$$

6.8 For the amplifier of Example 6.5, use SPICE methods to determine the voltage gain $A_v = v_L/v_i$.

Execute the file ⟨Ex6_5.CIR⟩ of Example 6.5, then use the Probe feature of PSpice to generate the instantaneous waveforms of input voltage v_i and output voltage v_L shown by Fig. 6-14. The peak values of v_i and v_L are marked. Hence,

$$A_v = \frac{v_L}{v_i} = -\frac{V_{Lm}}{V_{im}} = -\frac{1.1528}{0.250} = -4.61$$

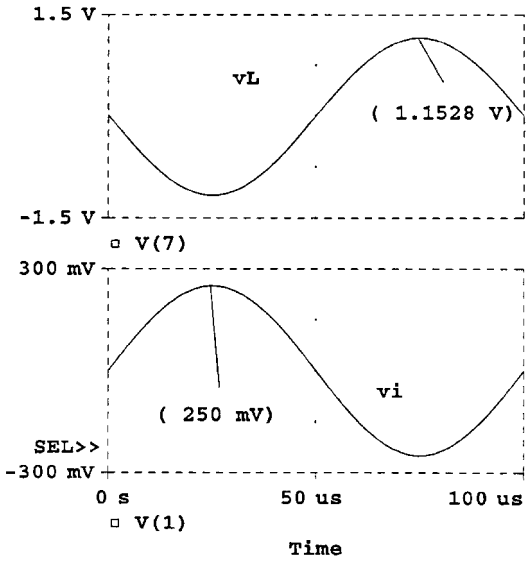


Fig. 6-14

6.9 Suppose the emitter-base junction of a Ge transistor is modeled as a forward-biased diode. Express h_{ie} in terms of the emitter current.

The use of transistor notation in (*2.1*) gives

$$i_B = I_{CBO}(e^{v_{BE}/v_T} - 1) \qquad (1)$$

Then, by (*6.5*),

$$\frac{1}{h_{ie}} = \left.\frac{\partial i_B}{\partial v_{BE}}\right|_Q = \frac{1}{V_T} I_{CBO} e^{v_{BEQ}/v_T} \qquad (2)$$

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But, by (*1*) and Problem 2.1,

$$I_{BQ} = I_{CBO}(e^{v_{BEQ}/v_T} - 1) \approx I_{CBO}e^{v_{BEQ}/v_T} \tag{3}$$

and

$$I_{BQ} = \frac{I_{EQ}}{\beta + 1} \tag{4}$$

Equations (*2*), (*3*), and (*4*) imply

$$h_{ie} = \frac{V_T(\beta + 1)}{I_{EQ}}$$

6.10 For the CB amplifier of Problem 3.12, determine graphically (*a*) h_{fb} and (*b*) h_{ob}.

(*a*) The Q point was established in Problem 3.12 and is indicated in Fig. 3-16. By (*6.13*),

$$h_{fb} \approx \left.\frac{\Delta i_C}{\Delta i_E}\right|_{v_{CBQ}=-6.1\,\text{V}} = \frac{(3.97 - 2.0) \times 10^{-3}}{(4 - 2) \times 10^{-3}} = 0.985$$

(*b*) By (*6.14*),

$$h_{ob} \approx \left.\frac{\Delta i_C}{\Delta v_{CB}}\right|_{I_{EQ}=3\,\text{mA}} = \frac{(3.05 - 2.95) \times 10^{-3}}{-10 - (-2)} = 12.5\,\mu\text{S}$$

6.11 Find the input impedance Z_{in} of the circuit of Fig. 3-10(*a*) in terms of the h parameters, all of which are nonzero.

The small-signal circuit of Fig. 6-13, with $R_B = R_1R_2/(R_1 + R_2)$, is applicable if a dependent source $h_{re}v_{ce}$ is added in series with h_{ie}, as in Fig. 6-1(*a*). The admittance of the collector circuit is given by

$$G = h_{oe} + \frac{1}{R_L} + \frac{1}{R_C}$$

and, by Ohm's law,

$$v_{ce} = \frac{-h_{fe}i_b}{G} \tag{1}$$

By KVL applied to the input circuit,

$$i_b = \frac{v_i - h_{re}v_{ce}}{h_{ie}} \tag{2}$$

Now (*1*) may be substituted in (*2*) to eliminate v_{ce}, and the result rearranged into

$$Z'_{\text{in}} = \frac{v_i}{i_b} = h_{ie} - \frac{h_{re}h_{fe}}{G} \tag{3}$$

Then

$$Z_{\text{in}} = \frac{R_BZ'_{\text{in}}}{R_B + Z'_{\text{in}}} = \frac{R_B(h_{ie} - h_{re}h_{fe}/G)}{R_B + h_{ie} - h_{re}h_{fe}/G} \tag{4}$$

6.12 In terms of the CB h parameters for the amplifier of Fig. 6-15(*a*), find (*a*) the input impedance Z_{in}, (*b*) the voltage gain A_v, and (*c*) the current gain A_i.

(*a*) The h-parameter equivalent circuit is given in Fig. 6-15(*b*). By Ohm's law,

$$v_{cb} = -\frac{h_{fb}i_e}{h_{ob} + 1/R_C + 1/R_L} \equiv -\frac{h_{fb}i_e}{G} \tag{1}$$

Application of KVL at the input gives

$$v_S = h_{rb}v_{cb} + h_{ib}i_e \tag{2}$$

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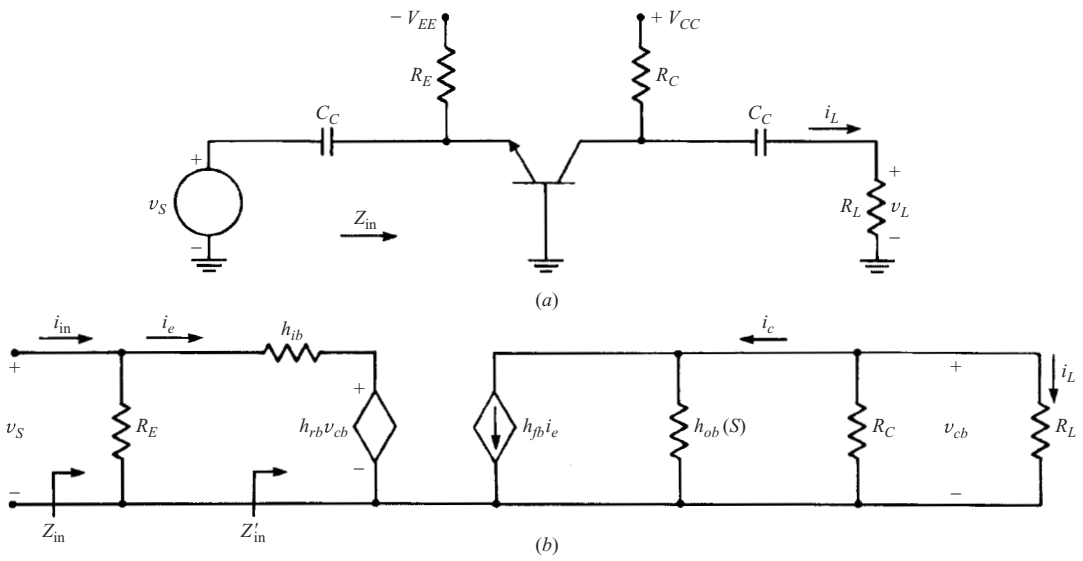


Fig. 6-15

Now (*1*) may be substituted into (*2*) and the result solved for $Z'_{\text{in}} \equiv v_S/i_e$. Finally, Z_{in} may be found as the parallel combination of Z'_{in} and R_E:

$$Z_{\text{in}} = \frac{R_E(h_{ib}G - h_{rb}h_{fb})}{R_E G + h_{ib}G - h_{rb}h_{fb}} \tag{3}$$

(*b*) By elimination of i_e between (*1*) and (*2*) followed by rearrangement,

$$A_v = \frac{v_{cb}}{v_S} = -\frac{h_{fb}}{h_{ib}G - h_{rb}h_{fb}}$$

(*c*) From (*1*),

$$i_L = \frac{v_{cb}}{R_L} = -\frac{h_{fb}i_e}{R_L G} \tag{4}$$

By KCL at the emitter node,

$$i_e = i_{\text{in}} - \frac{v_S}{R_E} = i_{\text{in}} - \frac{i_{\text{in}}Z_{\text{in}}}{R_E} = i_{\text{in}}\left(1 - \frac{Z_{\text{in}}}{R_E}\right) \tag{5}$$

Now elimination of i_e between (*4*) and (*5*) and rearrangement give

$$A_i = \frac{i_L}{i_{\text{in}}} = -\frac{h_{fb}}{R_L G}\left(1 - \frac{Z_{\text{in}}}{R_E}\right)$$

6.13 The CE *h*-parameter transistor model (with $h_{re} = h_{oe} = 0$) was applied to the CC amplifier in Section 6.2. Taking i_B and v_{EC} as independent variables, develop a CC *h*-parameter model which allows for more accurate representation of the transistor than the circuit of Fig. 6-2(*c*).

CC characteristics are not commonly given by transistor manufacturers, but they would be plots of i_B vs. v_{BC} with v_{EC} as parameter (input characteristics) and plots of i_E vs. v_{EC} with i_B as parameter (output or emitter characteristics). With i_B and v_{EC} as independent variables, we have

$$v_{BC} = f_1(i_B, v_{EC}) \tag{1}$$
$$i_E = f_2(i_B, v_{EC}) \tag{2}$$

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Next we apply the chain rule to form the total differentials of (*1*) and (*2*), assuming that $v_{bc} = \Delta v_{BC} \approx dv_{BC}$, and similarly for i_e:

$$v_{bc} = \Delta v_{BC} \approx dv_{BC} = \left.\frac{\partial v_{BC}}{\partial i_B}\right|_Q i_b + \left.\frac{\partial v_{BC}}{\partial v_{EC}}\right|_Q v_{ec} \tag{3}$$

$$i_e = \Delta i_E \approx di_E = \left.\frac{\partial i_E}{\partial i_B}\right|_Q i_b + \left.\frac{\partial i_E}{\partial v_{EC}}\right|_Q v_{ec} \tag{4}$$

Finally, we define

$$\textit{Input resistance} \quad h_{ic} \equiv \left.\frac{\partial v_{BC}}{\partial i_B}\right|_Q \approx \left.\frac{\Delta v_{BC}}{\Delta i_B}\right|_Q \tag{5}$$

$$\textit{Reverse voltage ratio} \quad h_{rc} \equiv \left.\frac{\partial v_{BC}}{\partial v_{EC}}\right|_Q \approx \left.\frac{\Delta v_{BC}}{\Delta v_{EC}}\right|_Q \tag{6}$$

$$\textit{Forward current gain} \quad h_{fc} \equiv \left.\frac{\partial i_E}{\partial i_B}\right|_Q \approx \left.\frac{\Delta i_E}{\Delta i_B}\right|_Q \tag{7}$$

$$\textit{Output admittance} \quad h_{oc} \equiv \left.\frac{\partial i_E}{\partial v_{EC}}\right|_Q \approx \left.\frac{\Delta i_E}{\Delta v_{EC}}\right|_Q \tag{8}$$

A circuit that satisfies (*3*) and (*4*) with definitions (*5*) to (*8*) is displayed by Fig. 6-16.

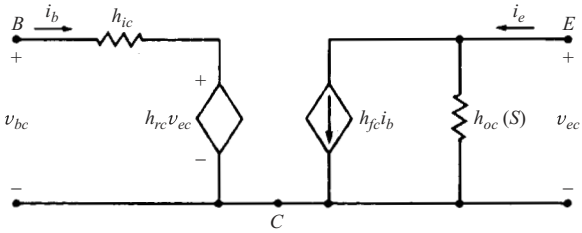


Fig. 6-16 CC small-signal equivalent circuit

6.14 Redraw the CE small-signal equivalent circuit of Fig. 6-1(*a*) so that the collector *C* is common to the input and output ports. Then apply KVL at the input port and KCL at the output port to find a set of equations that can be compared with (*3*) and (*4*) of Problem 6.13 to determine the CC *h* parameters in terms of the CE *h* parameters.

Figure 6-1(*a*) is rearranged, to make the collector common, in Fig. 6-17. Applying KVL around the *B*, *C* loop, with $v_{ce} = -v_{ec}$, results in

$$v_{bc} = h_{ie}i_b + h_{re}v_{ce} + v_{ec} = h_{ie}i_b + (1 - h_{re})v_{ec} \tag{1}$$

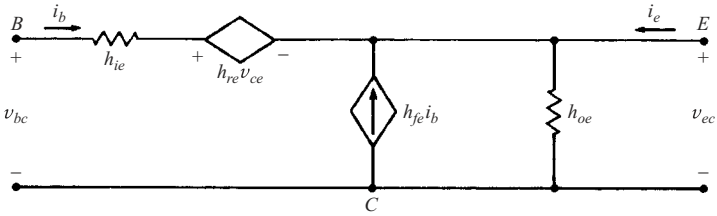


Fig. 6-17

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Applying KCL at node E gives

$$i_e = -i_b - h_{fe}i_b + h_{oe}v_{ec} = -(h_{fe}+1)i_b + h_{oe}v_{ec} \tag{2}$$

Comparison of (*1*) and (*2*) above with (*3*) and (*4*) of Problem 6.13 yields, by direct analogy,

$$h_{ic} = h_{ie} \qquad h_{rc} = 1 - h_{re} \qquad h_{fc} = -(h_{fe}+1) \qquad h_{oc} = h_{oe} \tag{3}$$

6.15 Use the CC transistor model of Fig. 6-16 to find the Thévenin equivalent for the circuit to the right of terminals B, C in Fig. 6-2(b), assuming $h_{rc} \approx 1$ and $h_{oc} \approx 0$. Compare the results with (*6.16*) to determine relationships between h_{ie} and h_{ic}, and between h_{fe} and h_{fc}.

The circuit to be analyzed is Fig. 6-16 with a resistor R_E connected from E to C. With terminal pair B, C open, the voltage across terminals C, E is zero; thus, the Thévenin equivalent circuit consists only of $Z_{Th} = R_{Th}$. Now consider v_{bc} as a driving-point source, and apply KVL around the B, C loop to obtain

$$v_{dp} = v_{bc} = h_{ic}i_b + h_{rc}v_{ec} \approx h_{ic}i_b + v_{ec} \tag{1}$$

Use KCL at node E to obtain

$$v_{ec} = -i_e R_E = -(h_{fc}i_b + h_{oc}v_{ce})R_E \approx -h_{fc}R_E i_b \tag{2}$$

Substitute (*2*) into (*1*), and solve for the driving-point impedance:

$$R_{Th} = \frac{v_{bc}}{i_b} = h_{ic} - h_{fc}R_E \tag{3}$$

Now (*3*) is compared with (*6.16*), it becomes apparent that $h_{ic} = h_{ie}$ and $h_{fc} = -(h_{fe}+1)$, as given in (*3*) of Problem 6.14.

6.16 Apply the definitions of the general h parameters given by (*1.16*) to (*1.19*) to the circuit of Fig. 6-1(b) to determine the CE h parameters in terms of the CB h parameters. Use the typically good approximations $h_{rb} \ll 1$ and $h_{ob}h_{ib} \ll 1 + h_{fb}$ to simplify the results.

By (*1.16*),

$$h_{ie} = \left.\frac{v_{be}}{i_b}\right|_{v_{ce}=0} \tag{1}$$

If $v_{ce} = 0$ (short-circuited) in the network of Fig. 6-1(b), then $v_{cb} = -v_{be}$, so that, by KVL around the E, B loop,

$$v_{be} = -h_{ib}i_e - h_{rb}v_{cb} = -h_{ib}i_e + h_{rb}v_{be}$$

which gives

$$i_e = \frac{h_{rb}-1}{h_{ib}}\,v_{be} \tag{2}$$

KCL at node B then gives

$$i_b = -(1+h_{fb})i_e - h_{ob}v_{cb} = \left[\frac{(1+h_{fb})(1-h_{rb})}{h_{ib}} + h_{ob}\right]v_{be}$$

Now, (*1*) and the given approximations,

$$h_{ie} = \frac{h_{ib}}{h_{ib}h_{ob} + (1+h_{fb})(1-h_{rb})} \approx \frac{h_{ib}}{1+h_{fb}}$$

By (*1.17*),

$$h_{re} = \left.\frac{v_{be}}{v_{ce}}\right|_{i_b=0} \tag{3}$$

If $i_b = 0$, then $i_c = -i_e$ in Fig. 6-1(b). By KVL,

$$v_{ce} = v_{cb} - h_{rb}v_{cb} - h_{ib}i_e = (1-h_{rb})v_{cb} - h_{ib}i_e \tag{4}$$

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KCL at node C then gives

$$i_c = -i_e = h_{fb} i_e + h_{ob} v_{cb}$$

so that

$$i_e = -\frac{h_{ob}}{1 + h_{fb}} \tag{5}$$

Substituting (5) into (4) with $v_{cb} = v_{ce} - v_{be}$ gives

$$v_{ce} = (1 - h_{rb})(v_{ce} - v_{be}) + \frac{h_{ib} h_{ob}}{1 + h_{fb}} (v_{ce} - v_{be})$$

After rearranging, (3) and the given approximations lead to

$$h_{re} = \frac{h_{rb}(1 + h_{fb}) - h_{ib} h_{ob}}{-h_{ib} h_{ob} + (h_{rb} - 1)(1 + h_{fb})} \approx \frac{h_{ib} h_{ob}}{1 + h_{fb}} - h_{rb}$$

By (*1.18*),

$$h_{fe} = \left. \frac{i_c}{i_b} \right|_{v_{ce}=0} \tag{6}$$

By KCL at node B of Fig. 6-1(b), with $v_{ce} = 0$ (and thus $v_{cb} = v_{eb} = -v_{be}$),

$$i_b = -(1 + h_{fb}) i_e - h_{ob} v_{cb} = -(1 + h_{fb}) i_e + h_{ob} v_{be}$$

Solving (2) for v_{be} with $i_e = -i_b - i_c$ and substituting now give

$$i_b = (1 + h_{fb})(i_b + i_c) + \frac{h_{ib} h_{ob}}{1 - h_{rb}} (i_b + i_c)$$

After rearranging, (6) and the given approximations lead to

$$h_{fe} = \frac{-h_{fb}(1 - h_{rb}) - h_{ib} h_{ob}}{(1 + h_{fb})(1 - h_{rb}) + h_{ib} h_{ob}} \approx \frac{-h_{fb}}{1 + h_{fb}}$$

By (*1.19*),

$$h_{oe} = \left. \frac{i_c}{v_{ce}} \right|_{i_b=0} \tag{7}$$

If $i_b = 0$, then $-i_c = i_e$. Replacing i_e with $-i_c$ in (4) and (5), solving (4) for v_{cb}, and substituting into (5) give

$$i_c = \frac{h_{ob}}{1 + h_{fb}} \left(\frac{v_{ce}}{1 - h_{rb}} - \frac{h_{ib}}{1 - h_{rb}} i_c \right)$$

After rearranging, (7) and the given approximations lead to

$$h_{oe} = \frac{h_{ob}}{(1 - h_{fb})(1 + h_{rb}) + h_{ib} h_{ob}} \approx \frac{h_{ob}}{1 + h_{fb}}$$

6.17 Apply the definitions of the z parameters given by (*1.10*) through (*1.13*) to the CB h-parameter circuit of Fig. 6-1(b) to find values for the z parameters in terms of the CB h parameters.

The circuit of Fig. 6-1(b) is described by the linear system of equations

$$\begin{bmatrix} h_{ib} & h_{rb} \\ h_{fb} & h_{ob} \end{bmatrix} \begin{bmatrix} i_e \\ v_{cb} \end{bmatrix} = \begin{bmatrix} v_{eb} \\ i_c \end{bmatrix} \tag{1}$$

By (*1.10*) and Fig. 1-8,

$$z_{11} = \left. \frac{v_{eb}}{i_e} \right|_{i_c=0} \tag{2}$$

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Setting $i_c = 0$ in (*1*) yields

$$v_{cb} = -\frac{h_{fb}}{h_{ob}}\, i_e \tag{3}$$

Substituting (*3*) into the first equation of (*1*) and applying (*2*) yield

$$z_{11} = h_{ib} - \frac{h_{rb}h_{fb}}{h_{ob}}$$

By (*1.12*) and (*3*),

$$z_{21} = \left.\frac{v_{cb}}{i_e}\right|_{i_c=0} = -\frac{h_{fb}}{h_{ob}}$$

By (*1.11*),

$$z_{12} = \left.\frac{v_{eb}}{i_c}\right|_{i_e=0} \tag{4}$$

Setting $i_e = 0$ in (*1*), solving the two equations for v_{cb}, and equating the results give

$$\frac{v_{eb}}{h_{rb}} = \frac{i_c}{h_{ob}} \qquad \text{from which} \qquad z_{12} = \frac{h_{rb}}{h_{ob}}$$

Finally, by (*1.13*),

$$z_{22} = \left.\frac{v_{cb}}{i_c}\right|_{i_e=0} \tag{5}$$

Letting $i_e = 0$ in the second equation of (*1*) and applying (*5*) yield $z_{22} = 1/h_{ob}$ directly.

6.18 For the CE amplifier of Fig. 3-17, assume that $h_{re} = h_{oe} \approx 0$, $h_{ie} = 1.1\,\text{k}\Omega$, $h_{fe} = 50$, $C_c \to \infty$, $R_F = 100\,\text{k}\Omega$, $R_S = 5\,\text{k}\Omega$, and $R_C = R_L + 20\,\text{k}\Omega$. Using CE h parameters, find and evaluate expressions for (*a*) $A_i = i_L/i_S$, (*b*) $A_i' = i_L/i_b$, (*c*) $A_v = v_L/v_S$, and (*d*) $A_v' = v_L/v_{be}$.

(*a*) The small-signal equivalent circuit for the amplifier is given in Fig. 6-18. By the method of node voltages,

$$\frac{v_s - v_{be}}{R_S} + \frac{v_{ce} - v_{be}}{R_F} - \frac{v_{be}}{h_{ie}} = 0 \tag{1}$$

$$\frac{v_{be} - v_{ce}}{R_F} - h_{fe}i_b - \frac{R_C + R_L}{R_C R_L}\, v_{ce} = 0 \tag{2}$$

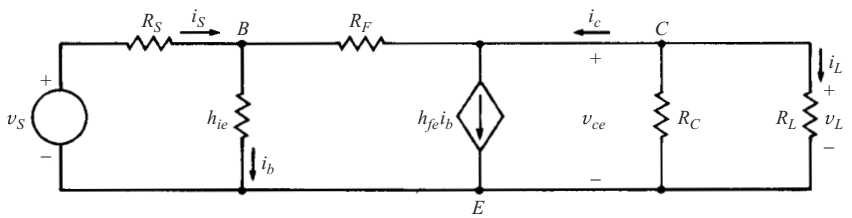


Fig. 6-18

Rearranging (*1*) and (*2*) and substituting $i_b = v_{be}/h_{ie}$ lead to

$$\begin{bmatrix} \dfrac{1}{R_S} + \dfrac{1}{R_F} + \dfrac{1}{h_{ie}} & -\dfrac{1}{R_F} \\ \dfrac{h_{fe}}{h_{ie}} - \dfrac{1}{R_F} & \dfrac{1}{R_F} + \dfrac{R_C + R_L}{R_C R_L} \end{bmatrix} \begin{bmatrix} v_{be} \\ v_{ce} \end{bmatrix} = \begin{bmatrix} \dfrac{v_S}{R_S} \\ 0 \end{bmatrix}$$

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The determinant of coefficients is then

$$\Delta = \left(\frac{1}{R_S}+\frac{1}{R_F}+\frac{1}{h_{ie}}\right)\left(\frac{1}{R_F}+\frac{R_C+R_L}{R_C R_L}\right)+\frac{1}{R_F}\left(\frac{h_{fe}}{h_{ie}}-\frac{1}{R_F}\right)$$
$$= \left(\frac{1}{5}+\frac{1}{100}+\frac{1}{1.1}\right)\left(\frac{1}{100}+\frac{10+10}{10\times 10}\right)(10^{-6})+\frac{1}{100}\left(\frac{50}{1.1}-\frac{1}{100}\right)10^{-6} = 4.557\times 10^{-6}$$

By Cramer's rule,

$$v_{be} = \frac{\Delta_1}{\Delta} = \frac{\left(\frac{1}{R_F}+\frac{R_C+R_L}{R_C R_L}\right)v_S}{R_S\,\Delta} = \frac{\left(\frac{1}{100}+\frac{1}{10}\right)(10^{-3})v_S}{(5\times 10^3)(4.557\times 10^{-6})} = 4.828\times 10^{-3}v_S \tag{3}$$

and
$$v_L = v_{ce} = \frac{\Delta_2}{\Delta} = \frac{\left(\frac{1}{R_F}-\frac{h_{fe}}{h_{ie}}\right)v_S}{R_S\,\Delta} = \frac{\left(\frac{1}{100}-\frac{50}{1.1}\right)(10^{-3})v_S}{(5\times 10^3)(4.557\times 10^{-6})} = -1.995v_S \tag{4}$$

So
$$A_i = \frac{i_L}{i_S} = \frac{v_L/R_L}{(v_S-v_{be})/R_S} = \frac{R_S v_L}{R_L(v_S-v_{be})} = \frac{(5\times 10^3)(-1.995v_S)}{(20\times 10^3)(v_S-4.828\times 10^{-3}v_S)} = -0.501$$

(*b*)
$$A_i' = \frac{i_L}{i_b} = \frac{v_L/R_L}{v_{be}/h_{ie}} = \frac{h_{ie}v_L}{R_L v_{be}} = \frac{(1.1\times 10^3)(-1.995v_s)}{(20\times 10^3)(4.828\times 10^{-3}v_S)} = -22.73$$

(*c*)
$$A_v = \frac{v_L}{v_S} = \frac{-1.995v_S}{v_S} = -1.995$$

(*d*)
$$A_v' = \frac{v_L}{v_{be}} = \frac{-1.995v_S}{4.828\times 10^{-3}v_S} = -413.2$$

6.19 In the CB amplifier of Fig. 6-19(*a*), let $R_1 = R_2 = 50\,\text{k}\Omega$, $R_C = 2.2\,\text{k}\Omega$, $R_E = 3.3\,\text{k}\Omega$, $R_L = 1.1\,\text{k}\Omega$, $C_C = C_B \to \infty$, $h_{rb} \approx 0$, $h_{ib} = 25\,\Omega$, $h_{ob} = 10^{-6}\,\text{S}$, and $h_{fb} = -0.99$. Find and evaluate expressions for (*a*) the voltage-gain ratio $A_v = v_L/v_s$ and (*b*) the current-gain ratio $A_i = i_L/i_s$.

(*a*) With $h_{rb} = 0$, the CB *h*-parameter model of Fig. 6-1(*b*) can be used to draw the small-signal circuit of Fig. 6-19(*b*). By Ohm's law at the input mesh,

$$i_e = \frac{v_s}{h_{ib}} \tag{1}$$

Ohm's law at the output mesh requires that

$$v_L = \left(\frac{1}{h_{ob}} \| R_C \| R_L\right)(-h_{fb}i_e) = -\frac{R_C R_L h_{fb} i_e}{R_C + R_L + h_{ob}R_C R_L} \tag{2}$$

Substitution of (*1*) into (*2*) allows the formation of A_v:

$$A_v = \frac{v_L}{v_s} = -\frac{R_C R_L h_{fb}}{h_{ib}(R_C + R_L + h_{ob}R_C R_L)}$$
$$= -\frac{(2.2\times 10^3)(1.1\times 10^3)(-0.99)}{(25)[2.2\times 10^3 + 1.1\times 10^3 + (10^{-6})(2.2\times 10^3)(1.1\times 10^3)]} = 29.02$$

(*b*) By current division at node *E*,

$$i_e = \frac{R_E}{R_E + h_{ib}}\, i_s \tag{3}$$

Current division at node *C* gives

$$i_L = \frac{(1/h_{ob}) \| R_C}{(1/h_{ob}) \| R_C + R_L}(-h_{fb}i_e) = -\frac{R_C h_{fb} i_e}{R_C + R_L + h_{ob}R_L R_C} \tag{4}$$

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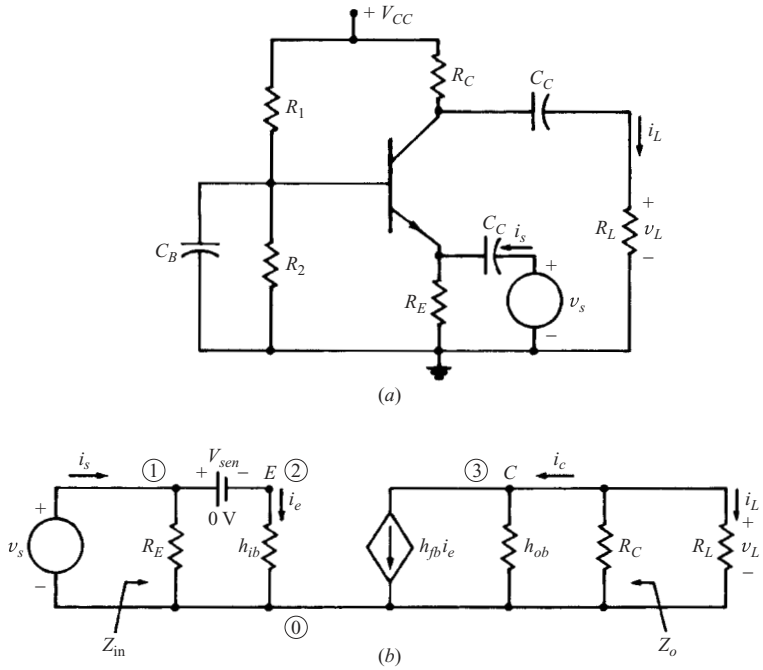


Fig. 6-19

Now substitution of (*3*) into (*4*) allows direct calculation of A_i:

$$A_i = \frac{i_L}{i_s} = -\frac{R_E R_C h_{fb}}{(R_E + h_{ib})(R_C + R_L + h_{ob} R_L R_C)}$$

$$= \frac{(3.3 \times 10^3)(2.2 \times 10^3)(-0.99)}{-(3.3 \times 10^3 + 25)[2.2 \times 10^3 + 1.1 \times 10^3 + (10^{-6})(1.1 \times 10^3)(2.2 \times 10^3)]} = 0.655$$

6.20 Let $v_S = \sin(2000\pi t)$ V and apply SPICE methods to the small-signal equivalent circuit of Fig. 6-19(*b*) to solve Problem 6.19.

(*a*) The netlist code below describes the circuit:

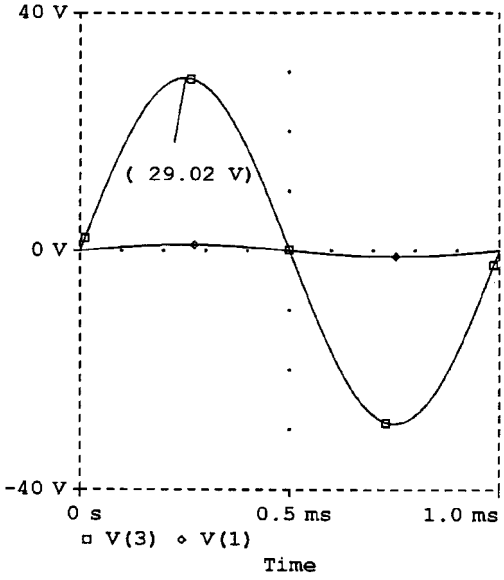
```
Prb6_20.CIR
vs    1 0 SIN( 0V 1V 1kHz )
RE    1 0 3.3kohms
Rhib  1 2 25ohms
Vsen  2 0 DC 0V
Fhfb  3 0 Vsen -0.99
Rhob  3 0 {1/1e-6S}
RC    3 0 2.2kohms
RL    3 0 1.1kohms
.TRAN 5 us 1ms
.PROBE
.END
```

After executing ⟨Prb6_20.CIR⟩, the traces of the input voltage $v_S = \text{V}(1)$ and the output voltage $v_L = \text{V}(3)$ of Fig. 6-20(*a*) are generated using the Probe feature of PSpice. Since the input voltage

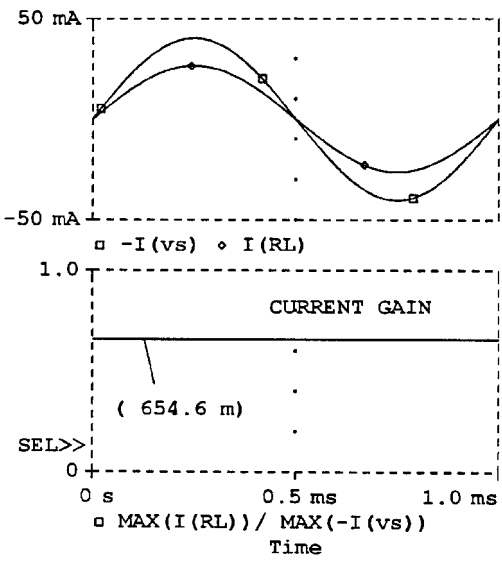
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has been conveniently selected at 1 V peak, the voltage gain is simply equal to the peak value of v_L, or $A_v = 29.02$ as marked on Fig. 6-20(*a*).

(*b*) The resulting instantaneous waveforms for $i_S = -\text{I(vs)}$ and $i_L = \text{I(RL)}$ are shown by the upper plot of Fig. 6-20(*b*). The current gain is determined by the ratio of maximum or peak values of output current (i_L) to input current (i_S) as displayed by the lower plot of Fig. 6-20(*b*) where $A_i = 654.6 \times 10^{-3}$.



(*a*)



(*b*)

Fig. 6-20

6.21 Use the CC *h*-parameter model of Fig. 6-16 to find expressions for the current-gain ratios (*a*) $A_i' = i_e/i_b$ and (*b*) $A_i = i_e/i_i$ for the amplifier of Fig. 6-2(*a*).

(*a*) The equivalent circuit is given in Fig. 6-21. At the output port,

$$-i_e R_E = v_{ec} = -h_{fc} i_b \left(\frac{1}{h_{oc}} \| R_E \right) = -\frac{h_{fc} R_E}{h_{oc} R_E + 1}\, i_b \tag{1}$$

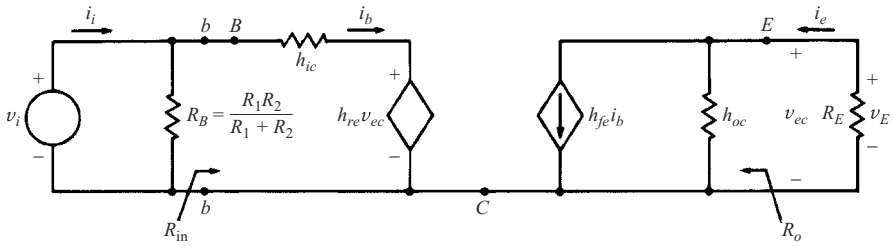


Fig. 6-21

and A_i' is obtained directly from (*1*) as

$$A_i' = \frac{i_e}{i_b} = \frac{h_{fc}}{h_{oc} R_E + 1}$$

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(*b*) With $R_{Th} = R_{in} = h_{ic} - h_{rc}h_{fc}R_E/(h_{oc}R_E + 1)$, current division at node B gives

$$\frac{i_b}{i_e} = \frac{1}{A_i'} = \frac{R_B}{R_B + R_{\text{in}}}\frac{i_i}{i_e} = \frac{R_B}{R_B + R_{\text{in}}}\frac{1}{A_i}$$

so

$$A_i = \frac{R_B}{R_B + R_{\text{in}}}A_i' = \frac{R_B}{R_B + h_{ic} + h_{rc}h_{fc}R_E/(h_{oc}R_E + 1)}\frac{h_{fc}}{h_{oc}R_E + 1}$$

$$= \frac{h_{fc}R_B}{(R_B + h_{ic})(h_{oc}R_E + 1) + h_{rc}h_{fc}R_E}$$

6.22 In the two-stage amplifier of Fig. 6-22, the transistors are identical, having $h_{ie} = 1500\,\Omega$, $h_{fe} = 40$, $h_{re} \approx 0$, and $h_{oe} = 30\,\mu\text{S}$. Also, $R_i = 1\,\text{k}\Omega$, $R_{C2} = 20\,\text{k}\Omega$, $R_{C1} = 10\,\text{k}\Omega$,

$$R_{B1} \equiv \frac{R_{11}R_{12}}{R_{11} + R_{12}} = 5\,\text{k}\Omega \qquad \text{and} \qquad R_{B2} = \frac{R_{21}R_{22}}{R_{21} + R_{22}} = 5\,\text{k}\Omega$$

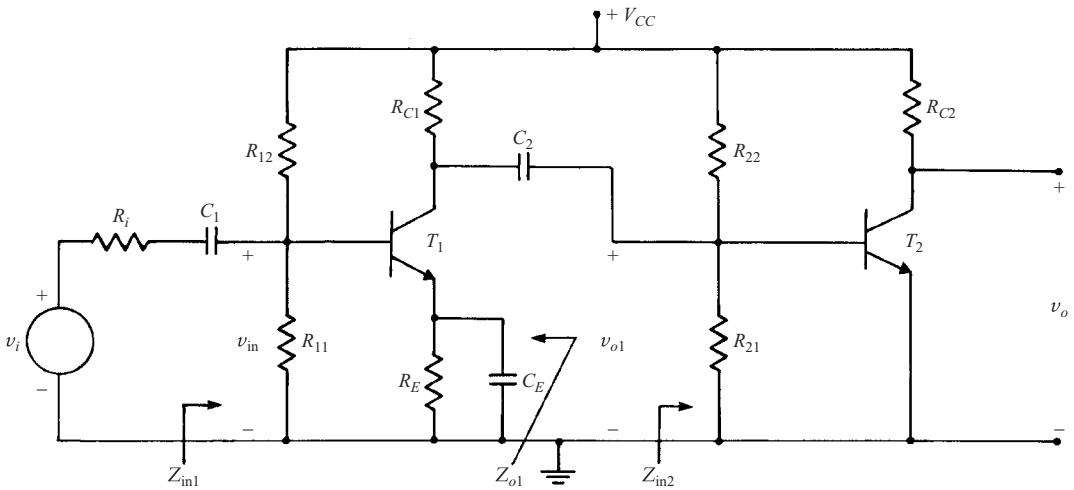


Fig. 6-22

Find (*a*) the final-stage voltage gain $A_{v2} \equiv v_o/v_{o1}$; (*b*) the final-stage input impedance Z_{in2}; (*c*) the initial-stage voltage gain $A_{v1} \equiv v_{o1}/v_{\text{in}}$; (*d*) the amplifier input impedance Z_{in1}; and (*e*) the amplifier voltage gain $A_v \equiv v_o/v_i$.

(*a*) The final-stage voltage gain is given by the result of Problem 6.7(*a*) if the parallel combination of R_L and R_C is replaced with R_{C2}:

$$A_{v2} = -\frac{h_{fe}R_{C2}}{h_{ie}(1 + h_{oe}R_{C2})} = -\frac{(40)(20 \times 10^3)}{(1500)[(1 + (30 \times 10^{-6})(20 \times 10^3)]} = -333.3$$

(*b*) From (*4*) of Problem 6.11 with $h_{re} \approx 0$,

$$Z_{\text{in2}} = \frac{R_{B2}h_{ie}}{R_{B2} + h_{ie}} = \frac{(5 \times 10^3)(1500)}{5 \times 10^3 + 1500} = 1.154\,\text{k}\Omega$$

(*c*) The initial-stage voltage gain is given by the result of Problem 6.7(*a*) if R_C and R_L are replaced with R_{C1} and Z_{in2}, respectively:

$$A_{v1} = -\frac{h_{fe}Z_{\text{in2}}R_{C1}}{h_{ie}(R_{C1} + Z_{\text{in2}} + h_{oe}Z_{\text{in2}}R_{C1})} = -\frac{(40)(1154)(10^4)}{(1500)(10^4 + 1154 + 346.2)} = -26.8$$

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(*d*) As in part *b*,

$$Z_{\text{in1}} = \frac{R_{B1} h_{ie}}{R_{B1} + h_{ie}} = 1.154\,\text{k}\Omega$$

(*e*) By voltage division,

$$\frac{v_{\text{in}}}{v_i} = \frac{Z_{\text{in1}}}{Z_{\text{in1}} + R_i} = \frac{1154}{1154 + 1000} = 0.5357$$

and

$$A_v \equiv \frac{v_o}{v_i} = \frac{v_{\text{in}}}{v_i} A_{v1} A_{v2} = (0.5357)(-26.8)(-333.3) = 4786$$

6.23 In the amplifier of Fig. 6-23(*a*), the transistors are identical and have $h_{re} = h_{oe} \approx 0$. Use the CE *h*-parameter model to draw an equivalent circuit and find expressions for (*a*) the current-gain ratio $A_i = i_E/i_i$, (*b*) the input resistance R_{in}, (*c*) the voltage-gain ratio $A_v = v_o/v_i$, and (*d*) the output resistance R_o.

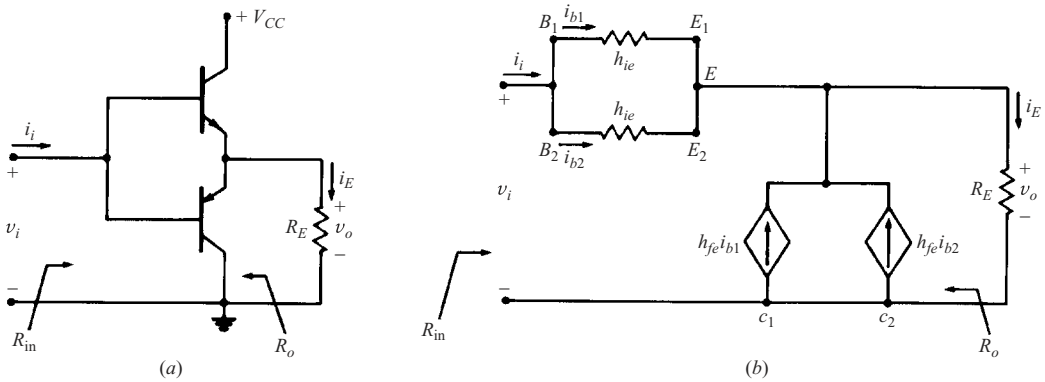


Fig. 6-23

(*a*) With $h_{re} = h_{oe} \approx 0$, the small-signal equivalent circuit is given by Fig. 6-23(*b*). KCL at node *E* gives

$$i_E = h_{fe} i_{b1} + h_{fe} i_{b2} + i_{b1} + i_{b2} = (h_{fe} + 1)(i_{b1} + i_{b2}) \tag{1}$$

Since $i_i = i_{b1} + i_{b2}$, the current-gain ratio follows directly from (*1*) and is $A_i = h_{fe} + 1$.

(*b*) KVL applied around the outer loop gives

$$v_i = (h_{ie} \| h_{ie}) i_i + R_E (h_{fe} + 1) i_i$$

so that

$$R_{\text{in}} = \frac{v_i}{i_i} = \frac{1}{2} h_{ie} + (h_{fe} + 1) R_E \tag{2}$$

(*c*) By KVL,

$$v_o = v_i - (h_{ie} \| h_{ie}) i_i = v_i - \tfrac{1}{2} h_{ie} i_i \tag{3}$$

But

$$i_i = \frac{v_i}{R_{\text{in}}} \tag{4}$$

Substitution of (*4*) and then (*2*) into (*3*) allows solution for the voltage-gain ratio as

$$A_v = \frac{v_o}{v_i} = 1 - \frac{1}{2} \frac{h_{ie}}{R_{\text{in}}} = 1 - \frac{\frac{1}{2} h_{ie}}{\frac{1}{2} h_{ie} + (h_{fe} + 1) R_E} = \frac{(h_{fe} + 1) R_E}{\frac{1}{2} h_{ie} + (h_{fe} + 1) R_E}$$

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(*d*) If R_E is replaced by a driving-point source with v_i shorted, KCL requires that

$$i_{dp} = -h_{fe}(i_{b1} + i_{b2}) + \frac{v_{dp}}{h_{ie} \| h_{ie}} \tag{5}$$

But

$$i_{b1} + i_{b2} = i_i = -\frac{v_{dp}}{h_{ie} \| h_{ie}} = -\frac{v_{dp}}{\frac{1}{2}h_{ie}} \tag{6}$$

Substituting (*6*) into (*5*) leads to

$$R_o = \frac{v_{dp}}{i_{dp}} = \frac{1}{h_{fe}/\frac{1}{2}h_{ie} + 1/\frac{1}{2}h_{ie}} = \frac{h_{ie}}{2(h_{fe}+1)}$$

6.24 The cascaded amplifier of Fig. 6-24(*a*) uses a CC first stage followed by a CE second stage. Let $R_S = 0$, $R_{11} = 100\,\text{k}\Omega$, $R_{12} = 90\,\text{k}\Omega$, $R_{21} = 10\,\text{k}\Omega$, $R_{22} = 90\,\text{k}\Omega$, $R_L = R_C = 5\,\text{k}\Omega$, and $R_E = 9\,\text{k}\Omega$. For transistor Q_1, $h_{oc} \approx 0$, $h_{ic} = 1\,\text{k}\Omega$, $h_{rc} \approx 1$, and $h_{fc} = -100$. For Q_2, $h_{re} = h_{oe} \approx 0$, $h_{fe} = 100$, and $h_{ie} = 1\,\text{k}\Omega$. Find (*a*) the overall voltage-gain ratio $A_v = v_L/v_s$ and (*b*) the overall current-gain ratio $A_i = i_L/i_s$.

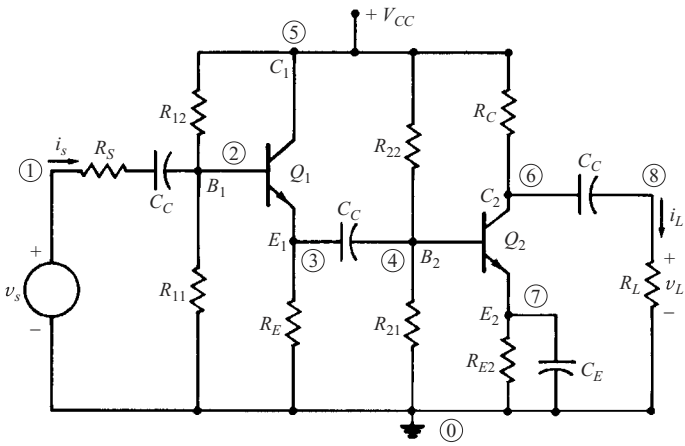


Fig. 6-24

(*a*) The small-signal equivalent circuit is drawn in Fig. 6-24(*b*), where

$$R_{B1} = R_{11} \| R_{12} = \frac{(90 \times 10^3)(100 \times 10^3)}{90 \times 10^3 + 100 \times 10^3} = 47.37\,\text{k}\Omega$$

and

$$R_{B2} = R_{22} \| R_{21} = \frac{(90 \times 10^3)(10 \times 10^3)}{90 \times 10^3 + 10 \times 10^3} = 4.5\,\text{k}\Omega$$

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From the results of Problem 6.44,

$$A_{v1} = -\frac{h_{fc}(R_E \| R_{B2} \| h_{ie})}{h_{ic} - h_{rc}h_{fc}(R_E \| R_{B2} \| h_{ie})} = -\frac{(-100)(818.2)}{1 \times 10^3 - (1)(-100)(818.2)} = 0.9879$$

and from the results of Problem 6.7,

$$A_{v2} = -\frac{h_{fe}R_L R_C}{h_{ie}(R_L + R_C)} = -\frac{(100)(5 \times 10^3)(5 \times 10^3)}{(1 \times 10^3)(5 \times 10^3 + 5 \times 10^3)} = -100$$

Then $$A_v = A_{v1}A_{v2} = (0.9879)(-100) = -98.79$$

(*b*) From the results of Problem 6.21,

$$A_{i1} = \frac{-i_{e1}}{i_s} = -\frac{h_{fc}R_{B1}}{R_{B1} + h_{ic} + h_{rc}h_{fc}(R_E \| R_{B2} \| h_{ie})} = -\frac{(-100)(47.37 \times 10^3)}{47.37 \times 10^3 + 1 \times 10^3 + (1)(-100)(818.2)}$$
$$= 36.38$$

and again from Problem 6.7,

$$A_{i2} = \frac{(R_E \| R_{B2})h_{ie}}{R_L(R_E \| R_{B2} + h_{ie})} A_{v2} = \frac{(4.5 \times 10^3)(1 \times 10^3)}{(5 \times 10^3)(4.5 \times 10^3 + 1 \times 10^3)}(-100) = -16.36$$

Then $$A_i = A_{i1}A_{i2} = (36.38)(-16.36) = -595.2$$

Note that, in this problem, we made use of the labor-saving technique of applying results determined for single-stage amplifiers to the individual stages of a cascaded (multistage) amplifier.

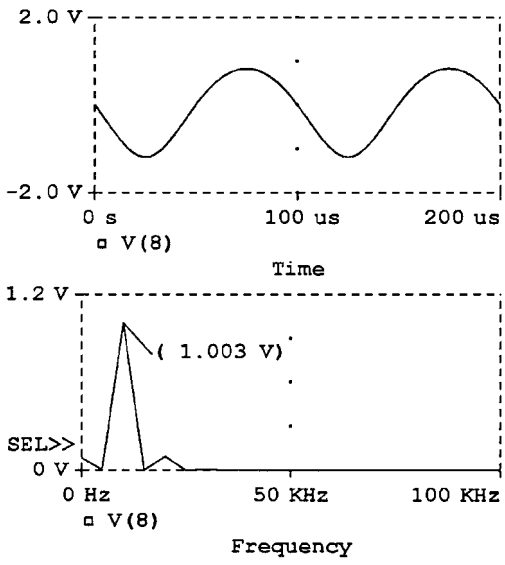
6.25 For the cascaded amplifier of Fig. 6-24(*a*), let $C_C = C_E = 100\,\mu\text{F}$, $R_{E2} = 600\,\Omega$, and $v_S = 10\sin(20\pi \times 10^3)\,\text{mV}$. All other resistors have the values of Problem 6.24. The transistors are characterized by the SPICE default *npn* model. Apply SPICE methods to determine (*a*) the overall voltage gain and (*b*) the overall current gain.

(*a*) The following netlist code describes the circuit:

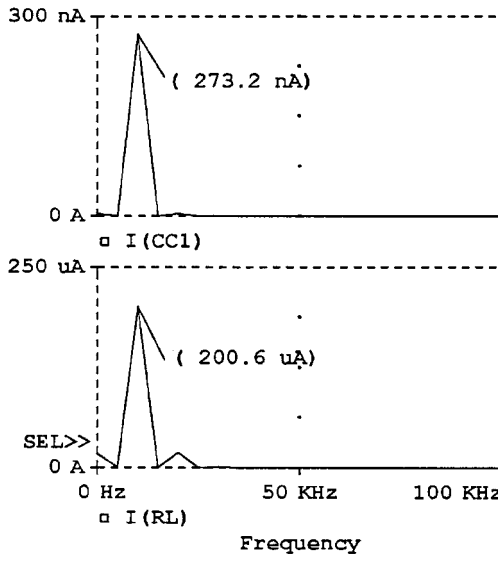
```
Prb6_25.CIR
vs   1 0 SIN(0 10mV 10kHz)
VCC  5 0 DC 15V
CC1  1 2 100uF
CC2  3 4 100uF
CC3  6 8 100uF
CE   7 0 100uF
R11  2 0 100kohm
R12  5 2 90kohm
R22  5 4 90kohm
R21  4 0 10kohm
RE   3 0 9kohm
RC   5 6 5kohm
RL   8 0 5kohm
RE2  7 0 600ohm
Q1   5 2 3 QNPN
Q2   6 4 7 QNPN
.MODEL QNPN NPN()
.PROBE
.TRAN 5us 0.2ms 0s 1us
.END
```

Execute ⟨Prb6_25.CIR⟩ and use the Probe feature of PSpice to plot the waveform of output voltage v_L shown in the upper plot of Fig. 6-25(*a*). Since the waveform has some distortion, the Fourier trans-

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(*a*)



(*b*)

Fig. 6-25

form has been implemented using the FFT feature of PSpice to determine the value of the fundamental frequency component of v_L as shown in the lower plot of Fig. 6-25(*a*). Then

$$A_v = -\frac{1.003}{0.01} = -100.3$$

The negative sign indicates that v_L has a 180° phase shift with respect to v_S.

(*b*) Use the Probe and FFT features of PSpice to plot the Fourier spectra of the input current I(CC1) and the output current I(RL) as shown by Fig. 6-25(*b*). The current gain is found as the ratio of the marked spectra fundamental component values of Fig. 6-25(*b*).

$$A_i = -\frac{200.6 \times 10^{-3}}{273.2 \times 10^{-6}} = -734.3$$

The negative sign indicates a 180° phase shift between i_S and i_L.

6.26 The cascaded amplifier of Fig. 6-26(*a*) is built up with identical transistors for which $h_{re} = h_{oe} \approx 0$, $h_{fe} = 100$, and $h_{ie} = 1\,\text{k}\Omega$. Let $R_{E1} = 1\,\text{k}\Omega$, $R_{C1} = 10\,\text{k}\Omega$, $R_{E2} = 100\,\Omega$, $R_{C2} = R_L = 3\,\text{k}\Omega$, and $C_c = C_E \to \infty$. Determine (*a*) the overall voltage-gain ratio $A_v = v_L/v_s$, and (*b*) the overall current-gain ratio $A_i = i_L/i_s$.

(*a*) The small-signal equivalent circuit is given in Fig. 6-26(*b*). From the results of Problem 6.7 with $h_{oe} = 0$ and R_C replaced with R_{C2},

$$A_{v2} = -\frac{h_{fe}R_L R_{C2}}{h_{ie}(R_L + R_{C2})} = -\frac{(100)(3 \times 10^3)(3 \times 10^3)}{(1 \times 10^3)(3 \times 10^3 + 3 \times 10^3)} = -150$$

From the results of Problems 6.48, in which R_C, R_L, and R_E are replaced with R_{C1}, h_{ie}, and R_{E1}, respectively,

$$A_{v1} = -\frac{h_{fe}R_{C1}h_{ie}}{(R_{C1} + h_{ie})[(h_{fe} + 1)R_{E1} + h_{ie}]} = -\frac{(100)(10 \times 10^3)(1 \times 10^3)}{(11 \times 10^3)[(100 + 1)(1 \times 10^3) + 1 \times 10^3]} = -0.891$$

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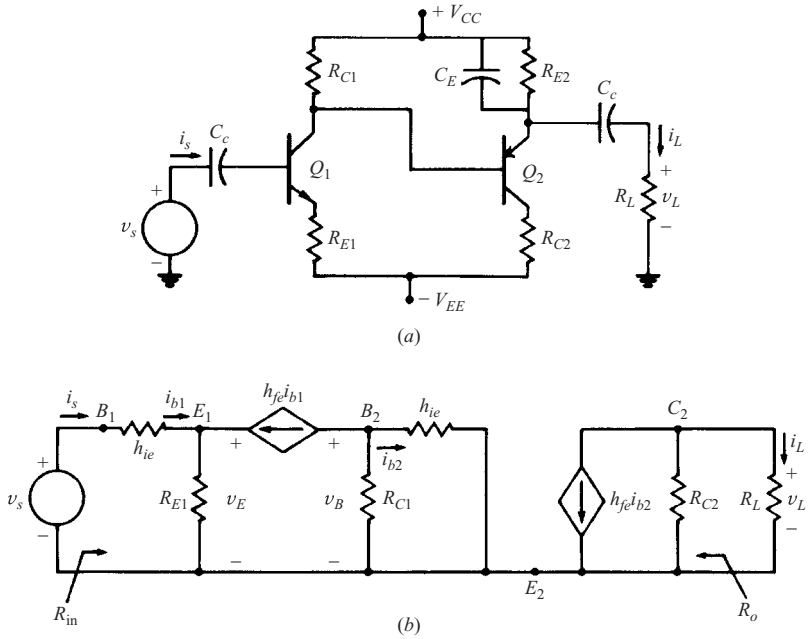


Fig. 6-26

Thus, $$A_v = A_{v1}A_{v2} = (-0.891)(-150) = 133.6$$

(*b*) From the results of Problem 6.48 with R_C and R_L replaced with R_{C1} and h_{ie}, respectively,

$$A_{i1} = -\frac{h_{fe}R_{C1}}{R_{C1} + h_{ie}} = -\frac{(100)(10 \times 10^3)}{10 \times 10^3 + 1 \times 10^3} = -90.91$$

Now, by current division at the output network,

$$i_L = -h_{fe}i_{b2}\frac{R_{C2}}{R_{C2} + R_L}$$

Hence, $$A_{i2} = \frac{i_L}{i_{b2}} = -\frac{h_{fe}R_{C2}}{R_{C2} + R_L} = -\frac{(100)(3 \times 10^3)}{3 \times 10^3 + 3 \times 10^3} = -50$$

and $$A_i = A_{i1}A_{i2} = (-90.91)(-50) = 4545.4$$

6.27 In the cascaded CB-CC amplifier of Fig. 6-27(*a*), transistor Q_1 is characterized by $h_{rb1} = h_{ob1} \approx 0$, $h_{ib1} = 50\,\Omega$, and $h_{fb1} = -0.99$. The h parameters of transistor Q_2 are $h_{oc2} \approx 0$, $h_{rc2} = 1$, $h_{ic2} = 500\,\Omega$, and $h_{fc2} = -100$. Let $R_L = R_{E2} = 2\,\text{k}\Omega$, $R_{B1} = 30\,\text{k}\Omega$, $R_{B2} = 60\,\text{k}\Omega$, $R_1 = 50\,\text{k}\Omega$, $R_2 = 100\,\text{k}\Omega$, $R_{E1} = 5\,\text{k}\Omega$, and $C_B = C_c \to \infty$. Find (*a*) the overall voltage-gain ratio $A_v = v_L/v_S$ and (*b*) the overall current-gain ratio $A_i = i_L/i_S$.

(*a*) The small-signal equivalent circuit is shown in Fig. 6-27(*b*). From the results of Problem 6.19, with $R_B = R_1 \| R_2$,

$$A_{v1} = -\frac{h_{fb1}R_B h_{ic2}}{h_{ib1}(R_B + h_{ic2})} = -\frac{(-0.99)(33.3 \times 10^3)(500)}{(50)(33.3 \times 10^3 + 500)} = 9.75$$

By the results of Problem 6.44,

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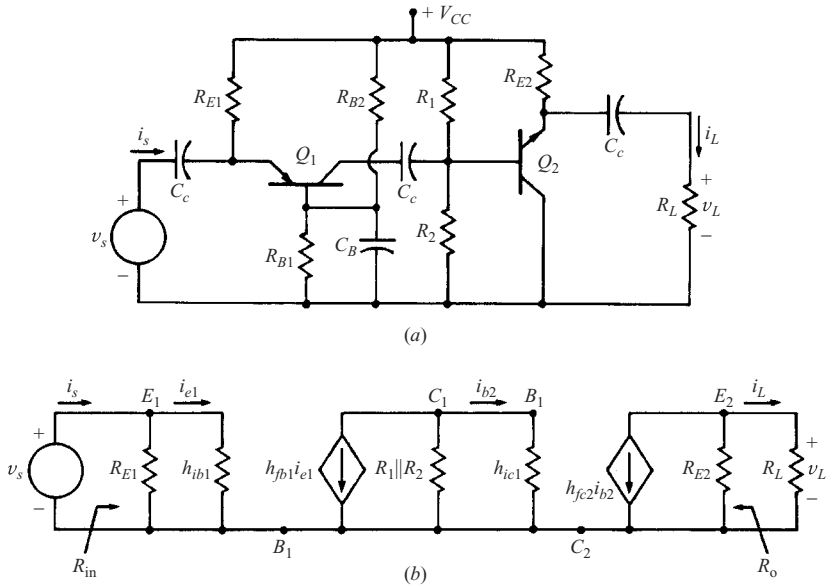


Fig. 6-27

$$A_{v2} = -\frac{h_{fc2}(R_{E2} \| R_L)}{h_{ic2} - h_{rc2}h_{fc2}(R_{E2} \| R_L)} = -\frac{(-100)(1 \times 10^3)}{500 - (1)(-100)(1 \times 10^3)} = 0.995$$

Thus,
$$A_v = A_{v1}A_{v2} = (9.75)(0.995) = 9.70$$

(*b*) Based on the results of Problem 6.19,

$$A_{i1} = -\frac{h_{fb2}R_{E1}R_B}{(R_{E1} + h_{ib1})(R_B + h_{ic2})} = -\frac{(-0.99)(5 \times 10^3)(33.3 \times 10^3)}{(5 \times 10^3 + 50)(33.3 \times 10^3 + 500)} = 0.966$$

By current division at node E_2,

$$\frac{i_L}{i_{b2}} = A_{i2} = -\frac{h_{fc2}R_{E2}}{R_{E2} + R_L} = -\frac{(-100)(2 \times 10^3)}{(2 \times 10^3) + (2 \times 10^3)} = 50$$

Then,
$$A_i = A_{i1}A_{i2} = (0.966)(50) = 48.3$$

6.28 Use the CE *h*-parameter model to calculate the output voltage v_o for the amplifier of Fig. 3-22, thus demonstrating that it is a *difference amplifier*. Assume identical transistors with $h_{re} = h_{oe} \approx 0$.

The small-signal circuit is given in Fig. 6-28. Let $a = h_{ie} + (h_{fe} + 1)R_E$ and $b = (h_{fe} + 1)R_E$; then, by KVL,

$$v_1 = ai_{b1} + bi_{b2} \tag{1}$$
$$v_2 = b_1 i_{b1} + ai_{b2} \tag{2}$$
$$v_o = h_{fe}R_C(i_{b1} - i_{b2}) \tag{3}$$

Solving (*1*) and (*2*) simultaneously using Cramer's rule gives

$$\Delta = a^2 - b^2$$

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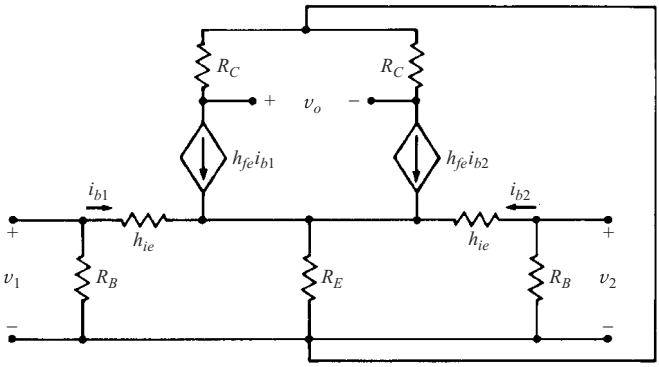


Fig. 6-28

and
$$i_{b1} = \frac{\Delta_1}{\Delta} = \frac{av_1 - bv_2}{a^2 - b^2} \tag{4}$$

$$i_{b2} = \frac{\Delta_2}{\Delta} = \frac{av_2 - bv_1}{a^2 - b^2} \tag{5}$$

Substituting (*4*) and (*5*) into (*3*) gives, finally,

$$v_o = \frac{h_{fe}R_C}{a^2 - b^2}(av_1 - bv_2 - av_2 + bv_1) = \frac{h_{fe}R_C}{a - b}(v_1 - v_2) = \frac{h_{fe}}{h_{ie}}R_C(v_1 - v_2)$$

which clearly shows that the circuit amplifies the *difference* between signals v_1 and v_2.

Supplementary Problems

6.29 For the CB amplifier of Fig. 3-23, find the voltage-gain ratio $A_v = v_L/v_{eb}$ using the tee-equivalent circuit of Fig. 6-3 if r_c is large enough that $i_c \approx \alpha i_e$. *Ans.* $A_v = (\alpha R_C R_L)/\{(R_C + R_L)[r_e + (1 - \alpha)r_b]\}$

6.30 For the CB amplifier of Fig. 3-23 and Problem 6.29, $R_C = R_L = 4\,\text{k}\Omega$, $r_e = 30\,\Omega$, $r_b = 300\,\Omega$, $r_c = 1\,\text{M}\Omega$, and $\alpha = 0.99$. Determine the percentage error in the approximate voltage gain of Problem 6.29 (in which we assumed $i_c \approx \alpha i_e$), relative to the exact gain as determined in Problem 6.1.
Ans. Approximate gain is 1.99 percent greater.

6.31 Use the *r*-parameter equivalent circuit of Fig. 6-10(*b*) to find the current-gain ratio $A_i = i_L/i_b$ for the CE amplifier of Fig. 3-10.

Ans. $A_i = \dfrac{R_C(r_e - r_m)}{(R_C + R_L)[(1 - \alpha)r_c + r_e] + R_C R_L}$

6.32 For the EF amplifier of Fig. 3-26(*a*), use an appropriate *r*-parameter model of the transistor to calculate the current-gain ratio $A_i = i_L/i_s$.

Ans. $A_i = \dfrac{R_E R_B r_c}{(R_E + R_L)(R_B + r_b)[r_e + (1 - \alpha)r_c + R_E \| R_L] + (R_E + R_L)r_c(r_e + R_E \| R_L)}$

6.33 Apply the definitions of the *h* parameters, given by (*1.16*) through (*1.19*), to the *r*-parameter circuit of Fig. 6-3 to find the CB *h* parameters in terms of the *r* parameters.
Ans. $h_{ib} = r_e + (1 - \alpha)r_b r_c/(r_b + r_c)$, $h_{rb} = r_b/(r_b + r_c)$, $h_{fb} = -(r_b + \alpha r_c)/(r_b + r_c)$, $h_{ob} = 1/(r_b + r_c)$

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6.34 Apply the definitions of the z parameters, given by (*1.10*) through (*1.13*), to the circuit of Fig. 6-3 to find values for the z parameters in the equivalent circuit of Fig. 6-29, which contains two dependent voltage sources. *Ans.* $z_{11} = r_e + r_b, z_{12} = r_b, z_{21} = r_b + \alpha r_c, z_{22} = r_b + r_c$

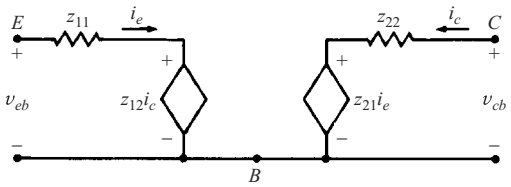


Fig. 6-29

6.35 Apply the definitions of the z parameters, given by (*1.10*) through (*1.13*), to the CE h-parameter circuit of Fig. 6-1(*a*) to find values for the z parameters in the equivalent circuit of Fig. 6-29 in terms of the CE h parameters. *Ans.* $z_{11} = h_{ie} - h_{fe}h_{re}/h_{oe}, z_{12} = h_{re}/h_{oe}, z_{21} = -h_{fe}/h_{oe}, z_{22} = 1/h_{oe}$

6.36 Use the z-parameter model of Fig. 6-29 to calculate (*a*) the current-gain ratio $A_i = i_L/i_i$ and (*b*) the voltage-gain ratio $A_v = v_L/v_i$ for the amplifier of Fig. 3-10(*a*).
Ans. $A_i = R_C R_B z_{21}/(R_C + R_L)[(R_B + z_{11})(z_{22} + R_C \| R_L) + z_{12}z_{21}]$,
$A_v = z_{21}R_B(R_L \| R_C)/\{(z_{22} + R_C \| R_L)[R_B R_i + z_{11}(R_B + R_i)]\}$

6.37 For the CE amplifier of Fig. 3-17 with values as given in Problem 6.18, find (*a*) the input resistance R_i and (*b*) the output resistance R_o. *Ans.* (*a*) 24.26 Ω; (*b*) 2.154 kΩ

6.38 A CE transistor amplifier is operating in the active region, with $V_{CC} = 12$ V and $R_{dc} = 2$ kΩ. If the collector characteristics are given by Fig. 3-9(*b*) and the quiescent base current is 30 μA, determine (*a*) h_{fe} and (*b*) h_{oe}. *Ans.* (*a*) 190; (*b*) 83.33 μS

6.39 In the circuit of Fig. 6-30, $h_{re} = 10^{-4}$, $h_{ie} = 200$ Ω, $h_{fe} = 100$, and $h_{oe} = 100$ μS. (*a*) Find the power gain as $A_p = |A_i A_v|$, the product of the current and voltage gains. (*b*) Determine the numerical value of R_L that maximizes the power gain. *Ans.* (*a*) $h_{fe}^2/|(h_{oe}R_L + 1)(h_{oe}h_{ie} - h_{re}h_{fe}h_{ie}R_L^{-1})|$; (*b*) 14.14 kΩ

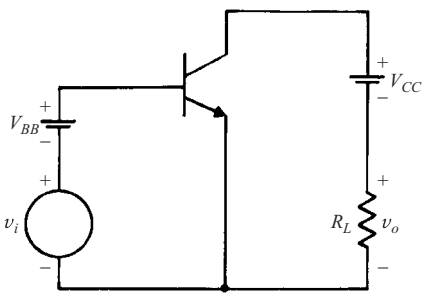


Fig. 6-30

6.40 The EF amplifier of Fig. 3-26(*a*) utilizes a Si transistor with negligible leakage current and $\beta = 59$. Also, $V_{CC} = 15$ V, $V_L = 3$ V (V_L is the dc component of v_L), and $R_E = 1.5$ kΩ. Calculate (*a*) R_B, (*b*) the output impedance Z_o, and (*c*) the input impedance Z_{in}.
Ans. (*a*) 339 kΩ; (*b*) 1.185 kΩ; (*c*) 50.98 kΩ

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6.41 The amplifier of Fig. 6-31 has an adjustable emitter resistor R_E, as indicated, with $0 \le \lambda \le 1$. Assume that $h_{re} = h_{oe} \approx 0$ and $C_c \to \infty$, and find expressions for (*a*) the current-gain ratio $A_i = i_L/i_s$, (*b*) the voltage-gain ratio $A_v = v_L/v_s$, and (*c*) the input impedance Z_{in}.

Ans. (*a*) $A_i = -\dfrac{h_{fe}R_B R_L}{(R_C + R_L)[R_B + h_{ie} + (h_{fe} + 1)\lambda R_E]}$;

(*b*) $A_v = -\dfrac{h_{fe}R_C R_B R_L}{(R_C + R_L)\{R_S R_B + (R_S + R_B)[h_{ie} + (h_{fe} + 1)\lambda R_E]\}}$;

(*c*) $R_i = \dfrac{R_B[h_{ie} + (h_{fe} + 1)\lambda R_E]}{R_B + h_{ie} + (h_{fe} + 1)\lambda R_E}$

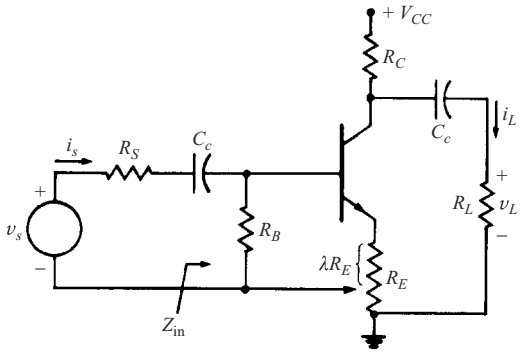


Fig. 6-31

6.42 For the CB amplifier of Problem 6.19, use SPICE methods to find (*a*) the input impedance Z_{in} and (*b*) the output impedance Z_o. (*Netlist code available at author website.*) *Ans.* (*a*) 24.81 Ω; (*b*) 2.195 kΩ

6.43 The exact small-signal equivalent circuit for the CC amplifier of Fig. 6-2(*a*) is given by Fig. 6-21. Find the Thévenin equivalent for the circuit to the right of terminals *b*, *b*, assume that $h_{re} = h_{oe} \approx 0$, and show that the circuit of Fig. 6-2(*c*) results. (*Hint*: The conversion from CE to CC *h* parameters was worked out in Problem 6.14.)

6.44 Apply the CC *h*-parameter model of Fig. 6-16 to the amplifier of Fig. 6-2(*a*) to find an expression for the voltage-gain ratio $A_v = v_E/v_i$. Evaluate A_v if $h_{ic} = 100\,\Omega$, $h_{rc} = 1$, $h_{fc} = -100$, $h_{oc} = 10^{-5}$ S, and $R_E = 1\,\text{k}\Omega$.
Ans. $A_v = -h_{fc}R_E/[h_{ic}(h_{oc}R_E + 1) - h_{rc}h_{fc}R_E] \approx 0.999$

6.45 Find an expression for R_o in the CC amplifier of Fig. 6-21; use the common approximations $h_{rc} \approx 1$ and $h_{oc} \approx 0$ to simplify the expression; and then evaluate it if $R_1 = 1\,\text{k}\Omega$, $R_2 = 10\,\text{k}\Omega$, $h_{fc} = -100$, and $h_{ic} = 100\,\Omega$. *Ans.* $R_o = h_{ic}/(h_{oc}h_{ic} - h_{fc}h_{rc}) \approx -h_{ic}/h_{fc} = 1\,\Omega$

6.46 The cascaded amplifier circuit of Fig. 6-24(*a*) matches a high-input-impedance CC first stage with a high-output-impedance CE second stage to produce an amplifier with high input and output impedances. To illustrate this claim, refer to Fig. 6-24(*b*) and determine values for (*a*) $Z_{\text{in}} = R_{\text{in}}$, (*b*) Z'_{in}, (*c*) Z_o, and (*d*) Z'_o if $R_S = 5\,\text{k}\Omega$ and all other circuit values are as given in Problem 6.24.
Ans. (*a*) 29.18 kΩ; (*b*) 818.2 Ω; (*c*) 5 kΩ; (*d*) 9.99 Ω

6.47 To illustrate the effect of signal-source internal impedance, calculate the voltage-gain ratio $A_v = v_L/v_s$ for the cascaded amplifier of Fig. 6-24(*a*) if $R_S = 20\,\text{k}\Omega$ and all other values are as given in Problem 6.24; then compare your result with the value of A_v found in Problem 6.24.
Ans. $A_v = -58.61$, which represents a reduction of approximately 40 percent

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6.48 For the amplifier of Fig. 6-32, find expressions for (*a*) the voltage-gain ratio $A_v = v_L/v_s$ and (*b*) the current-gain ratio $A_i = i_L/i_s$. Assume that $h_{re} = h_{oe} \approx 0$.

Ans. (*a*) $A_v = -h_{fe}R_C R_L/\{(R_C + R_L)[(h_{fe} + 1)R_E + h_{ie}]\}$; (*b*) $A_i = -h_{fe}R_C/(R_C + R_L)$

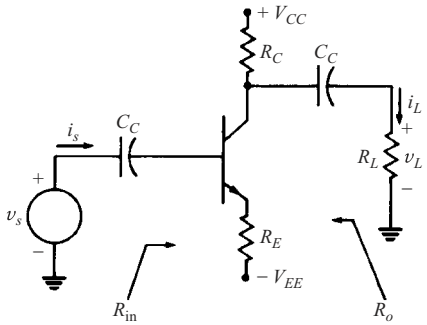


Fig. 6-32

6.49 Find expressions for (*a*) R_{in} and (*b*) R_o for the amplifier of Fig. 6-32 if $h_{re} = h_{oe} \approx 0$.

Ans. (*a*) $R_{in} = h_{ie} + (h_{fe} + 1)R_E$; (*b*) $R_o = R_C$

6.50 Suppose v_2 is replaced with a short circuit in the differential amplifier of Fig. 3-22. Find the input impedance R_{in1} looking into the terminal across which v_1 appears if $R_B = 20\,\text{k}\Omega$, $R_E = 1\,\text{k}\Omega$, $h_{ie} = 25\,\Omega$, $h_{fe} = 100$, and $h_{re} = h_{oe} \approx 0$. *Ans.* 9.11 kΩ

6.51 For the Darlington-pair emitter-follower of Fig. 6-33, $h_{re1} = h_{re2} = h_{oe1} = h_{oe2} = 0$. In terms of the (non-zero) h parameters, find expressions for (*a*) Z'_{in}; (*b*) the voltage gain $A_v \equiv v_E/v_s$; (*c*) the current gain $A_i \equiv i_{e2}/i_{in}$; (*d*) Z_{in}; and (*e*) Z_o (if the signal source has internal resistance R_S).

Ans. (*a*) $Z'_{in} = h_{ie1} + (h_{fe1} + 1)[h_{ie2} + (h_{fe2} + 1)R_E]$; (*b*) $A_v = \dfrac{(h_{fe1} + 1)(h_{fe2} + 1)R_E}{Z'_{in}}$;

(*c*) $A_i = \dfrac{(h_{fe} + 1)(h_{fe2} + 1)R_F}{R_F + Z'_{in}}$; (*d*) $Z_{in} = \dfrac{R_F Z'_{in}}{R_F + Z'_{in}}$;

(*e*) $Z_o = \dfrac{h_{ie2}}{h_{fe2} + 1} \dfrac{[R_S R_F/(R_S + R_F) + h_{ie1}]}{(h_{fe1} + 1)(h_{fe2} + 1)}$

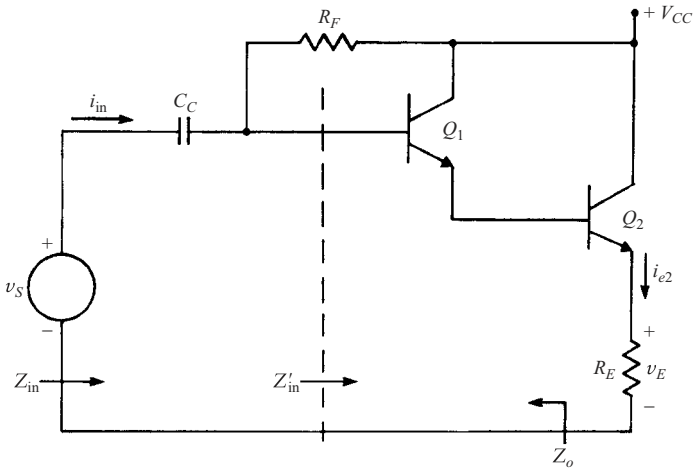


Fig. 6-33

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CHAPTER 7

Small-Signal Midfrequency FET and Triode Amplifiers

7.1. INTRODUCTION

Several two-port linear network models are available that allow accurate analysis of the FET for small drain-source voltage and small current excursions about a quiescent point (small-signal operation). In this chapter, all voltage and current signals are considered to be in the midfrequency range, where all capacitors appear as short circuits (see Section 4.6).

There are three basic FET amplifier configurations: the *common-source* (CS), *common-drain* (CD) or *source-follower* (SF), and *common-gate* (CG) configurations. The CS amplifier, which provides good voltage amplification, is most frequently used. The CD and CG amplifiers are applied as buffer amplifiers (with high input impedance and near-unity voltage gain) and high-frequency amplifiers, respectively.

7.2. SMALL-SIGNAL EQUIVALENT CIRCUITS FOR THE FET

From the FET drain characteristics of Fig. 4-2(*a*), it is seen that if i_D is taken as the dependent variable, then

$$i_D = f(v_{GS}, v_{DS}) \tag{7.1}$$

For small excursions (ac signals) about the Q point, $\Delta i_D = i_d$; thus, application of the chain rule to (7.1) leads to

$$i_d = \Delta i_D \approx di_D = g_m v_{gs} + \frac{1}{r_{ds}} v_{ds} \tag{7.2}$$

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where g_m and r_{ds} are defined as follows:

$$\textit{Transconductance} \quad g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q \approx \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_Q \tag{7.3}$$

$$\textit{Source-drain resistance} \quad r_{ds} \equiv \left.\frac{\partial v_{DS}}{\partial i_D}\right|_Q \approx \left.\frac{\Delta v_{DS}}{\Delta i_D}\right|_Q \tag{7.4}$$

As long as the JFET is operated in the pinchoff region, $i_G = i_g = 0$, so that the gate acts as an open circuit. This, along with (7.2), leads to the current-souce equivalent circuit of Fig. 7-1(*a*). The voltage-source model of Fig. 7-1(*b*) is derived in Problem 7.2. Either of these models may be used in analyzing an amplifier, but one may be more efficient than the other in a particular circuit.

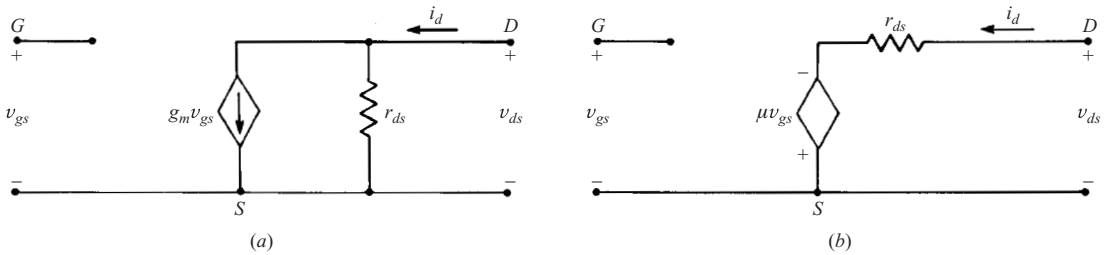


Fig. 7-1 Small-signal models for the CS FET

7.3. CS AMPLIFIER ANALYSIS

A simple common-source amplifier is shown in Fig. 7-2(*a*); its associated small-signal equivalent circuit, incorporating the voltage-source model of Fig. 7-1(*b*), is displayed in Fig. 7-2(*b*). Source resistor R_s is used to set the Q point but is bypassed by C_s for midfrequency operation.

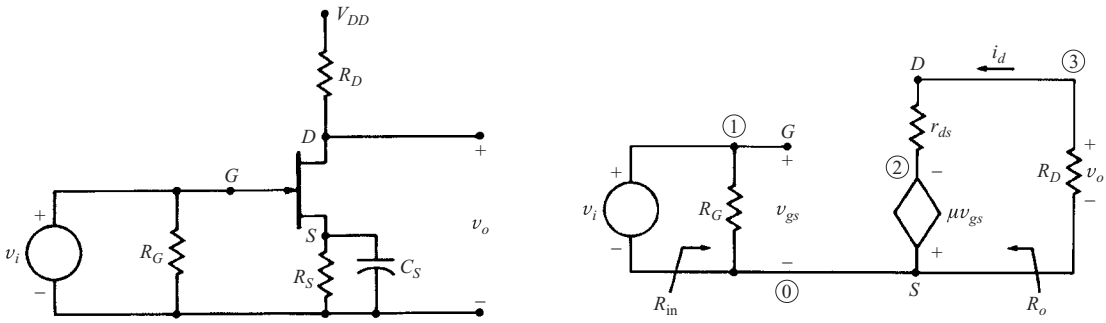


Fig. 7-2

Example 7.1. In the CS amplifier of Fig. 7-2(*b*), let $R_D = 3\,\text{k}\Omega$, $\mu = 60$, and $r_{ds} = 30\,\text{k}\Omega$. (*a*) Find an expression for the voltage-gain ratio $A_v = v_o/v_i$. (*b*) Evaluate A_v using the given typical values.

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(*a*) By voltage division,

$$v_o = -\frac{R_D}{R_D + r_{ds}}\,\mu v_{gs}$$

Substitution of $v_{gs} = v_i$ and rearrangement give

$$A_v = \frac{v_o}{v_i} = -\frac{\mu R_D}{R_D + r_{ds}} \tag{7.5}$$

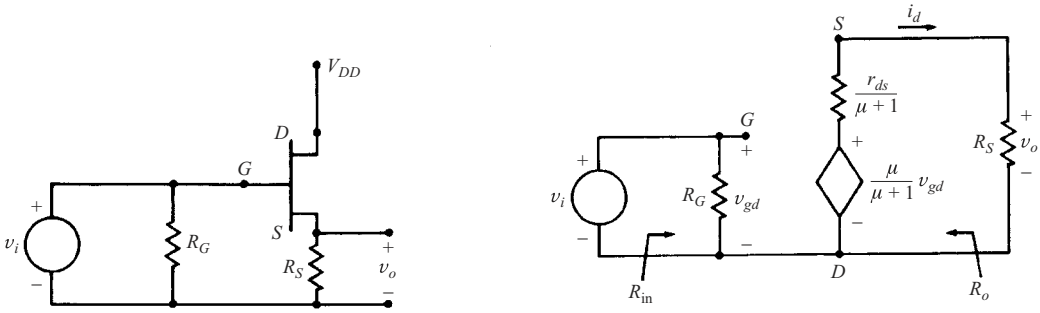
(*b*) The given values lead to

$$A_v = -\frac{(60)(3 \times 10^3)}{3 \times 10^3 + 30 \times 10^3} = -5.45$$

where the minus sign indicates a 180° phase shift between v_i and v_o.

7.4. CD AMPLIFIER ANALYSIS

A simple common-drain (or source-follower) amplifier is shown in Fig. 7-3(*a*); its associated small-signal equivalent circuit is given in Fig. 7-3(*b*), where the voltage-source equivalent of Fig. 7-1(*b*) is used to model the FET.



(*a*) CD or SF amplifier

(*b*) Small-signal equivalent circuit

Fig. 7-3

Example 7.2. In the CD amplifier of Fig. 7-3(*b*), let $R_S = 5\,\text{k}\Omega$, $\mu = 60$, and $r_{ds} = 30\,\text{k}\Omega$. (*a*) Find an expression for the voltage-gain ratio $A_v = v_o/v_i$. (*b*) Evaluate A_v using the given typical values.

(*a*) By voltage division,

$$v_o = \frac{R_S}{R_S + r_{ds}/(\mu+1)}\,\frac{\mu}{\mu+1}\,v_{gd} = \frac{\mu R_S v_{gd}}{(\mu+1)R_S + r_{ds}}$$

Replacement of v_{gd} by v_i and rearrangement give

$$A_v = \frac{v_o}{v_i} = \frac{\mu R_S}{(\mu+1)R_S + r_{ds}} \tag{7.6}$$

(*b*) Substitution of the given values leads to

$$A_v = \frac{(60)(5 \times 10^3)}{(61)(5 \times 10^3) + (30 \times 10^3)} = 0.895$$

Note that the gain is less than unity; its positive value indicates that v_o and v_i are in phase.

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7.5. CG AMPLIFIER ANALYSIS

Figure 4-28 is a simple common-gate amplifier circuit. Its small-signal equivalent circuit, incorporating the current-source model of Fig. 7-1(*a*), is given in Fig. 7-4.

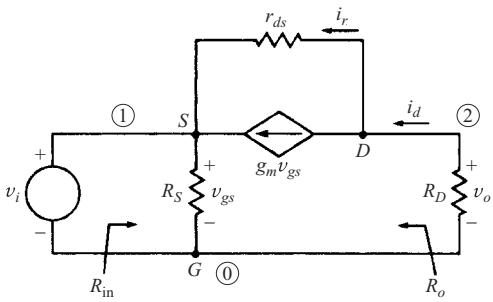


Fig. 7-4 CG small-signal equivalent circuit

Example 7.3. In the CG amplifier of Fig. 7-4, let $R_D = 1\,\text{k}\Omega$, $g_m = 2 \times 10^{-3}\,\text{S}$, and $r_{ds} = 30\,\text{k}\Omega$. (*a*) Find an expression for the voltage-gain ratio $A_v = v_o/v_i$. (*b*) Evaluate A_v using the given typical values.

(*a*) By KCL, $i_r = i_d - g_m v_{gs}$. Applying KVL around the outer loop gives

$$v_o = (i_d - g_m v_{gs}) r_{ds} - v_{gs}$$

But $v_{gs} = -v_i$ and $i_d = -v_o/R_D$; thus,

$$v_o = \left(-\frac{v_o}{R_D} + g_m v_i\right) r_{ds} + v_i$$

and

$$A_v = \frac{v_o}{v_i} = \frac{(g_m r_{ds} + 1) R_D}{R_D + r_{ds}} \tag{7.7}$$

(*b*) Substitution of the given values yields

$$A_v = \frac{(61)(1 \times 10^3)}{1 \times 10^3 + 30 \times 10^3} = 1.97$$

7.6. FET AMPLIFIER GAIN CALCULATION WITH SPICE

SPICE models of the JFET and MOSFET (introduced in Chapter 4) provide the terminal characteristic of the devices; thus, an amplifier can be properly biased and a time-varying input signal directly applied to the completely modeled amplifier circuit. Such a simulation is the analytical equivalent of laboratory amplifier circuit operation. Any desired signal can be measured directly in the time domain to form signal ratios that yield current and voltage gains. Any signal distortion that may result from device nonlinearity is readily apparent from inspection of the signal time plots.

Example 7.4. For the JFET amplifier of Fig. 7-5, $V_{DD} = 15\,\text{V}$, $R_1 = 100\,\text{k}\Omega$, $R_2 = 600\,\text{k}\Omega$, $R_D = 5\,\text{k}\Omega$, $R_S = 2.5\,\text{k}\Omega$, $R_L = 3\,\text{k}\Omega$, and $C_{C1} = C_{C2} = C_S = 100\,\mu\text{F}$. The *n*-channel JFET has the parameter values of Example 4-1. If $v_S = 0.25\sin(2\pi \times 10^4 t)\,\text{V}$ and r_i is negligible, use SPICE methods to determine the voltage gain of the amplifier circuit.

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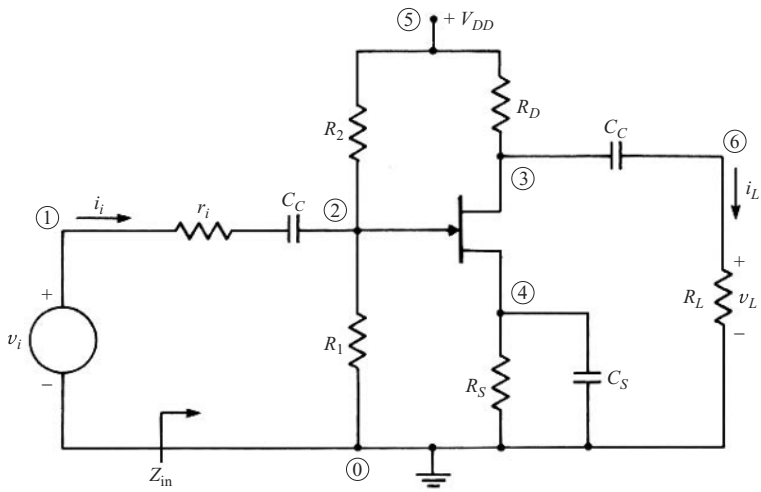


Fig. 7-5

The following netlist code describes the circuit:

```
Ex7_4.CIR
vs  1 0 SIN(0V 0.25V 10kHz)
VDD 5 0 DC 15V
CC1 1 2 100uf
CC2 3 6 100uF
CS  4 0 100uF
R1  2 0 100kohm
R2  5 2 600kohm
RD  5 3 5kohm
RS  4 0 2.5kohm
RL  6 0 3kohm
J 3 2 4 NJFET
.MODEL NJFET NJF(Vto=-4V Beta=0.005ApVsq
+ Rd=1ohm Rs=1ohm CGS=2pF CGD=2pF)
.TRAN 1us 0.1ms
.PROBE
.END
```

Execute ⟨Ex7_4.CIR⟩ and use the Probe and FFT features of PSpice to plot the input voltage v_i and output voltage v_L waveforms and their Fourier spectra as displayed by Fig. 7-6. The voltage gain is found as the ratio of the marked spectra fundamental components of Fig. 7-6.

$$A_v = \frac{v_L}{v_S} = -\frac{0.748}{0.250} = -2.99$$

The negative sign indicates the 180° phase difference between v_i and v_L as noted by inspection of the instantaneous waveforms.

The capabilities of SPICE are also suited to FET amplifier analysis using the small-signal equivalent circuit of the types shown by Figs. 7-1 through 7-4. Use of the voltage-controlled voltage source (VCVS) and the voltage-controlled current source (VCCS) of Section 1.3 finds obvious application in the small-signal equivalent circuit analysis.

Example 7.5. Rework Example 7.1 using SPICE methods. For purposes of computation, let $v_i = 0.25\sin(2\pi \times 10^4 t)$ V.

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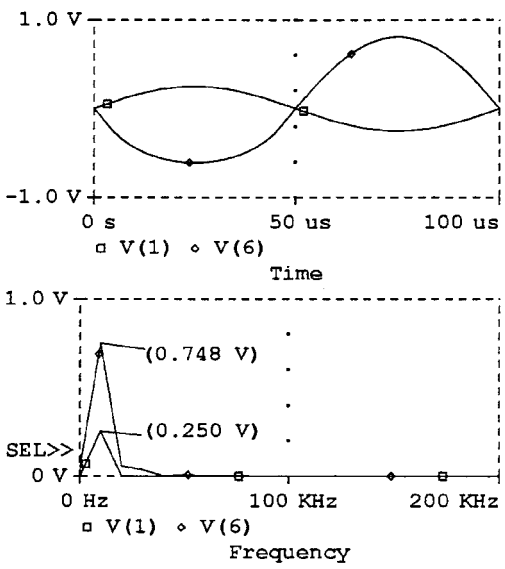


Fig. 7-6

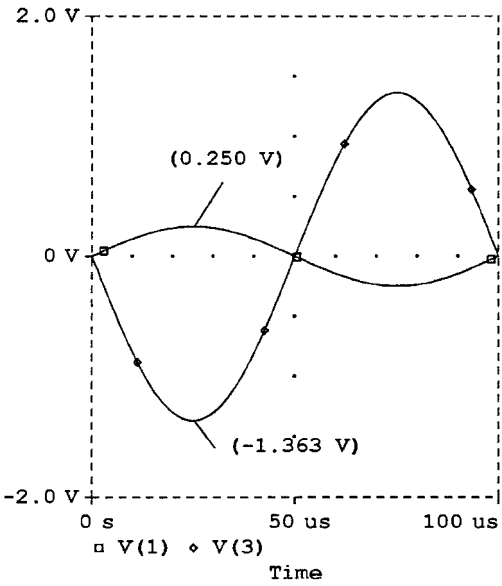


Fig. 7-7

The following netlist code describes the circuit:

```
Ex7_5.CIR
vi  1 0 SIN(0V 0.25V 10kHz)
RG  1 0 100kohm
E   0 2 (1,0) 60
rds 2 3 30kohm
RD  3 0 3kohm
.TRAN 1us 0.1ms
.PROBE
.END
```

Execute ⟨Ex7_5.CIR⟩ and use the Probe feature of PSpice to plot the instantaneous waveforms of v_i and v_o as shown in Fig. 7-7. The gain is found as the ratio of the marked peak values with the 180° phase shift accounted for by the negative sign.

$$A_v = \frac{v_o}{v_i} = -\frac{1.363}{0.250} = -5.45$$

7.7. GRAPHICAL AND EQUIVALENT CIRCUIT ANALYSIS OF TRIODE AMPLIFIERS

The application of a time-varying signal v_S to the triode amplifier circuit of Fig. 4-14 results in a grid voltage with a time-varying component,

$$v_G = V_{GQ} + v_g$$

It is usual practice to ensure that $v_G \leq 0$ by proper selection of the combination of bias and signal. Then $i_G = 0$, and the operating point must move along the dc load line from the Q point in accordance with the variation of v_g, giving instantaneous values of v_P and i_P that simultaneously satisfy (*4.8*) and (*4.11*).

Example 7.6. The triode amplifier of Fig. 4-14 has V_{GG}, V_{PP}, R_G, and R_L, as given in Example 4.7. If the plate characteristics of the triode are given by Fig. 7-8 and $v_S = 2\sin\omega t$ V, graphically find v_P and i_P.

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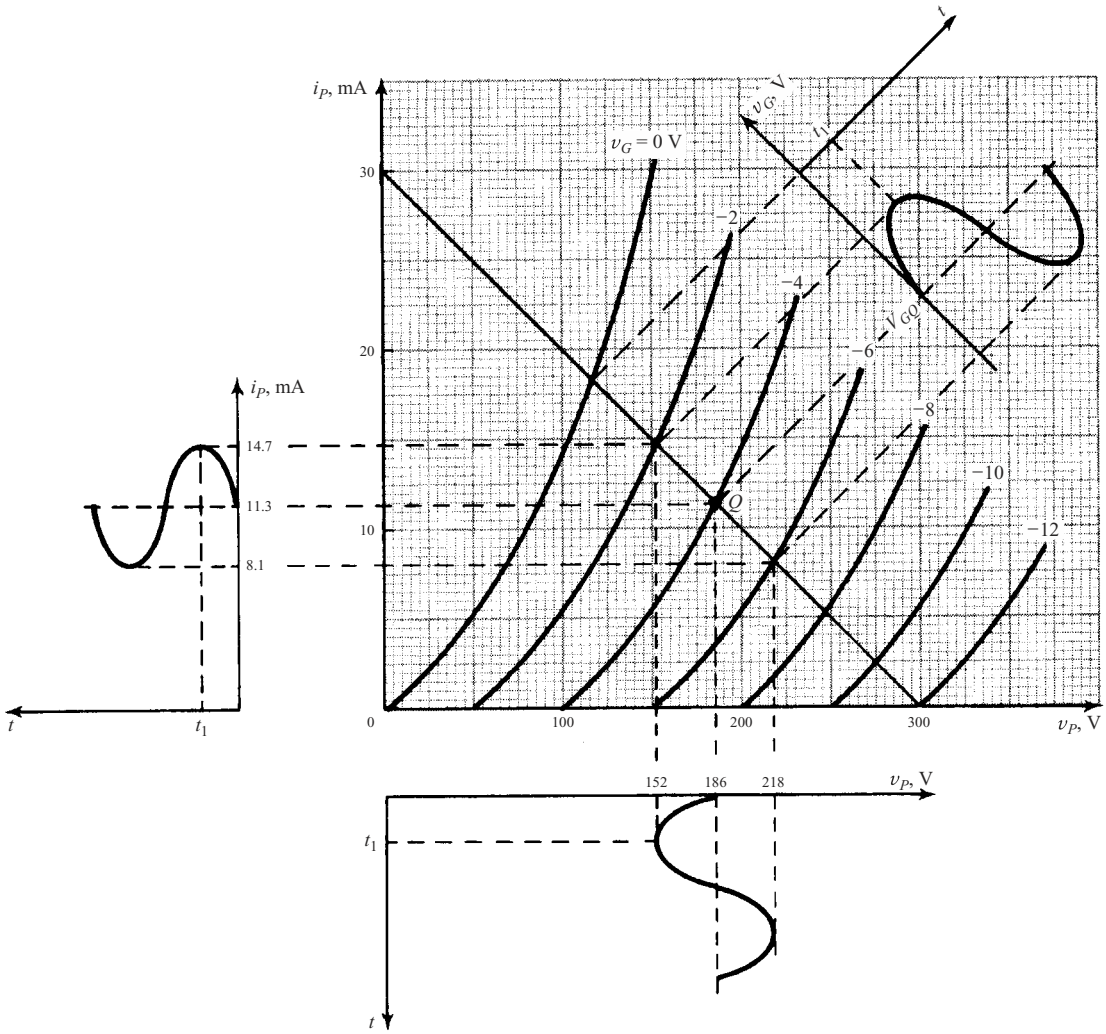


Fig. 7-8

The dc load line, with the same intercepts as in Example 4.7, is superimposed on the characteristics of Fig. 7-8; however, because the plate characteristics are different from those of Example 4.7, the quiescent values are now $I_{PQ} = 11.3\,\text{mA}$ and $V_{PQ} = 186\,\text{V}$. Then a time axis on which to plot $v_G = -4 + 2\sin\omega t\,\text{V}$ is constructed perpendicular to the dc load line at the Q point. Time axes for i_P and v_P are also constructed as shown, and values of i_P and v_P corresponding to particular values of $v_G(t)$ are found by projecting through the dc load line, for one cycle of v_G. The result, in Fig. 7-8, shows that v_P varies from 152 to 218 V and i_P ranges from 8.1 to 14.7 mA.

The following treatment echoes that of Section 6.2 For the usual case of negligible grid current, (*4.7*) degenerates to $i_G = 0$ and the grid acts as an open circuit. For small excursions (ac signals) about the Q point, $\Delta i_P = i_p$ and an application of the chain rule to (*4.8*) leads to

$$i_p = \Delta i_P \approx di_P = \frac{1}{r_p} v_p + g_m v_g \tag{7.8}$$

where we have defined

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$$\textit{Plate resistance} \quad r_p \equiv \left.\frac{\partial v_P}{\partial i_P}\right|_Q \simeq \left.\frac{\Delta v_P}{\Delta i_P}\right|_Q \tag{7.9}$$

$$\textit{Transconductance} \quad g_m \equiv \left.\frac{\partial i_P}{\partial v_G}\right|_Q \simeq \left.\frac{\Delta i_P}{\Delta v_G}\right|_Q \tag{7.10}$$

Under the condition $i_G = 0$, (7.8) is simulated by the current-source equivalent circuit of Fig 7-9(*a*). The frequently used voltage-source model of Fig. 7-9(*b*) is developed in Problem 7.19.

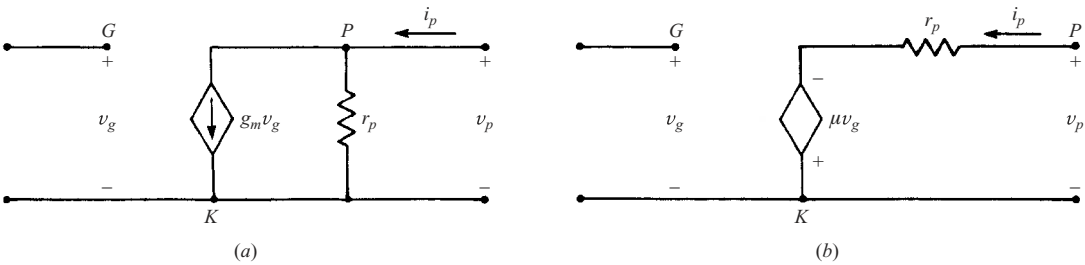


Fig. 7-9 Triode small-signal equivalent circuits

Solved Problems

7.1 (*a*) For the JFET amplifier of Example 4.2, use the drain characteristics of Fig. 4-6 to determine the small-signal equivalent-circuit constants g_m and r_{ds}. (*b*) Alternatively, evaluate g_m from the transfer characteristic.

(*a*) Let v_{gs} change by ± 1 V about the Q point of Fig. 4-6(*b*); then, by (7.3),

$$g_m \approx \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_Q = \frac{(3.3 - 0.3) \times 10^{-3}}{2} = 1.5\,\text{mS}$$

At the Q point of Fig. 4-6(*b*), while v_{DS} changes from 5 V to 20 V, i_D changes from 1.4 mA to 1.6 mA; thus, by (7.4),

$$r_{ds} \approx \left.\frac{\Delta v_{DS}}{\Delta i_D}\right|_Q = \frac{20 - 5}{(1.6 - 1.4) \times 10^{-3}} = 75\,\text{k}\Omega$$

(*b*) At the Q point of Fig. 4-6(*a*), while i_D changes from 1 mA to 2 mA, v_{GS} changes from -2.4 V to -1.75 V; by (7.3),

$$g_m \approx \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_Q = \frac{(2 - 1) \times 10^{-3}}{-1.75 - (-2.4)} = 1.54\,\text{mS}$$

7.2 Derive the small-signal voltage-source model of Fig. 7-1(*b*) from the current source model of Fig. 7-1(*a*).

We find the Thévenin equivalent for the network to the left of the output terminals of Fig.7-1(*a*). If all independent sources are deactivated, $v_{gs} = 0$; thus, $g_m v_{gs} = 0$, so that the dependent source also is deactivated (open circuit for a current source), and the Thévenin resistance is $R_{Th} = r_{ds}$. The open-circuit voltage

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appearing at the output terminals is $v_{Th} = v_{ds} = -g_m v_{gs} r_{ds} = -\mu v_{gs}$, where we have defined a new equivalent-circuit constant,

$$\textit{Amplification factor} \qquad \mu \equiv g_m r_{ds}$$

Proper series arrangement of v_{Th} and R_{Th} leads to Fig. 7-1(b).

7.3 In the drain-feedback-biased amplifier of Fig. 4-9(a), $R_F = 5\,\text{M}\Omega$, $R_L = 14\,\text{k}\Omega$, $r_{ds} = 40\,\text{k}\Omega$, and $g_m = 1\,\text{mS}$. Find (a) $A_v = v_{ds}/v_i$, (b) Z_{in}, (c) Z_o looking back through the drain-source terminals, and (d) $A_i = i_i/i_L$.

(a) The voltage-source small-signal equivalent circuit is given in Fig. 7-10. With v_{ds} as a node voltage,

$$\frac{v_i - v_{ds}}{R_F} = \frac{v_{ds}}{R_L} + \frac{v_{ds} + \mu v_i}{r_{ds}}$$

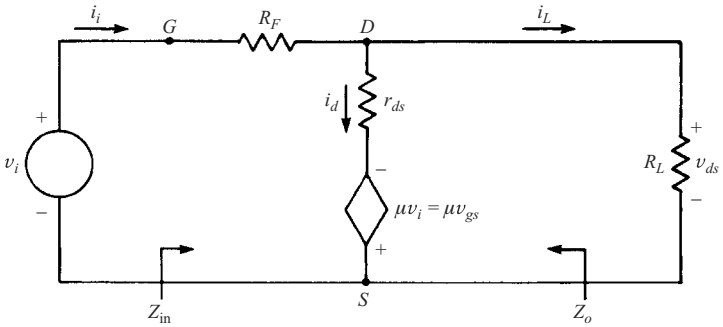


Fig. 7-10

Substituting for $\mu = g_m r_{ds}$ and rearranging yield

$$A_v = \frac{v_{ds}}{v_i} = \frac{R_L r_{ds}(1 - R_F g_m)}{R_F r_{ds} + R_L r_{ds} + R_L R_F}$$

$$= \frac{(14 \times 10^3)(40 \times 10^3)[1 - (5 \times 10^6)(1 \times 10^{-3})]}{(5 \times 10^6)(40 \times 10^3) + (14 \times 10^3)(40 \times 10^3) + (14 \times 10^3)(5 \times 10^6)} = -10.35$$

(b) KVL around the outer loop of Fig. 7-10 gives $v_i = i_i R_F + v_{ds} = i_i R_F + A_v v_i$, from which

$$Z_{\text{in}} = \frac{v_i}{i_i} = \frac{R_F}{1 - A_v} = \frac{5 \times 10^6}{1 - (-10.35)} = 440\,\text{k}\Omega$$

(c) The driving-point impedance Z_o is found after deactivating the independent source v_i. With $v_i = 0$, $\mu v_{gs} = \mu v_i = 0$ and

$$Z_o = \frac{r_{ds} R_F}{r_{ds} + R_F} = \frac{(40 \times 10^3)(5000 \times 10^3)}{5040 \times 10^3} = 39.68\,\text{k}\Omega$$

(d) $$A_i = \frac{i_L}{i_i} = \frac{v_{ds}/R_L}{v_i/Z_{\text{in}}} = \frac{A_v Z_{\text{in}}}{R_L} = \frac{(-10.35)(440 \times 10^3)}{14 \times 10^3} = -325.3$$

7.4 For the JFET amplifier of Fig. 7-5, $g_m = 2\,\text{mS}$, $r_{ds} = 30\,\text{k}\Omega$, $R_S = 3\,\text{k}\Omega$, $R_D = R_L = 2\,\text{k}\Omega$, $R_1 = 200\,\text{k}\Omega$, $R_2 = 800\,\text{k}\Omega$, and $r_i = 5\,\text{k}\Omega$. If C_C and C_S are large and the amplifier is biased in the pinchoff region, find (a) Z_{in}, (b) $A_v = v_L/v_i$, and (c) $A_i = i_L/i_i$.

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(*a*) The current-source small-signal equivalent circuit is drawn in Fig. 7-11. Since the gate draws negligible current,

$$Z_{\text{in}} = R_G = \frac{R_1 R_2}{R_1 + R_2} = \frac{(200 \times 10^3)(800 \times 10^3)}{1000 \times 10^3} = 160\,\text{k}\Omega$$

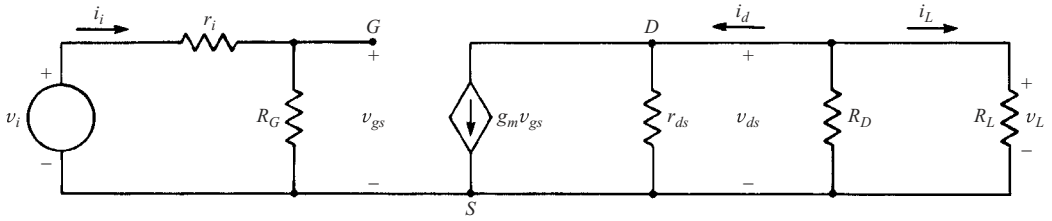


Fig. 7-11

(*b*) By voltage division at the input loop,

$$v_{gs} = \frac{R_G}{R_G + r_1} v_i = \frac{160 \times 10^3}{165 \times 10^3} v_i = 0.97 v_i \qquad (1)$$

The dependent current source drives into R_{ep}, where

$$\frac{1}{R_{ep}} = \frac{1}{r_{ds}} + \frac{1}{R_D} + \frac{1}{R_L} = \frac{1}{30 \times 10^3} + \frac{1}{2 \times 10^3} + \frac{1}{2 \times 10^3} = \frac{1}{967.74}\ S$$

and so

$$v_L = -g_m v_{gs} R_{ep} \qquad (2)$$

Eliminating v_{gs} between (*1*) and (*2*) yields

$$A_v = \frac{v_L}{v_i} = 0.97(-g_m R_{ep}) = -(0.97)(2 \times 10^{-3})(967.74) = -1.88$$

(*c*)
$$A_i = \frac{i_L}{i_i} = \frac{v_L / R_L}{v_i (R_G + r_i)} = \frac{A_v (R_G + r_i)}{R_L} = \frac{(-1.88)(165 \times 10^3)}{2 \times 10^3} = -155.1$$

7.5 Show that a small-signal equivalent circuit for the common-drain FET amplifier of Fig. 4-15 is given by Fig. 7-12(*b*).

The voltage-source model of Fig. 7-1(*b*) has been inserted in the ac equivalent of Fig. 4-15, and the result redrawn to give the circuit of Fig. 7-12(*a*), where R_G is determined as in Problem 4.6. Voltage v_{gd}, which is

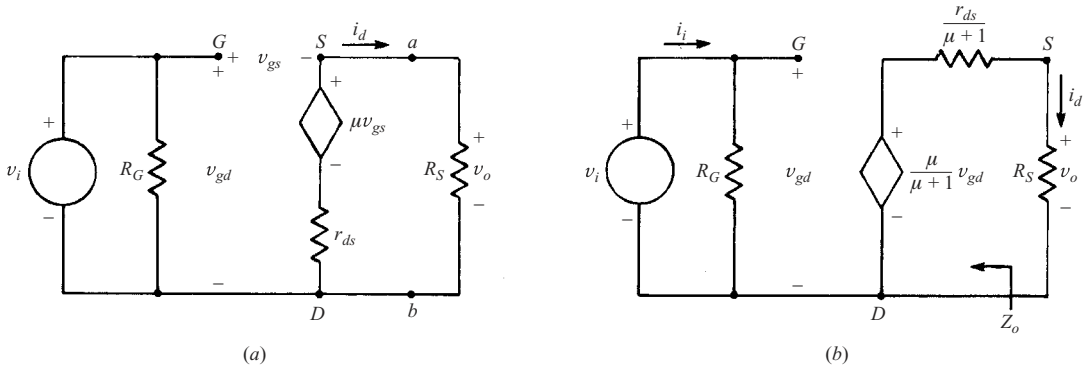


Fig. 7-12

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more easily determined than v_{gs}, has been labeled. With terminals a, b opened in Fig. 7-12(a), KVL around the S, G, D loop yields

$$v_{gs} = \frac{v_{gd}}{\mu + 1}$$

Then the Thévenin voltage at the open-circuited terminals a, b is

$$v_{Th} = \mu v_{gs} = \frac{\mu}{\mu + 1} v_{gd} \tag{1}$$

The Thévenin impedance is found as the driving-point impedance to the left through a, b (with v_i deactivated or shorted), as seen by a source v_{ab} driving current i_a into terminal a. Since $v_{gs} = -v_{ab}$, KVL around the output loop of Fig. 7-12(a) gives

$$v_{ab} = \mu v_{gs} + i_a r_{ds} = -\mu v_{ab} + i_a r_{ds}$$

from which

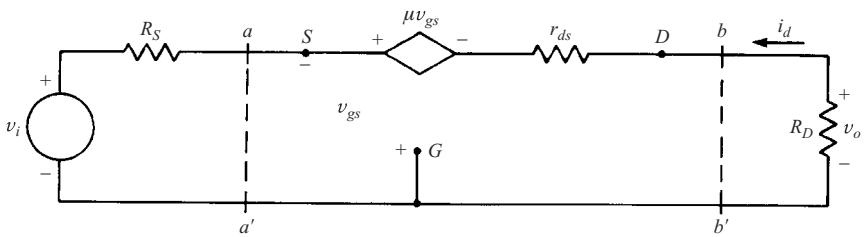
$$R_{Th} = \frac{v_{ab}}{i_a} = \frac{r_{ds}}{\mu + 1} \tag{2}$$

Expressions (*1*) and (*2*) lead directly to the circuit of Fig. 7-12(b).

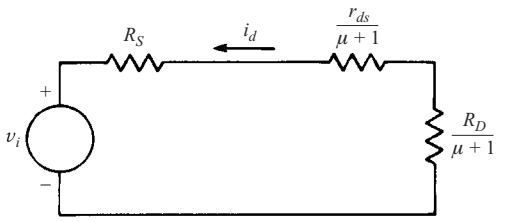
7.6 Figure 7-13(a) is a small-signal equivalent circuit (voltage-source model) of a common-gate JFET amplifier. Use the circuit to verify two *rules of impedance and voltage reflection* for FET amplifiers:

(a) Voltages and impedances in the drain circuit are reflected to the source circuit divided by $\mu + 1$. [Verify this rule by finding the Thévenin equivalent for the circuit to the right of a, a' in Fig. 7-13(a) and showing that Fig. 7-13(b) results.]

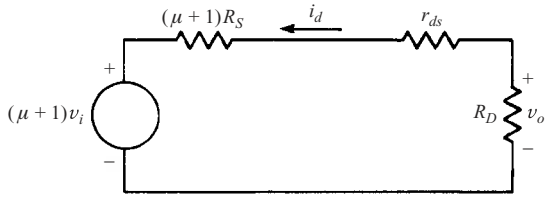
(b) Voltages and impedances in the source circuit are reflected to the drain circuit multiplied by $\mu + 1$. [Verify this rule by finding the Thévenin equivalent for the circuit to the left of b, b' in Fig. 7-13(a) and showing that Fig. 7-13(c) results.]



(a)



(b)



(c)

Fig. 7-13

(a) With a, a' open, $i_d = 0$; hence, $v_{gs} = 0$ and $v_{Th} = 0$. After a driving-point source $v_{aa'}$ is connected to terminals a, a' to drive current i_a into terminal a, KVL gives

$$v_{aa'} = \mu v_{gs} + i_a(r_{ds} + R_D) \tag{1}$$

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But $v_{gs} = -v_{aa'}$, which can be substituted into (*1*) to give

$$R_{Th} = \frac{v_{aa'}}{i_a} = \frac{r_{ds}}{\mu + 1} + \frac{R_D}{\mu + 1} \tag{2}$$

With $v_{Th} = 0$, insertion of R_{Th} in place of the network to the right of a, a' in Fig. 7-13(*a*) leads directly to Fig. 7-13(*b*).

(*b*) Applying KVL to the left of b, b' in Fig. 7-13(*a*) with b, b' open, while noting that $v_i = -v_{gs}$, yields

$$v_{Th} = v_i - \mu v_{gs} = (\mu + 1)v_i \tag{3}$$

Deactivating (shorting) v_i, connecting a driving-point source $v_{bb'}$ to terminals b, b' to drive current i_b into terminal b, noting that $v_{gs} = -i_b R_S$, and applying KVL around the outer loop of Fig. 7-13(*a*) yield

$$v_{bb'} = i_b(r_{ds} + R_S) - \mu v_{gs} = i_b[r_{ds} + (\mu + 1)R_S] \tag{4}$$

The Thévenin impedance follows from (*4*) as

$$R_{Th} = \frac{v_{bb'}}{i_b} = r_{ds} + (\mu + 1)R_S \tag{5}$$

When the Thévenin source of (*3*) and impedance of (*5*) are used to replace the network to the left of b, b', the circuit of Fig. 7-13(*c*) results.

7.7 Suppose capacitor C_S is removed from the circuit of Problem 7.4 (Fig. 7-5), and all else remains unchanged. Find (*a*) the voltage-gain ratio $A_v = v_L/v_i$, (*b*) the current-gain ratio $A_i = i_L/i_i$, and (*c*) the output impedance R_o looking to the left through the output port with R_L removed.

(*a*) The voltage-source small-signal equivalent circuit is given in Fig. 7-14 (the current-source model was utilized in Problem 7.4). Voltage division and KVL give

$$v_{gs} = \frac{R_G}{R_G + r_i} v_i - i_d R_S \tag{1}$$

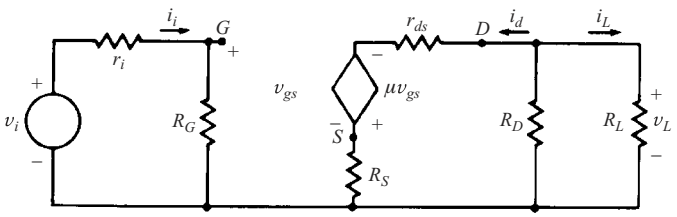


Fig. 7-14

But by Ohm's law,

$$i_d = \frac{\mu v_{gs}}{r_{ds} + R_S + R_D \| R_L} \tag{2}$$

Substituting (*2*) into (*1*) and solving for v_{gs} yield

$$v_{gs} = \frac{R_G(r_{ds} + R_S + R_D \| R_L)v_i}{(R_G + r_i)[r_{ds} + (\mu + 1)R_S + R_D \| R_L]} \tag{3}$$

Now voltage division gives

$$v_L = -\frac{R_D \| R_L}{r_{ds} + R_S + R_D \| R_L} \mu v_{gs} \tag{4}$$

and substitution of (*3*) into (*4*) and rearrangement give

$$A_v = \frac{v_L}{v_i} = \frac{-\mu R_G R_D R_L}{(R_G + r_i)\{(R_D + R_L)[r_{ds} + (\mu + 1)R_S] + R_D R_L\}} \tag{5}$$

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With $\mu = g_m r_{ds}$ and the given values, (5) becomes

$$A_v = \frac{-(2 \times 10^{-3})(30 \times 10^3)(160)(2)(2)}{(160+5)\{(2+2)[30+(60+1)3]+(2)(2)\}} = -0.272$$

(*b*) The current gain is found as

$$A_i = \frac{i_L}{i_i} = \frac{v_L/R_L}{v_i/(R_G+r_i)} = \frac{A_v(R_G+r_i)}{R_L} = \frac{(-0.272)(160+5)}{2} = -22.4$$

(*c*) R_L is disconnected, and a driving-point source is added such that $v_{dp} = v_L$. With v_i deactivated (short-circuited), $v_{gs} = 0$ and

$$R_o = R_D \| (r_{ds} + R_S) = \frac{R_D(r_{ds}+R_S)}{R_D + r_{ds} + R_S} = \frac{(2 \times 10^3)(30 \times 10^3 + 3 \times 10^3)}{2 \times 10^3 + 30 \times 10^3 + 3 \times 10^3} = 1.89\,\text{k}\Omega$$

Note that when R_S is not bypassed, the voltage- and current-gain ratios are significantly reduced.

7.8 Use SPICE methods to determine the voltage gain for the CG amplifier of Example 7.3. Let $R_S = 2\,\text{k}\Omega$ and $v_i = 0.25\sin(2\pi \times 10^3 t)\,\text{V}$ for computational purposes.

The netlist code that follows describes the circuit:

```
Prb7_8.CIR
vi  1 0 SIN(0V 0.25V 1kHz)
RS  1 0 2kohm
RD  2 0 1kohm
rds 1 2 30kohm
G   1 2 (1,0) 2e-3
.TRAN 1us 1ms
.PROBE
.END
```

Execute ⟨Prb7_8.CIR⟩ and use the Probe feature of PSpice to give the resulting waveforms for v_i and v_o shown by Fig. 7-15. The voltage gain is found as the ratio of the marked peak values.

$$A_v = \frac{v_i}{v_o} = \frac{0.492}{0.250} = 1.97$$

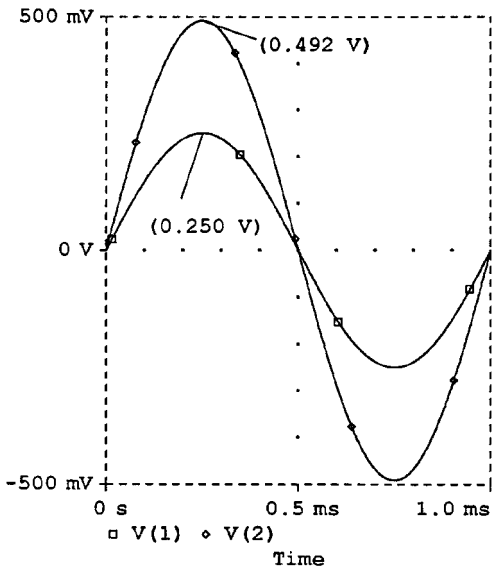


Fig. 7-15

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7.9 Find a small-signal equivalent circuit for the two parallel-connected JFETs of Fig. 7-16 if the devices are not identical.

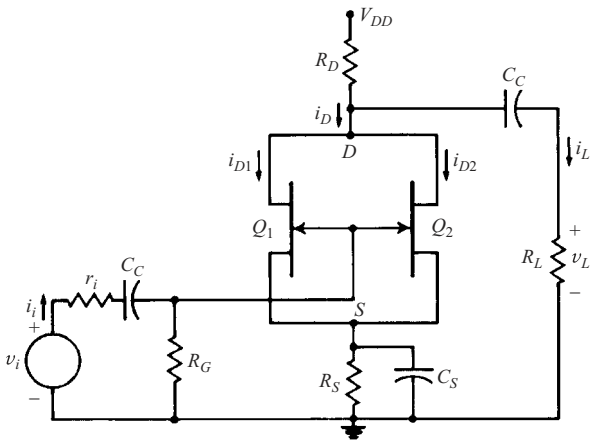


Fig. 7-16

By KCL,

$$i_D = i_{D1} + i_{D2} \tag{1}$$

Since the parallel connection assures that the gate-source and drain-source voltages are the same for both devices, (*1*) can be written as

$$i_D = f_1(v_{GS}, v_{DS}) + f_2(v_{GS}, v_{DS}) \tag{2}$$

Application of the chain rule to (*2*) yields

$$i_d = \Delta i_D \approx di_D = (g_{m1} + g_{m2})v_{gs} + \left(\frac{1}{r_{ds1}} + \frac{1}{r_{ds2}}\right)v_{ds} \tag{3}$$

where $g_{m1} = \left.\dfrac{\partial i_{D1}}{\partial v_{GS}}\right|_Q$ $g_{m2} = \left.\dfrac{\partial i_{D2}}{\partial v_{GS}}\right|_Q$ $r_{ds1} = \left.\dfrac{\partial v_{DS}}{\partial i_{D1}}\right|_Q$ $r_{ds2} = \left.\dfrac{\partial v_{DS}}{\partial i_{D2}}\right|_Q$

Equation (*3*) is satisfied by the current-source circuit of Fig. 7-1(*a*) if $g_m = g_{m1} + g_{m2}$ and $r_{ds} = r_{ds1} \| r_{ds2}$.

7.10 In the circuit of Fig. 7-16, $R_S = 3\,\text{k}\Omega$, $R_D = R_L = 2\,\text{k}\Omega$, $r_i = 5\,\text{k}\Omega$, and $R_G = 100\,\text{k}\Omega$. Assume that the two JFETs are identical with $r_{ds} = 25\,\text{k}\Omega$ and $g_m = 0.0025\,\text{S}$. Find (*a*) the voltage-gain ratio $A_v = v_L/v_i$, (*b*) the current-gain ratio $A_i = i_L/i_i$, and (*c*) the output impedance R_o.

(*a*) The small-signal equivalent circuit is given in Fig. 7-17, which includes the model for two parallel JFETs as determined in Problem 7.9. By voltage division,

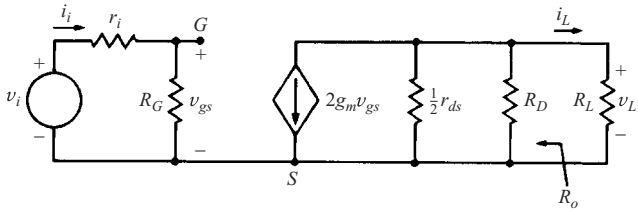


Fig. 7-17

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$$v_{gs} = \frac{R_G}{R_G + r_i} v_i = \frac{100}{100 + 5} v_i = 0.952 v_i \tag{1}$$

Now let

$$R_{eq} = \tfrac{1}{2} r_{ds} \| R_D \| R_L = \frac{r_{ds} R_D R_L}{2R_L R_D + r_{ds}(R_L + R_D)} = \frac{(25)(2)(2) \times 10^3}{(2)(2)(2) + (25)(2 + 2)} = 962\,\Omega \tag{2}$$

Then, by Ohm's law, $v_L = -2 g_m v_{gs} R_{eq}$; with (*1*) and (*2*), this gives

$$A_v = \frac{v_L}{v_i} = -2 g_m \frac{R_G}{R_G + r_i} R_{eq} = -2(0.0025)(0.952)(962) = -4.58$$

(*b*) The current-gain ratio is

$$A_i = \frac{i_L}{i_i} = \frac{v_L / R_L}{v_i / (R_G + r_i)} = \frac{A_v (R_G + r_i)}{R_L} = \frac{(-4.58)(100 + 5)}{2} = -240.4$$

(*c*) We replace R_L with a driving-point source oriented such that $v_{dp} = v_L$. With v_i deactivated (short-circuited), $v_{gs} = 0$; thus,

$$R_o = R_D \| (\tfrac{1}{2} r_{ds}) = \frac{R_D r_{ds}}{2R_D + r_{ds}} = \frac{(2)(25) \times 10^3}{(2)(2) + 25} = 1.72\,\text{k}\Omega$$

7.11 Move capacitor C_S from its parallel connection across R_{S2} to a position across R_{S1} in Fig. 4-33. Let $R_G = 1\,\text{M}\Omega$, $R_{S1} = 800\,\Omega$, $R_{S2} = 1.2\,\text{k}\Omega$, and $R_L = 1\,\text{k}\Omega$. The JFET is characterized by $g_m = 0.002\,\text{S}$ and $r_{ds} = 30\,\text{k}\Omega$. Find (*a*) the voltage-gain ratio $A_v = v_L / v_i$, (*b*) the current-gain ratio $A_i = i_L / i_i$, (*c*) the input impedance R_{in}, and (*d*) the output impedance R_o.

(*a*) The equivalent circuit (with current-source JFET model) is given in Fig. 7-18. By KVL,

$$v_{gs} = v_i - v_L \tag{1}$$

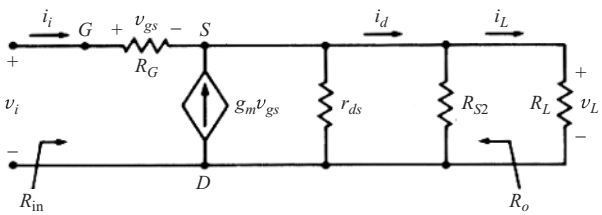


Fig. 7-18

Using v_i and v_L as node voltages, we have

$$i_i = \frac{v_i - v_L}{R_G} \tag{2}$$

Now let

$$\frac{1}{R_{eq}} = \frac{1}{r_{ds}} + \frac{1}{R_{S2}} + \frac{1}{R_L} = \frac{1}{30 \times 10^3} + \frac{1}{1.2 \times 10^3} + \frac{1}{1 \times 10^3} = \frac{1}{536}$$

By KCL and Ohm's law,

$$v_L = (i_i + g_m v_{gs}) R_{eq} \tag{3}$$

Substitution of (*1*) and (*2*) into (*3*) and rearrangement lead to

$$A_v = \frac{v_L}{v_i} = \frac{(g_m R_G + 1) R_{eq}}{R_G + (g_m R_G + 1) R_{eq}} = \frac{[(0.002)(1 \times 10^6) + 1](536)}{1 \times 10^6 + [(0.002)(1 \times 10^6) + 1](536)} = 0.517$$

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(*b*) The current-gain ratio follows from part *a* as

$$A_i = \frac{i_L}{i_i} = \frac{v_L/R_L}{(v_i - v_L)/R_G} = \frac{A_v R_G}{(1 - A_v)R_L} = \frac{(0.517)(1 \times 10^6)}{(1 - 0.517)(1 \times 10^3)} = 1070.4$$

(*c*) From (*2*),

$$i_i = \frac{v_i - v_L}{R_G} = \frac{v_i(1 - A_v)}{R_G} \tag{4}$$

R_{in} is found directly from (*4*) as

$$R_{\text{in}} = \frac{v_i}{i_i} = \frac{R_G}{1 - A_v} = \frac{1 \times 10^6}{1 - 0.517} = 2.07\,\text{M}\Omega$$

(*d*) We remove R_L and connect a driving-point source oriented such that $v_{dp} = v_L$. With v_i deactivated (shorted), $v_{gs} = -v_{dp}$. Then, by KCL,

$$i_{dp} = v_{dp}\left(\frac{1}{R_{S2}} + \frac{1}{r_{ds}} + \frac{1}{R_G}\right) - g_m v_{gs} = v_{dp}\left(\frac{1}{R_{S2}} + \frac{1}{r_{ds}} + \frac{1}{R_G} + g_m\right)$$

and

$$R_o = \frac{v_{dp}}{i_{dp}} = \frac{1}{\dfrac{1}{R_{S2}} + \dfrac{1}{r_{ds}} + \dfrac{1}{R_G} + g_m} = \frac{1}{\dfrac{1}{1.2 \times 10^3} + \dfrac{1}{30 \times 10^3} + \dfrac{1}{1 \times 10^6} + 0.002} = 348.7\,\Omega$$

7.12 Use the small-signal equivalent circuit to predict the peak values of i_d and v_{ds} in Example 4.3. Compare your results with that of Example 4.3, and comment on any differences.

The values of g_m and r_{ds} for operation near the Q point of Fig. 4-6 were determined in Problem 7.1. We may use the current-source model of Fig. 7-1(*a*) to form the equivalent circuit of Fig. 4-5. In that circuit, with $v_{gs} = \sin t\,\text{V}$, Ohm's law requires that

$$v_{ds} = -g_m v_{gs}(r_{ds} \| R_D) = \frac{-g_m r_{ds} R_D v_{gs}}{r_{ds} + R_D} = \frac{-(1.5 \times 10^{-3})(75 \times 10^3)(3 \times 10^3)v_{gs}}{75 \times 10^3 + 3 \times 10^3} = -4.33 v_{gs}$$

Thus,

$$V_{dsm} = 4.33 V_{gsm} = 4.33(1) = 4.33\,\text{V}$$

Also, from Fig. 7-1(*a*),

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_{ds}}$$

so

$$I_{dm} = g_m V_{gsm} + \frac{V_{dsm}}{r_{ds}} = (1.5 \times 10^{-3})(1) + \frac{1}{75 \times 10^3} = 1.513\,\text{mA}$$

The ± 1-V excursion of v_{gs} leads to operation over a large portion of the nonlinear drain characteristics. Consequently, the small-signal equivalent circuit predicts greater positive peaks and smaller negative peaks of i_d and v_{ds} than the graphical solution of Example 4.3, which inherently accounts for the nonlinearities.

7.13 For the JFET drain characteristics of Fig. 4-2(*a*), take v_{DS} as the dependent variable [so that $v_{DS} = f(v_{GS}, i_D)$] and derive the voltage-source small-signal model.

For small variations about a Q point, the chain rule gives

$$v_{ds} = \Delta v_{DS} \approx dv_{DS} = \left.\frac{\partial v_{DS}}{\partial v_{GS}}\right|_Q v_{gs} + \left.\frac{\partial v_{DS}}{\partial i_D}\right|_Q i_d \tag{1}$$

Now we may define

$$\left.\frac{\partial v_{DS}}{\partial v_{GS}}\right|_Q = \mu \qquad \text{and} \qquad \left.\frac{\partial v_{DS}}{\partial i_D}\right|_Q = r_{ds}$$

If the JFET operates in the pinchoff region, then gate current is negligible and (*1*) is satisfied by the equivalent circuit of Fig. 7-1(*b*).

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7.14 Find a current-source small-signal equivalent circuit for the CD FET amplifier.

Norton's theorem can be applied to the voltage-source model of Fig. 7-12(*b*). The open-circuit voltage at terminals S, D (with R_S removed) is

$$v_{oc} = \frac{\mu}{\mu + 1} v_{gd} \tag{1}$$

The short-circuit current at terminals S, D is

$$i_{SC} = \frac{\dfrac{\mu}{\mu + 1} v_{gd}}{r_{ds}/(\mu + 1)} = \frac{\mu}{r_{ds}} v_{gd} = g_m v_{gd} \tag{2}$$

The Norton impedance is found as the ratio of (*1*) to (*2*):

$$R_N = \frac{v_{oc}}{i_{SC}} = \frac{\dfrac{\mu}{\mu + 1} v_{gd}}{g_m v_{gd}} = \frac{\mu}{(\mu + 1) g_m}$$

The equivalent circuit is given in Fig. 7-19. Usually, $\mu \gg 1$ and, thus, $R_N \approx 1/g_m$.

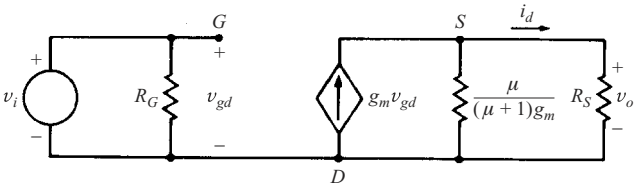


Fig. 7-19

7.15 Replace the JFET of Fig. 7-5 with the *n*-channel MOSFET that has the parameters of Example 4.4 except Vto $= -4$ V. Let $R_1 = 200\,\text{k}\Omega$, $R_2 = 600\,\text{k}\Omega$, $R_D = R_S = 2\,\text{k}\Omega$, $R_L = 3\,\text{k}\Omega$, $C_{C1} = C_{C2} = C_S = 100\,\mu\text{F}$, and $V_{DD} = 15\,\text{V}$. Assume $v_S = 0.250 \sin(2\pi \times 10^4 t)\,\text{V}$ for computation purposes and determine the voltage gain of this amplifier circuit using SPICE methods.

The netlist code below describes the MOSFET amplifier circuit:

```
Prb7_15.CIR
vs  1 0 SIN(0V 0.25V 10kHz)
VDD 5 0 DC 15V
CC1 1 2 100uF
CC2 3 6 100uF
CS  4 0 100uF
R1  2 0 200kohm
R2  5 2 600kohm
RD  5 3 2kohm
RS  4 0 2kohm
RL  6 0 3kohm
M 3  2 4 4 NMOSG
.MODEL NMOSG NMOS (Vto=-4V Kp=0.0008ApVsq
+ Rd=1ohm Rg=1kohm)
.TRAN 1us 0.1ms
.PROBE
.END
```

Execute ⟨Prb7_15.CIR⟩ and use the Probe and FFT features of PSpice to plot the instantaneous waveforms of v_S and v_L along with their Fourier spectra as shown by Fig. 7-20. The voltage gain follows from ratio of

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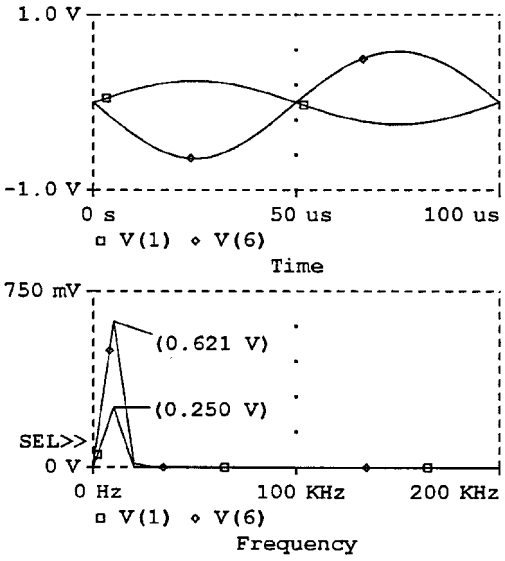


Fig. 7-20

the marked spectra magnitudes with the negative sign accounting for the 180° phase shift observed from inspection of the instantaneous waveforms.

$$A_v = \frac{v_L}{v_S} = -\frac{0.621}{0.250} = 2.48$$

7.16 In the cascaded MOSFET amplifier of Fig. 7-21, $C_C \to \infty$. Find (*a*) the voltage-gain ratio $A_v = v_L/v_i$ and (*b*) the current-gain ratio $A_i = i_L/i_i$.

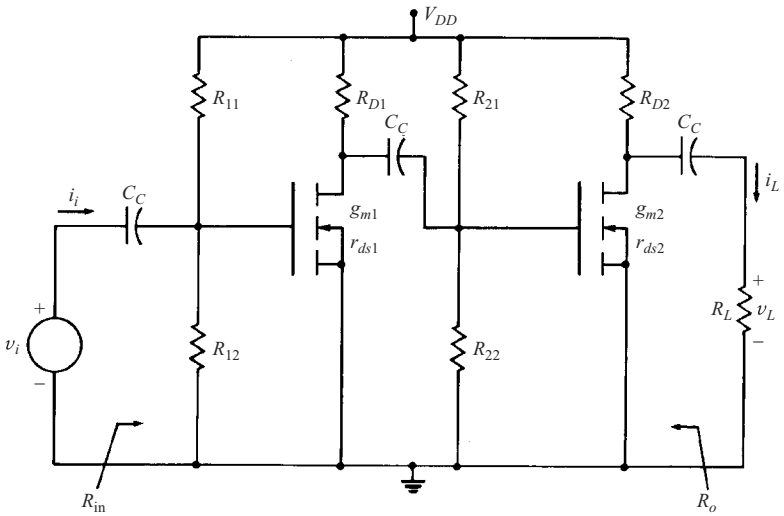


Fig. 7-21

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(*a*) The small-signal equivalent circuit is given in Fig. 7-22. Using the result of Example 7.1, but replacing R_D with $R_{D1} \| R_{G2}$ where $R_{G2} = R_{21} \| R_{22}$, we have

$$A_{v1} = \frac{-g_{m1} r_{ds1} (R_{D1} \| R_{G2})}{r_{ds1} + (R_{D1} \| R_{G2})} \tag{1}$$

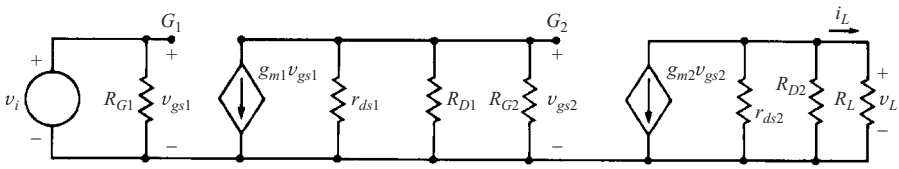


Fig. 7-22

Similarly,
$$A_{v2} = \frac{-g_{m2} r_{ds2} (R_{D2} \| R_L)}{r_{ds2} + (R_{D2} \| R_L)} \tag{2}$$

Then
$$A_v = A_{v1} A_{v2} = \frac{g_{m1} g_{m2} r_{ds1} r_{ds2} (R_{D1} \| R_{G2})(R_{D2} \| R_L)}{[r_{ds1} + (R_{D1} \| R_{G2})][r_{ds2} + (R_{D2} \| R_L)]} \tag{3}$$

(*b*) Realizing that $R_{G1} = R_{11} \| R_{12}$, we have

$$A_i = \frac{i_L}{i_i} = \frac{v_o / R_L}{v_i / R_{G1}} = A_v \frac{R_{G1}}{R_L}$$

where A_v is given by (*3*).

7.17 For the JFET-BJT Darlington amplifier of Fig. 7-23(*a*), find (*a*) the voltage-gain ratio $A_v = v_e / v_i$ and (*b*) the output impedance R_o. Assume $h_{re} = h_{oe} = 0$ and that $R_G \gg R_1, R_2$.

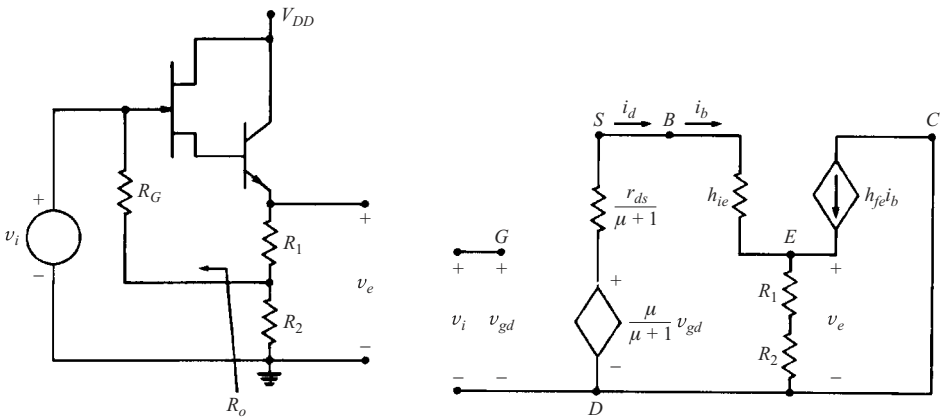


Fig. 7-23

(*a*) The small-signal equivalent circuit is given in Fig. 7-23(*b*), where the CD model of the JFET (see Problem 7.5) has been used. Since $i_b = i_d$ and $v_{gd} = v_i$, KVL yields

$$\frac{\mu}{\mu + 1} v_i = i_d \left(\frac{r_{ds}}{\mu + 1} + h_{ie} \right) + (h_{fe} + 1) i_d (R_1 + R_2) \tag{1}$$

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By Ohm's law,

$$v_e = (h_{fe} + 1)i_d(R_1 + R_2) \tag{2}$$

Solving (*1*) for i_d, substituting the result into (*2*), and rearranging give

$$A_v = \frac{v_e}{v_i} = \frac{\mu(h_{fe} + 1)(R_1 + R_2)}{r_{ds} + (\mu + 1)[h_{ie} + (h_{fe} + 1)(R_1 + R_2)]}$$

(*b*) We replace $R_1 + R_2$ with a driving-point source oriented such that $v_{dp} = v_e$. With v_i deactivated (short circuited), $v_{gd} = 0$. Then, by Ohm's law,

$$i_b = -\frac{v_{dp}}{h_{ie} + r_{ds}/(\mu + 1)} \tag{3}$$

and by KCL,

$$i_{dp} = -(h_{fe} + 1)i_b \tag{4}$$

Substituting (*3*) into (*4*) and rearranging give

$$R_o = \frac{v_{dp}}{i_{dp}} = \frac{r_{ds} + (\mu + 1)h_{ie}}{(\mu + 1)(h_{fe} + 1)}$$

7.18 For a triode with plate characteristics given by Fig. 7-8, find (*a*) the perveance κ and (*b*) the amplification factor μ.

(*a*) The perveance can be evaluated at any point on the $v_G = 0$ curve. Choosing the point with coordinates $i_P = 15\,\text{mA}$ and $v_P = 100\,\text{V}$, we have, from (*4.9*),

$$\kappa = \frac{i_P}{v_P^{3/2}} = \frac{15 \times 10^{-3}}{100^{3/2}} = 15\,\mu\text{A/V}^{3/2}$$

(*b*) The amplification factor is most easily evaluated along the v_P axis. From (*4.9*), for the point $i_P = 0$, $v_P = 100\,\text{V}$, $v_G = -4\,\text{V}$, we obtain

$$\mu = -\frac{v_P}{v_G} = -\frac{100}{-4} = 25$$

7.19 Use the current-source small-signal triode model of Fig. 7-9(*a*) to derive the voltage-source model of Fig. 7-9(*b*).

We need to find the Thévenin equivalent for the circuit to the left of the output terminals in Fig. 7-9(*a*). If the independent source is deactivated, then $v_g = 0$; thus, $g_m v_g = 0$, and the dependent current source acts as an open circuit. The Thévenin resistance is then $R_{Th} = r_p$. The open-circuit voltage appearing at the output terminals is

$$v_{Th} = -g_m v_g r_p \equiv -\mu v_g$$

where $\mu \equiv g_m r_p$ is the *amplification factor*. Proper series arrangement of v_{Th} and R_{Th} gives the circuit of Fig. 7-9(*b*).

7.20 For the amplifier of Example 7.6, (*a*) use (*7.9*) to evaluate the plate resistance and (*b*) use (*7.10*) to find the transconductance.

(*a*)
$$r_p \approx \left.\frac{\Delta v_P}{\Delta i_P}\right|_{v_G=-4} = \frac{218 - 152}{(14.7 - 8.1) \times 10^{-3}} = 10\,\text{k}\Omega$$

(*b*)
$$g_m \approx \left.\frac{\Delta i_P}{\Delta v_G}\right|_{v_P=186} = \frac{(14.7 - 8.1) \times 10^{-3}}{-2 - (-6)} = 1.65\,\text{mS}$$

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7.21 Find an expression for the voltage gain $A_v = v_p/v_g$ of the basic triode amplifier of Fig. 4-12, using an ac equivalent circuit.

The equivalent circuit of Fig. 7-9(*b*) is applicable if R_L is connected from P to K. Then, by voltage division in the plate circuit,

$$v_p = \frac{R_L}{R_L + r_p}(-\mu v_g) \qquad \text{so} \qquad A_v = \frac{v_p}{v_g} = \frac{-\mu R_L}{R_L + r_p}$$

7.22 In the amplifier of Problem 4.27, let $v_S = 2\cos\omega t$ V. (*a*) Draw the ac load line on Fig. 4-31. (*b*) Graphically determine the voltage gain. (*c*) Calculate the voltage gain using small-signal analysis.

(*a*) If capacitor C_K appears as a short circuit to ac signals, then application of KVL around the plate circuit of Fig. 4-30 gives, as the equation of the ac load line, $V_{PP} + V_{GQ} = i_P R_L + v_P$. Thus, the ac load line has vertical and horizontal intercepts

$$\frac{V_{PP} + V_{GQ}}{R_L} = \frac{300 - 4}{11.6 \times 10^3} = 25.5\,\text{mA} \qquad \text{and} \qquad V_{PP} + V_{GQ} = 296\,\text{V}$$

as shown on Fig. 4-31.

(*b*) We have $v_g = v_S$; thus, as v_g swings ± 2 V along the ac load line from the Q point in Fig. 4-31, v_p swings a total of $2V_{pm} = 213 - 145 = 68$ V as shown. The voltage gain is then

$$A_v = -\frac{2V_{pm}}{2V_{gm}} = -\frac{68}{4} = -17$$

where the minus sign is included to account for the phase reversal between v_p and v_g.

(*c*) Applying (*7.9*) and (*7.10*) at the Q point of Fig. 4-31 yields

$$r_p = \left.\frac{\Delta v_P}{\Delta i_P}\right|_{v_G=-4} = \frac{202 - 168}{(15 - 8) \times 10^{-3}} = 4.86\,\text{k}\Omega$$

$$g_m = \left.\frac{\Delta i_P}{\Delta v_G}\right|_{v_P=180} = \frac{(15.5 - 6.5) \times 10^{-3}}{-3 - (-5)} = 4.5\,\text{mS}$$

Then, $\mu \equiv g_m r_p = 21.87$, and Problem 7.21, yields

$$A_v = -\frac{\mu R_L}{R_L + r_p} = -\frac{(21.87)(11.6 \times 10^3)}{(11.6 + 4.86) \times 10^3} = -15.41$$

7.23 The input admittance to a triode modeled by the small-signal equivalent circuit of Fig. 7-9(*b*) is obviously zero; however, there are interelectrode capacitances that must be considered for high-frequency operation. Add these interelectrode capacitances (grid-cathode capacitance C_{gk}; plate-grid, C_{pg}; and plate-cathode, C_{pk}) to the small-signal equivalent circuit of Fig. 7-9(*b*). Then (*a*) find the input admittance Y_{in}, (*b*) find the output admittance Y_o, and (*c*) develop a high-frequency model for the triode.

(*a*) With the interelectrode capacitances in position, the small-signal equivalent circuit is given by Fig. 7-24. The input admittance is

$$Y_{\text{in}} = \frac{I_S}{V_S} = \frac{I_1 + I_2}{V_S} \tag{1}$$

But

$$I_1 = \frac{V_S}{1/sC_{gk}} = sC_{gk}V_S \tag{2}$$

and

$$I_2 = \frac{V_S - V_o}{1/sC_{pg}} = sC_{pg}(V_S - V_o) \tag{3}$$

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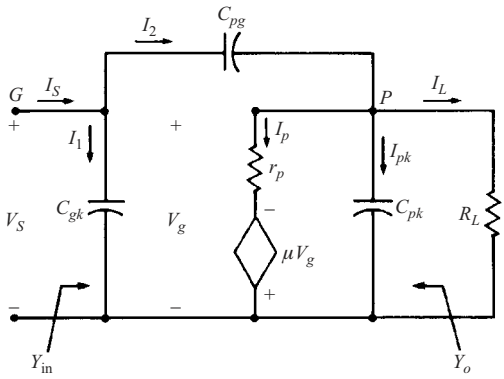


Fig. 7-24

Substituting (*2*) and (*3*) into (*1*) and rearranging give

$$Y_{\text{in}} = s\left[C_{gk} + \left(1 - \frac{V_o}{V_S}\right)C_{pg}\right] \tag{4}$$

Now, from the result of Problem 7.21,

$$\frac{V_o}{V_S} = -\frac{\mu R_L}{R_L + r_p} \tag{5}$$

so (*4*) becomes

$$Y_{\text{in}} = s\left[C_{gk} + \left(1 + \frac{\mu R_L}{R_L + r_p}\right)C_{pg}\right] \tag{6}$$

(*b*) The output admittance is

$$Y_o = -\frac{I_L}{V_o} = -\frac{I_2 - I_p - I_{pk}}{V_o} \tag{7}$$

and

$$I_{pk} = sC_{pk}V_o \tag{8}$$

Let Y_o' be the output admittance that would exist if the capacitances were negligible; then

$$I_p = Y_o'V_o \tag{9}$$

so that

$$Y_o = s\left[\left(1 + \frac{R_L + r_p}{\mu R_L}\right)C_{pg} + C_{pk}\right] + Y_o' \tag{10}$$

(*c*) From (*6*) and (*10*) we see that high-frequency triode operation can be modeled by Fig. 7-9(*b*) with a capacitor $C_{\text{in}} = C_{gk} + [1 + R_L/(R_L + r_p)]C_{pg}$ connected from the grid to the cathode, and a capacitor $C_o = [1 + (R_L + r_p)/\mu R_L]C_{pg} + C_{pk}$ connected from the plate to the cathode.

Supplementary Problems

7.24 Find the input impedance as seen by the source v_i of Example 4.2 if C_C is large. *Ans.* 940 kΩ

7.25 Show that the transconductance of a JFET varies as the square root of the drain current.
Ans. $g_m = (2\sqrt{I_{DSS}}/V_{p0})\sqrt{i_D}$

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7.26 In the amplifier of Fig. 4-15, $R_1 = 20\,\text{k}\Omega$, $R_2 = 100\,\text{k}\Omega$, $R_3 = 1\,\text{M}\Omega$, $r_{ds} = 30\,\text{k}\Omega$, $\mu = 150$ (see Problem 7.2), and $R_S = 1\,\text{k}\Omega$. Find (*a*) $A_v = v_o/v_i$, (*b*) $A_i = i_d/i_i$, and (*c*) Z_o.
Ans. (*a*) 0.829; (*b*) 843; (*c*) 198.7 Ω

7.27 Find the voltage gain of the CG amplifier of Fig. 7-13(*a*).
Ans. $A_v = v_o/v_i = (\mu + 1)R_D/[R_D + r_{ds} + (\mu + 1)R_S]$

7.28 Find the voltage gain $A_{v2} = v_2/v_i$ for the circuit of Fig. 7-25(*a*). Figure 7-25(*b*) is a small-signal equivalent circuit in which impedance reflection has been used for simplification.
Ans. $A_{v2} = -\mu R_D/[R_D + r_{ds} + (\mu + 1)R_S]$

7.29 Let $R_{L1} = R_{L2} \to \infty$ for the amplifier of Fig. 7-25(*a*). If $R_D = R_S$, the circuit is commonly called a *phase splitter*, since $v_2 = -v_1$ (the outputs are equal in magnitude but 180° out of phase). Find $A_{v1} = v_1/v_i$ and, by comparison with A_{v2} of Problem 7.28, verify that the circuit actually is a phase splitter.
Ans. $A_{v1} = \mu R_S/[R_D + r_{ds} + (\mu + 1)R_S]$

7.30 For the circuit of Fig. 7-25(*a*), model the MOSFET by NMOSG of Example 4.4 except use Vto = −4 V. Let $V_{GG} = -2\,\text{V}$, $V_{DD} = 15\,\text{V}$, $R_D = R_S = 1.5\,\text{k}\Omega$, $R_{L1} = R_{L2} = 10\,\text{k}\Omega$, and $C_{C1} = C_{C2} = 100\,\mu\text{F}$. Use SPICE analysis to show that $v_1 = -v_2$, thus substantiating the claim of Problem 7.29 that the circuit is a phase splitter. (*Netlist code available from author website.*)

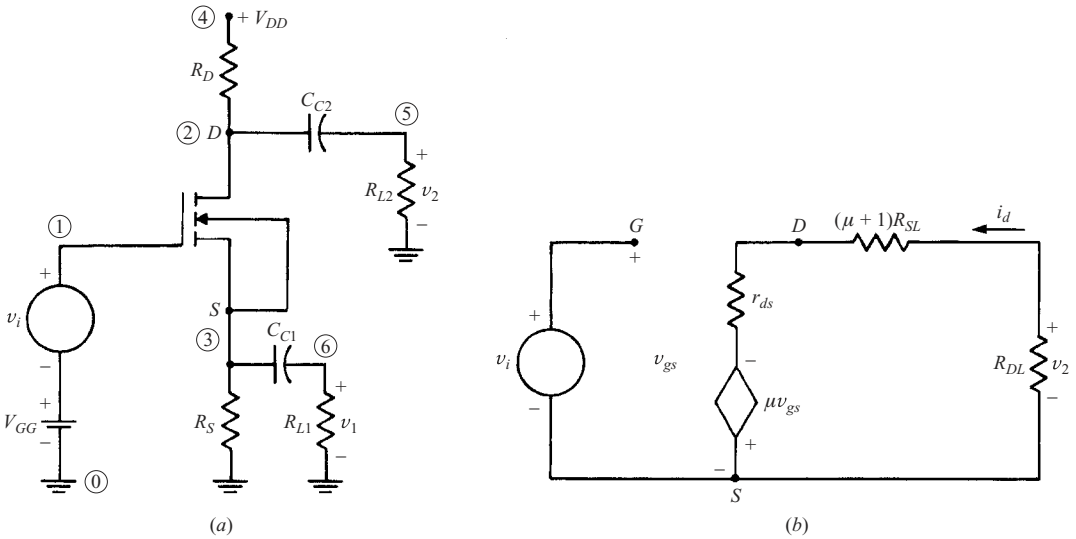


Fig. 7-25

7.31 For the amplifier circuit of Example 7.4, reduce the value of the bypass capacitor C_S to 0.01 μF so that R_S no longer appears shorted to ac signals and assess the impact on voltage gain. (*Netlist code available from author website.*) *Ans.* $A_v = 1.22\angle -139°$

7.32 The series-connected JFETs of Fig. 4-23 are identical, with $\mu = 70$, $r_{ds} = 30\,\text{k}\Omega$, $R_G = 100\,\text{k}\Omega$, and $R_D = R_L = 4\,\text{k}\Omega$. Find (*a*) the voltage-gain ratio $A_v = v_L/v_i$, (*b*) the current-gain ratio $A_i = i_L/i_i$, and (*c*) the output impedance R_o. *Ans.* (*a*) $A_v = -9.32$; (*b*) $A_i = -233$; (*c*) $R_o = 2.16\,\text{M}\Omega$

7.33 The JFET amplifier of Fig. 4-33 has $R_G = 1\,\text{M}\Omega$, $R_{S1} = 800\,\Omega$, $R_{S2} = 1.2\,\text{k}\Omega$, and $R_L = 1\,\text{k}\Omega$. The JFET obeys (*4.2*) and is characterized by $I_{DSS} = 10\,\text{mA}$, $V_{p0} = 4\,\text{V}$, $V_{GSQ} = -2\,\text{V}$, and $\mu = 60$. Determine (*a*) g_m by use of (*7.3*), (*b*) r_{ds}, and (*c*) the voltage-gain ratio $A_v = v_L/v_i$.
Ans. (*a*) 2.5 mS; (*b*) 24 kΩ; (*c*) 0.52

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7.34 For the JFET amplifier of Fig. 4-20, find expressions for (*a*) the voltage-gain ratio $A_{v1} = V_o/V_G$ and (*b*) the voltage-gain ratio $A_{v2} = V_1/V_G$.
Ans. (*a*) $A_{v1} = \mu R_S/[(\mu+1)R_S + R_D + r_{ds}]$; (*b*) $A_{v2} = -\mu R_D/[(\mu+1)R_S + R_D + r_{ds}]$

7.35 Frequently, in integrated circuits, the gate of a FET is connected to the drain; then the drain-to-source terminals are considered the terminals of a resistor. Starting with (*7.2*), show that if $\mu \gg 1$, then the small-signal equivalent circuit is no more than a resistor of value $1/g_m$.

7.36 For the CS amplifier of Fig. 7-2(*b*), find (*a*) the input impedance R_{in} and (*b*) the output impedance R_o.
Ans. (*a*) $R_{\text{in}} = R_G$; (*b*) $R_o = r_{ds}$

7.37 For the CD amplifier of Fig. 7-3(*b*), find (*a*) the input impedance R_{in} and (*b*) the output impedance R_o.
Ans. (*a*) $R_{\text{in}} = R_G$; (*b*) $R_o = r_{ds}/(\mu+1)$

7.38 For the CG amplifier of Fig. 7-4, find (*a*) the input impedance R_{in} and (*b*) the output impedance R_o.
Ans. (*a*) $R_{\text{in}} = R_S(R_D + r_{ds})/[(\mu+1)R_S + R_D + r_{ds}]$; (*b*) $R_o = r_{ds}$

7.39 In the circuit of Fig. 7-26, the two FETs are identical. Find (*a*) the voltage-gain ratio $A_v = v_o/v_i$ and (*b*) the output impedance R_o.
Ans. (*a*) $A_v = -\mu R_L|\{2R_L + 2[(\mu+1)R + r_{ds}]\}$; (*b*) $R_o = \frac{1}{2}[(\mu+1)R + r_{ds}]$

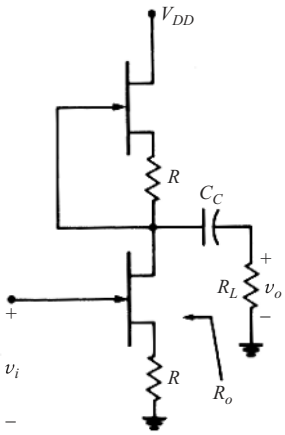


Fig. 7-26

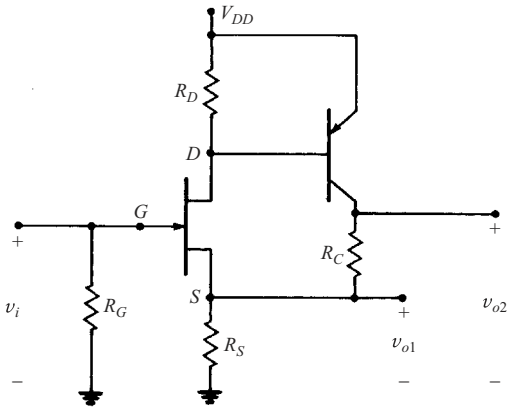


Fig. 7-27

7.40 For the cascaded MOSFET amplifier of Fig. 7-21 with equivalent circuit in Fig. 7-22, find (*a*) the input impedance R_{in} and (*b*) the output impedance R_o.
Ans. (*a*) $R_{\text{in}} = R_{11}R_{12}/(R_{11} + R_{12})$; (*b*) $R_o = r_{ds2}R_{D2}/(r_{ds2} + R_{D2})$

7.41 In the cascaded FET-BJT circuit of Fig. 7-27, assume $h_{re} = h_{oe} = 0$ and $h_{ie} \ll R_D$. Find expressions for (*a*) $A_{v1} = v_{o1}/v_i$ and (*b*) $A_{v2} = v_{o2}/v_i$.
Ans. (*a*) $A_{v1} = \mu(h_{fe}+1)R_S/[(\mu+1)(h_{fe}+1)R_S + h_{ie} + r_{ds}]$;
(*b*) $A_{v2} = [\mu h_{fe}R_C + \mu(h_{fe}+1)R_S]/[(\mu+1)(h_{fe}+1)R_S + h_{ie} + r_{ds}]$

7.42 Suppose the amplifier of Problem 4.25 has plate resistance $r_p = 20\,\text{k}\Omega$ and $v_S = 1\cos\omega t\,\text{V}$. Find its amplification factor μ using the small-signal voltage-source model of Fig. 7-9(*b*). *Ans.* 30

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7.43 Suppose the bypass capacitor C_K is removed from the amplifier of Fig. 4-30. Find (*a*) an expression for the voltage gain and (*b*) the percentage deviation of the voltage gain from the result of Problem 7.22.
Ans. $A_v = -\mu R_L/[R_L + r_p + (\mu + 1)R_k]$; (b) 35.7% decrease

7.44 Two triodes are parallel-connected plate to plate, grid to grid, and cathode to cathode. Find the equivalent amplification factor μ_{eq} and plate resistance r_{peq} for the combination.
Ans. $\mu_{eq} = (\mu_1 r_{p2} + \mu_2 r_{p1})/(r_{p1} + r_{p2})$, $r_{peq} = r_{p1} r_{p2}/(r_{p1} + r_{p2})$

7.45 The circuit of Fig. 7-28 is a *cathode follower*, so called because v_o is in phase with v_S and nearly equal to it in magnitude. Find a voltage-source equivalent circuit of the form of Fig. 7-9(*b*) that models the cathode follower. *Ans.* See Fig. 7-29

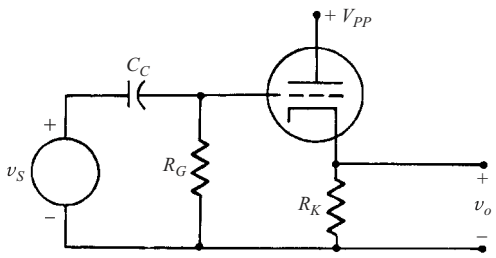


Fig. 7-28

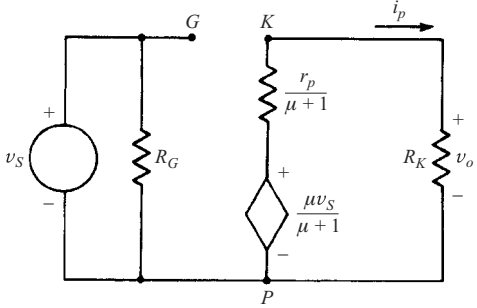


Fig. 7-29

7.46 For the cathode follower of Fig. 7-28, $r_p = 5\,\text{k}\Omega$, $\mu = 25$, and $R_K = 15\,\text{k}\Omega$. (*a*) Use the equivalent circuit of Fig. 7-29 to find a formula for the voltage gain. (*b*) Evaluate the voltage gain.
Ans. (*a*) $A_v = \mu R_K/[r_p + (\mu + 1)R_K]$; (*b*) 0.95

7.47 The cathode follower is frequently used as a final-stage amplifier to effect an impedance match with a low-impedance load for maximum power transfer. In such a case, the load (resistor R_L) is capacitor-coupled to the right of R_K in Fig. 7-29. Find an expression for the internal impedance (output impedance) of the cathode follower as seen by the load. *Ans.* $R_o = R_K r_p/[r_p + (\mu + 1)R_K]$

7.48 The amplifier of Fig. 7-30 is a *common-grid* amplifier. By finding a Thévenin equivalent for the network to the right of G, K and another for the network to the left of R_P, verify that the small-signal circuit of Fig. 7-31 is valid. Then, (*a*) find an expression for the voltage gain; (*b*) evaluate the voltage gain for the typical values $\mu = 20$, $r_p = 5\,\text{k}\Omega$, $R_K = 1\,\text{k}\Omega$, and $R_P = 15\,\text{k}\Omega$; (*c*) find the input resistance R_{in}; and (*d*) find the output resistance R_o.
Ans. (*a*) $A_v = (\mu + 1)R_P/[R_P + r_p + (\mu + 1)R_K]$; (*b*) 7.7; (*c*) $R_{\text{in}} = 1.95\,\text{k}\Omega$; (*d*) $R_o = 26\,\text{k}\Omega$

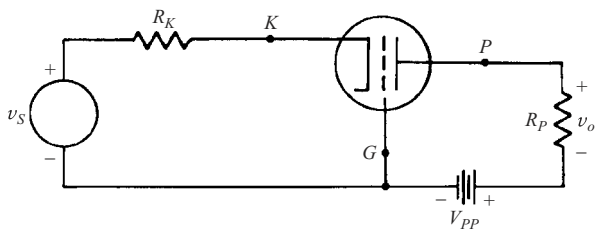


Fig. 7-30

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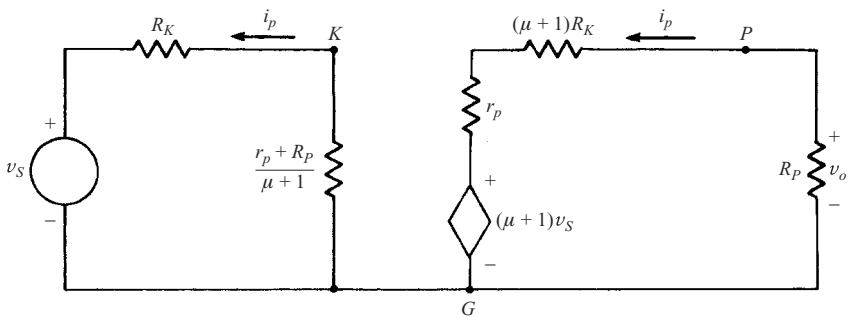


Fig. 7-31

7.49 In the circuit of Fig. 7-32, the triodes are identical, $R_G \approx \infty$, and $(R_L + r_p)/(\mu + 1) \ll R_K$. Show that the circuit is a difference amplifier, meaning that $v_o = f(v_1 - v_2)$. *Ans.* $v_o = \mu R_L(v_1 - v_2)/(2R_L + 2r_p)$

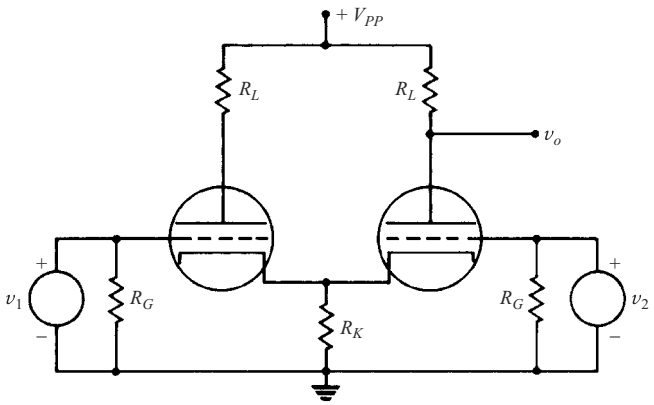


Fig. 7-32

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CHAPTER 8

Frequency Effects in Amplifiers

8.1. INTRODUCTION

In the analyses of the two preceding chapters, we assumed *operation* in the midfrequency range, in which the reactances of all bypass and coupling capacitors can be considered to be zero while all inherent capacitive reactances associated with transistors are infinitely large. However, over a wide range of signal frequencies, the response of an amplifier is that of a *band-pass filter*: Low and high frequencies are attenuated, but signals over a band (or range) of frequencies between high and low are not attenuated. The typical frequency behavior of an *RC*-coupled amplifier is illustrated by Fig. 8-1(*a*). In practical amplifiers the midfrequency range spans several orders of magnitude, so that terms in the gain ratio expression which alter low-frequency gain are essentially constant over the high-frequency range. Conversely, terms that alter high-frequency gain are practically constant over the low-frequency range. Thus the high- and low-frequency analyses of amplifiers are treated as two independent problems.

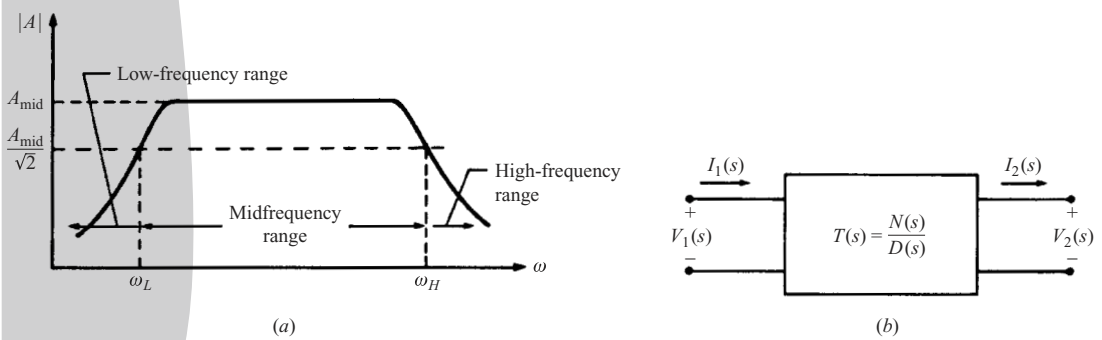


Fig. 8-1

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8.2. BODE PLOTS AND FREQUENCY RESPONSE

Any linear two-port electrical network that is free of independent sources (including a small-signal amplifier equivalent circuit) can be reduced to the form of Fig. 8-1(*b*), where $T(s) = N(s)/D(s)$ is the Laplace-domain *transfer function* (a ratio of port variables).

Of particular interest in amplifier analysis are the *current-gain ratio* (*transfer function*) $T(s) = A_i(s)$ and *voltage-gain ratio* (*transfer function*) $T(s) = A_v(s)$. For a sinusoidal input voltage signal, the Laplace transform pair

$$v_1(t) = V_{1m} \sin \omega t \leftrightarrow V_1(s) = \frac{V_{1m}\omega}{s^2 + \omega^2}$$

is applicable, and the network response is given by

$$V_2(s) = A_v(s)V_1(s) = \frac{A_v(s)V_{1m}\omega}{s^2 + \omega^2} \tag{8.1}$$

Without loss of generality, we may assume that the polynomial $D(s) = 0$ has n distinct roots. Then the partial-fraction expansion of (*8.1*) yields

$$V_2(s) = \frac{k_1}{s - j\omega} + \frac{k_2}{s + j\omega} + \frac{k_3}{s + p_1} + \frac{k_4}{s + p_2} + \cdots + \frac{k_{n+2}}{s + p_n} \tag{8.2}$$

where the first two terms on the right-hand side are forced-response terms (called the *frequency response*), and the balance of the terms constitute the transient response. The transient response diminishes to zero with time, provided the roots of $D(s) = 0$ are located in the left half plane of complex numbers (the condition for a *stable* system).

The coefficients k_1 and k_2 are evaluated by the method of residues, and the results are used in an inverse transformation to the time-domain steady-state sinusoidal response given by

$$v_2(t) = V_{1m}|A_v(j\omega)| \sin(\omega t + \phi) = V_{2m} \sin(\omega t + \phi) \tag{8.3}$$

(see Problem 8.23). The *network phase angle* ϕ is defined as

$$\phi = \tan^{-1} \frac{\text{Im}\{A_v(j\omega)\}}{\text{Re}\{A_v(j\omega)\}} \tag{8.4}$$

From (*8.4*), it is apparent that a sinusoidal input to a stable, linear, two-port network results in a steady-state output that is also sinusoidal; the input and output waveforms differ only in amplitude and phase angle.

For convenience, we make the following definitions:

1. Call $A(j\omega)$ the *frequency transfer function*.
2. Define $M \equiv |A(j\omega)|$, the *gain ratio*.
3. Define $M_{db} \equiv 20 \log M = 20 \log |A(j\omega)|$, the *amplitude ratio*, measured in *decibels* (db).

The subscript v or i may be added to any of these quantities to specifically denote reference to voltage or current, respectively. The graph of M_{db} (simultaneously with ϕ if desired) versus the logarithm of the input signal frequency (positive values only) is called a *Bode plot*.

Example 8.1. A simple first-order network has Laplace-domain transfer function and frequency transfer function

$$A(s) = \frac{1}{\tau s + 1} \qquad \text{and} \qquad A(j\omega) = \frac{1}{1 + j\omega\tau}$$

where τ is the system time constant. (*a*) Determine the network phase angle ϕ and the amplitude ratio M_{db} and (*b*) construct the Bode plot for the network.

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(*a*) In polar form, the given frequency transfer function is

$$A(j\omega) = \frac{1}{\sqrt{1+(\omega\tau)^2}\ \underline{|\tan^{-1}(\omega\tau/1)}} = \frac{1}{\sqrt{1+(\omega\tau)^2}}\ \underline{|\tan^{-1}\omega\tau}$$

Hence,
$$\phi = -\tan^{-1}\omega\tau \tag{8.5}$$

and
$$M_{db} = 20\log|A(j\omega)| = 20\log\frac{1}{\sqrt{1+(\omega\tau)^2}} = -10\log[1+(\omega\tau)^2] \tag{8.6}$$

(*b*) If values of (*8.5*) and (*8.6*) are calculated and plotted for various values of ω, then a Bode plot is generated. This is done in Fig. 8-2, where ω is given in terms of time constants τ rather than, say, hertz. This particular system is called a *lag network* because its phase angle ϕ is negative for all ω.

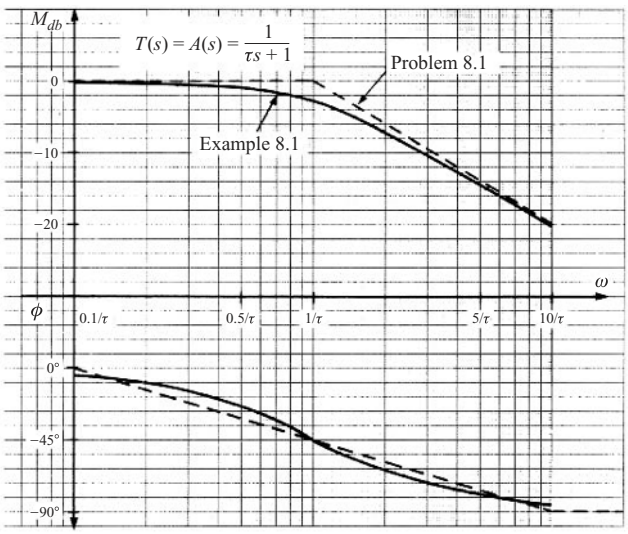


Fig. 8-2

Example 8.2. A simple first-order network has Laplace-domain transfer function and frequency transfer function

$$A(s) = \tau s + 1 \qquad \text{and} \qquad A(j\omega) = 1 + j\omega\tau$$

Determine the network phase angle ϕ and the amplitude ratio M_{db}, and discuss the nature of the Bode plot.

After $A(j\omega)$ is converted to polar form, it becomes apparent that

$$\phi = \tan^{-1}\omega\tau \tag{8.7}$$

and
$$M_{db} = 20\log|A(j\omega)| = 20\log\sqrt{1+(\omega\tau)^2} = 10\log[1+(\omega\tau)^2] \tag{8.8}$$

Comparison of (*8.5*) and (*8.7*) reveals that the network phase angle is the mirror image of the phase angle for the network of Example 8.1. (As ω increases, ϕ ranges from 0° to 90°.) Further, (*8.8*) shows that the amplitude ratio is the mirror image of the amplitude ratio of Example 8.1. (As ω increases, M_{db} ranges from 0 to positive values.) Thus, the complete Bode plot consists of the mirror images about zero of M_{db} and ϕ of Fig. 8-2. Since here the phase angle ϕ is everywhere positive, this network is called a *lead network*.

A *break frequency* or *corner frequency* is the frequency $1/\tau$. For a simple lag or lead network, it is the frequency at which $M^2 = |A(j\omega)|^2$ has changed by 50 percent from its value at $\omega = 0$; at that frequency, M_{db} has changed by 3 db from its value at $\omega = 0$. Corner frequencies serve as key points in the construction of Bode plots.

Example 8.3. Describe the Bode plot of a network whose output is the time derivative of its input.

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The network has Laplace-domain transfer function $A(s) = s$ and frequency transfer function $A(j\omega) = j\omega$. Converting $A(j\omega)$ to polar form shows that

$$\phi = \tan^{-1}\frac{\omega}{0} = 90^\circ \tag{8.9}$$

and

$$M_{db} = 20\log\omega \tag{8.10}$$

Obviously, the network phase angle is a constant 90°. By (*8.10*), $M_{db} = 0$ when $\omega = 1$; further, M_{db} increases by 20 db for each order-of-magnitude (*decade*) change in ω. A graph of M_{db} versus the logarithm of ω would thus have a slope of 20 db per decade of frequency. A complete Bode plot is shown in Fig. 8-3.

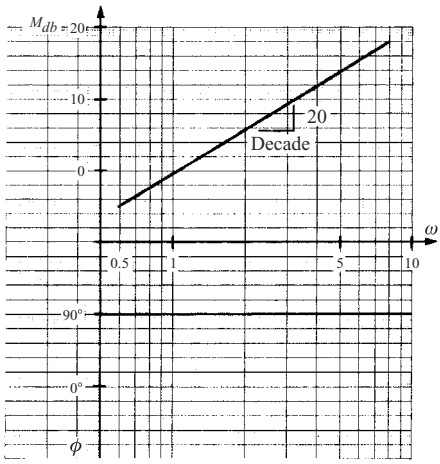


Fig. 8-3

The exact Bode plot of a network frequency transfer function is tedious to construct. Frequently, sufficiently accurate information can be obtained from an *asymptotic* Bode plot (see Problem 8.1).

Example 8.4. The exact Bode plot for the first-order system of Example 8.1 is given in Fig. 8-2. (*a*) Add the asymptotic Bode plot to that figure. (*b*) Describe the asymptotic Bode plot for the system of Example 8.2.

(*a*) Asymptotic Bode plots are piecewise-linear approximations. The asymptotic plot of M_{db} for a simple lag network has value zero out to the single break frequency $\omega = 1/\tau$ and then *decreases* at 20 db per decade. The asymptotic plot of ϕ has the value zero out to $\omega = 0.1/\tau$, decreases linearly to -90° at $\omega = 10/\tau$, and then is constant at -90°. Both asymptotic plots are shown dashed in Fig. 8-2.

(*b*) The asymptotic Bode plot for a simple lead network is the mirror image of that for a simple lag network. Thus, the asymptotic plot of M_{db} in Example 8.2 is zero out to $\omega = 1/\tau$ and then *increases* at 20 db per decade; the plot of ϕ is zero out to $\omega = 0.1/\tau$, increases to 90° at $\omega = 10/\tau$, and then remains constant.

8.3. LOW-FREQUENCY EFFECT OF BYPASS AND COUPLING CAPACITORS

As the frequency of the input signal to an amplifier decreases below the midfrequency range, the voltage (or current) gain ratio decreases in magnitude. The *low-frequency cutoff point* ω_L is the frequency at which the gain ratio equals $1/\sqrt{2}(= 0.707)$ times its midfrequency value [Fig. 8-1(*a*)], or at which M_{db} has decreased by exactly 3 db from its midfrequency value. The range of frequencies below ω_L is called the *low-frequency region*. Low-frequency amplifier performance (attenuation, really) is a consequence of the use of bypass and coupling capacitors to fashion the dc bias characteristics. When viewed from the low-frequency region, such amplifier response is analogous to that of a *high-pass*

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filter (signals for which $\omega < \omega_L$ are appreciably attenuated, whereas higher-frequency signals with $\omega \geq \omega_L$ are unattenuated).

Example 8.5. For the amplifier of Fig. 3-10, assume that $C_C \to \infty$ but that the bypass capacitor C_E cannot be neglected. Also, let $h_{re} = h_{oe} \approx 0$ and $R_i = 0$. Find an expression that is valid for small signals and that gives (*a*) the voltage-gain ratio $A_v(s)$ at any frequency; then find (*b*) the voltage-gain ratio at low frequencies, (*c*) the voltage-gain ratio at higher frequencies, and (*d*) the low-frequency cutoff point. (*e*) Sketch the asymptotic Bode plot for the amplifier (amplitude ratio only).

(*a*) The small-signal low-frequency equivalent circuit (with the approximation implemented) is displayed in Fig. 8-4. In the Laplace domain, we have

$$Z_E = R_E \| \frac{1}{sC_E} = \frac{(R_E)(1/sC_E)}{R_E + 1/sC_E} = \frac{R_E}{sR_EC_E + 1} \tag{8.11}$$

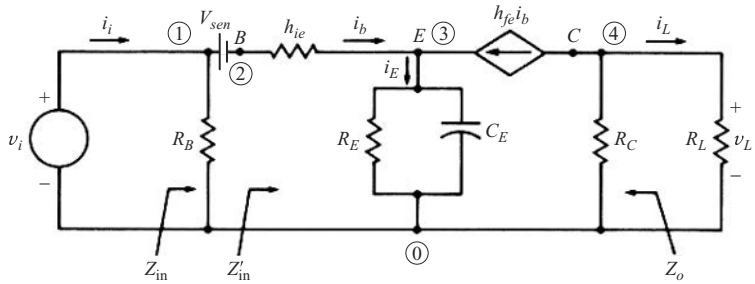


Fig. 8-4

We next note that

$$I_E = I_b + h_{fe}I_b = (h_{fe} + 1)I_b \tag{8.12}$$

Then KVL and (*8.12*) yield

$$V_i = h_{ie}I_b + Z_EI_E = [h_{ie} + (h_{fe} + 1)Z_E]I_b \tag{8.13}$$

But, by Ohm's law,

$$V_L = -(h_{fe}I_b)(R_C \| R_L) = -\frac{h_{fe}R_CR_L}{R_C + R_L} I_b \tag{8.14}$$

Solving (*8.13*) for I_b, substituting the result into (*8.14*), using (*8.11*), and rearranging give the desired voltage-gain ratio:

$$A_v(s) = \frac{V_L}{V_i} = -\frac{h_{fe}R_CR_L}{R_C + R_L} \frac{sR_EC_E + 1}{sR_EC_Eh_{ie} + h_{ie} + (h_{fe} + 1)R_E} \tag{8.15}$$

(*b*) The low-frequency voltage-gain ratio is obtained by letting $s \to 0$ in (*8.15*):

$$A_v(0) = \lim_{s \to 0} \frac{V_L}{V_i} = \frac{-h_{fe}R_CR_L}{(R_C + R_L)[h_{ie} + (h_{fe} + 1)R_E]} \tag{8.16}$$

Comparison of (*8.16*) with (*1*) of Problem 6.7 (but with $h_{oe} = 0$) shows that inclusion of the bypass capacitor in the analysis can significantly change the expression one obtains for the voltage-gain ratio.

(*c*) The higher-frequency (midfrequency) voltage-gain ratio is obtained by letting $s \to \infty$ in (*8.15*):

$$A_v(\infty) = \lim_{s \to \infty} \frac{V_L}{V_i} = \lim_{s \to \infty} \left\{ -\frac{h_{fe}R_CR_L}{R_C + R_L} \frac{R_EC_E + 1/s}{R_EC_Eh_{ie} + [h_{ie} + (h_{fe} + 1)R_E]/s} \right\} = \frac{-h_{fe}R_CR_L}{h_{ie}(R_C + R_L)} \tag{8.17}$$

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(*d*) Equation (*8.15*) can be rearranged to give

$$A_v(s) = \frac{-h_{fe}R_C R_L}{(R_C + R_L)[h_{ie} + (h_{fe} + 1)R_E]} \frac{sR_E C_E + 1}{s\dfrac{R_E C_E h_{ie}}{h_{ie} + (h_{fe} + 1)R_E} + 1} \tag{8.18}$$

which clearly is of the form

$$A_v(s) = k_v \frac{\tau_1 s + 1}{\tau_2 s + 1}$$

Thus, we may use (*8.18*) to write

$$\omega_1 = \frac{1}{\tau_1} = \frac{1}{C_E R_E} \tag{8.19}$$

and

$$\omega_2 = \frac{1}{\tau_2} = \frac{h_{ie} + (h_{fe} + 1)R_E}{R_E C_E h_{ie}} \tag{8.20}$$

Typically, $h_{fe} \gg 1$ and $h_{fe}R_E \gg h_{ie}$, so a reasonable approximation of ω_2 is

$$\omega_2 \approx \frac{1}{C_E h_{ie}/h_{fe}} \tag{8.21}$$

Since h_{ie}/h_{fe} is typically an order of magnitude smaller than R_E, ω_2 is an order of magnitude greater than ω_1, and $\omega_L = \omega_2$.

(*e*) The low- and midfrequency asymptotic Bode plot is depicted in Fig. 8-5, where ω_1 and ω_2 are given by (*8.19*) and (*8.21*), respectively. From (*8.16*) and (*8.17*),

$$M_{dbL} = 20 \log \frac{h_{fe}R_C R_L}{(R_C + R_L)[h_{ie} + (h_{fe} + 1)R_E]} \tag{8.22}$$

and

$$M_{dbM} = 20 \log \frac{h_{fe}R_C R_L}{h_{ie}(R_C + R_L)} \tag{8.23}$$

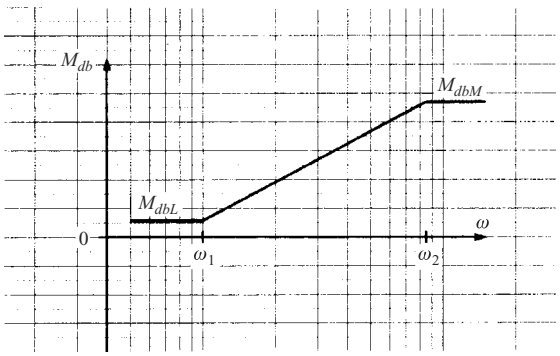


Fig. 8-5

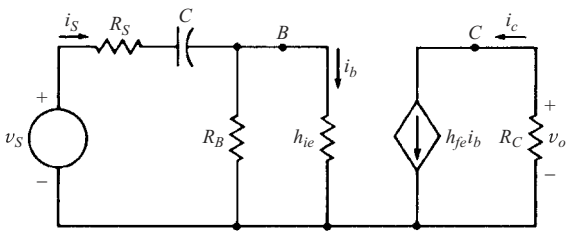


Fig. 8-6

Example 8.6. In the circuit of Fig. 3-20, battery V_S is replaced with a sinusoidal source v_S. The impedance of the coupling capacitor is not negligibly small. (*a*) Find an expression for the voltage-gain ratio $M = |A_v(j\omega)| = |v_o/v_S|$. (*b*) Determine the midfrequency gain of this amplifier. (*c*) Determine the low-frequency cutoff point ω_L, and sketch an asymptotic Bode plot.

(*a*) The small-signal low-frequency equivalent circuit is shown in Fig. 8-6. By Ohm's law,

$$I_S = \frac{V_S}{R_S + h_{ie} \| R_B + 1/sC} \tag{8.24}$$

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Then current division gives

$$I_b = \frac{R_B}{R_B + h_{ie}} I_S = \frac{R_B V_S}{(R_B + h_{ie})(R_S + h_{ie} \| R_B + 1/sC)} \tag{8.25}$$

But Ohm's law requires that

$$V_o = -h_{fe} R_C I_b \tag{8.26}$$

Substituting (*8.25*) into (*8.26*) and rearranging give

$$A(s) = \frac{V_o}{V_S} = \frac{-h_{fe} R_C R_B Cs}{(R_B + h_{ie})[1 + sC(R_S + h_{ie} \| R_B)]} \tag{8.27}$$

Now, with $s = j\omega$ in (*8.27*), its magnitude is

$$M = |A(j\omega)| = \frac{h_{fe} R_C R_B C\omega}{(R_B + h_{ie})\sqrt{1 + (\omega C)^2 (R_S + h_{ie} \| R_B)^2}} \tag{8.28}$$

(*b*) The midfrequency gain follows from letting $s = j\omega \to \infty$ in (*8.27*). We may do so because reactances associated with inherent capacitances have been assumed infinitely large (neglected) in the equivalent circuit. We have, then,

$$A_{\text{mid}} = \frac{-h_{fe} R_C R_B}{(R_B + h_{ie})(R_S + h_{ie} \| R_B)} \tag{8.29}$$

(*c*) From (*8.27*),

$$\omega_L = 1/\tau = \frac{1}{C(R_S + h_{ie} \| R_B)} = \frac{R_B + h_{ie}}{C[R_S(h_{ie} + R_B) + h_{ie} R_B]} \tag{8.30}$$

The asymptotic Bode plot is sketched in Fig. 8-7.

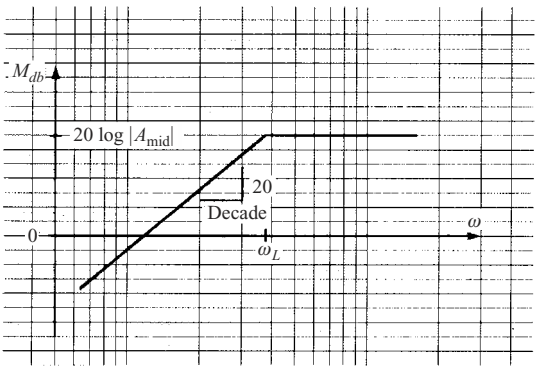


Fig. 8-7

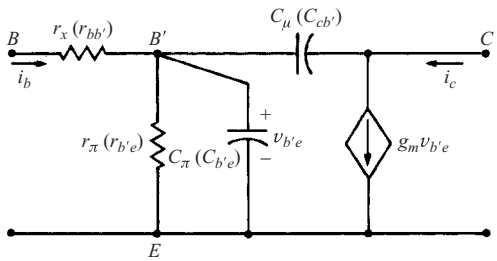


Fig. 8-8 Hybrid-π model for the BJT

8.4. HIGH-FREQUENCY HYBRID-π BJT MODEL

Because of capacitance that is inherent within the transistor, amplifier current- and voltage-gain ratios decrease in magnitude as the frequency of the input signal increases beyond the midfrequency range. The *high-frequency cutoff point* ω_H is the frequency at which the gain ratio equals $1/\sqrt{2}$ times its midfrequency value [see Fig. 8-1(*a*)], or at which M_{db} has decreased by 3 db from its midfrequency value. The range of frequencies above ω_H is called the *high-frequency region*. Like ω_L, ω_H is a break frequency.

The most useful high-frequency model for the BJT is called the *hybrid-π* equivalent circuit (see Fig. 8-8). In this model, the reverse voltage ratio h_{re} and output admittance h_{oe} are assumed negligible. The *base ohmic resistance* $r_{bb'}$, assumed to be located between the base terminal B and the base junction B',

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has a constant value (typically 10 to 50 Ω) that depends directly on the base width. The *base-emitter-junction resistance* $r_{b'e}$ is usually much larger than $r_{bb'}$ and can be calculated as

$$r_{b'e} = \frac{V_T(\beta + 1)}{I_{EQ}} = \frac{V_T \beta}{I_{CQ}} \tag{8.31}$$

(see Problem 6.9). Capacitance C_μ is the depletion capacitance (see Section 2.3) associated with the reverse-biased collector-base junction; its value is a function of V_{BCQ}. Capacitance C_π ($\gg C_\mu$) is the diffusion capacitance associated with the forward-biased base-emitter junction; its value is a function of I_{EQ}.

Example 8.7. Apply the hybrid-π model of Fig. 8-8 to the amplifier of Fig. 3-10 to find an expression for its voltage-gain ratio $A_v(s)$ valid at high frequencies. Assume $R_i = 0$.

The high-frequency hybrid-π, small-signal equivalent circuit is drawn in Fig. 8-9(a). To simplify the analysis, a Thévenin equivalent circuit may be found for the network to the left of terminal pair B', E, with

$$V_{Th} = \frac{r_\pi}{r_\pi + r_x} V_S \tag{8.32}$$

and

$$R_{Th} = r_\pi \| r_x = \frac{r_\pi r_x}{r_\pi + r_x} \tag{8.33}$$

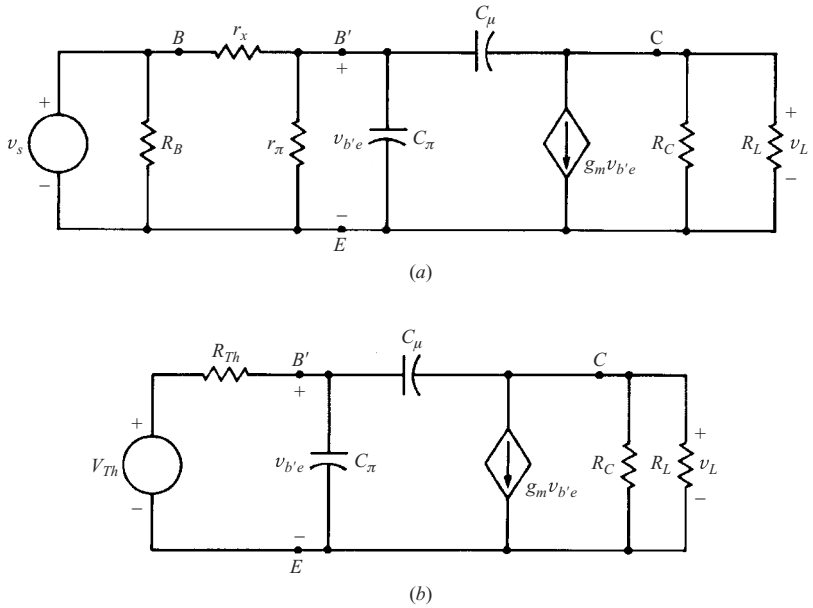


Fig. 8-9

Figure 8-9(b) shows the circuit with the Thévenin equivalent in position. Using $v_{b'e}$ and v_L as node voltages and working in the Laplace domain, we may write the following two equations:

$$\frac{V_{b'e} - V_{Th}}{R_{Th}} + \frac{V_{b'e}}{1/sC_\pi} + \frac{V_{b'e} - V_L}{1/sC_\mu} = 0 \tag{8.34}$$

$$\frac{V_L}{R_C \| R_L} + g_m V_{b'e} + \frac{V_L - V_{b'e}}{1/sC_\mu} = 0 \tag{8.35}$$

The latter equation can be solved for $V_{b'e}$, then substituted into (8.34), and the result rearranged to give the voltage ratio V_{Th}/V_L:

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$$\frac{V_{Th}}{V_L} = \frac{s^2 C_\mu C_\pi R_{Th}(R_C \| R_L) + s[(1 - g_m)C_\mu(R_C \| R_L)] + 1}{(R_C \| R_L)(sC_\mu - g_m)} \tag{8.36}$$

For typical values, the coefficient of s^2 on the right side of (*8.36*) is several orders of magnitude smaller than the other terms; by approximating this coefficient as zero (i.e., neglecting the s^2 term), we neglect a breakpoint at a frequency much greater than ω_H. Doing so and using (*8.32*), we obtain the desired high-frequency voltage-gain ratio:

$$A_v(s) = \frac{V_L}{V_S} = \frac{r_\pi}{r_\pi + r_x} \frac{R_C \| R_L(sC_\mu - g_m)}{s(1 - g_m)C_\mu(R_C \| R_L) + 1} \tag{8.37}$$

8.5. HIGH-FREQUENCY FET MODELS

The small-signal high-frequency model for the FET is an extension of the midfrequency model of Fig. 7-1. Three capacitors are added: C_{gs} between gate and source, C_{gd} between gate and drain, and C_{ds} between drain and source. They are all of the same order of magnitude—typically 1 to 10 pF. Figure 8-10 shows the small-signal high-frequency model based on the current-source model of Fig. 7-1(*a*). Another model, based on the voltage-source model of Fig. 7-1(*b*), can also be drawn.

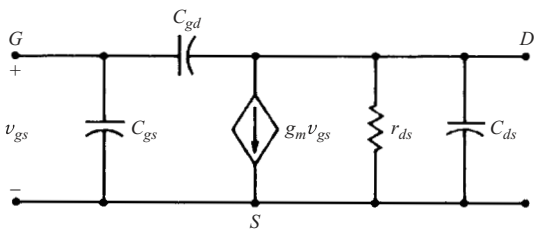


Fig. 8-10 High-frequency small-signal current-source FET model

Example 8.8. For the JFET amplifier of Fig. 4-5(*b*), (*a*) find an expression for the high-frequency voltage-gain ratio $A_v(s)$ and (*b*) determine the high-frequency cutoff point.

(*a*) The high-frequency small-signal equivalent circuit is displayed in Fig. 8-11, which incorporates Fig. 8-10. We first find a Thévenin equivalent for the network to the left of terminal pair a, a'. Noting that $v_{gs} = v_i$, we see that the open-circuit voltage is given by

$$V_{Th} = V_i - \frac{g_m}{sC_{gd}} V_i = \frac{sC_{gd} - g_m}{sC_{gd}} V_i \tag{8.38}$$

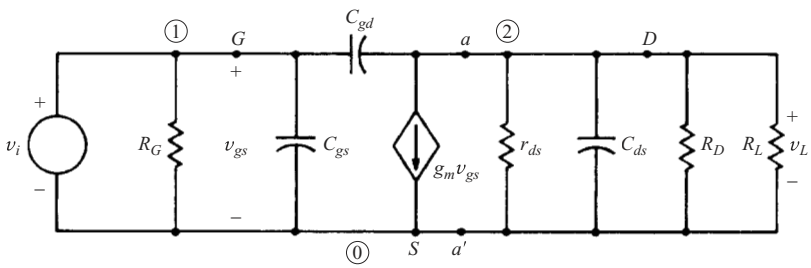


Fig. 8-11

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If V_i is deactivated, $V_i = V_{gs} = 0$ and the dependent current source is zero (open-circuited). A driving-point source connected to a, a' sees only

$$Z_{Th} = \frac{V_{dp}}{I_{dp}} = \frac{1}{sC_{gd}} \tag{8.39}$$

Now, with the Thévenin equivalent in place, voltage division leads to

$$V_L = \frac{Z_{eq}}{Z_{eq} + Z_{Th}} V_{Th} = \frac{1}{1 + Z_{Th}/Z_{eq}} \frac{sC_{gd} - g_m}{sC_{gd}} V_i \tag{8.40}$$

where
$$\frac{1}{Z_{eq}} = Y_{eq} = sC_{ds} + \frac{1}{r_{ds}} + \frac{1}{R_D} + \frac{1}{R_L} = sC_{ds} + g_{ds} + G_D + G_L \tag{8.41}$$

Rearranging (*8.40*) and using (*8.41*), we get

$$A_v(s) = \frac{V_L}{V_i} = \frac{sC_{gd} - g_m}{s(C_{ds} + C_{gd}) + g_{ds} + G_D + G_L} \tag{8.42}$$

(*b*) From (*8.42*), the high-frequency cutoff point is obviously

$$\omega_H = \frac{g_{ds} + G_D + G_L}{C_{ds} + C_{gd}} \tag{8.43}$$

Note that the high-frequency cutoff point is independent of C_{gs} as long as the source internal impedance is negligible. (See Problem 8.40.)

8.6. MILLER CAPACITANCE

High-frequency models of transistors characteristically include a capacitor path from input to ouput, modeled as admittance Y_F in the two-port network of Fig. 8-12(*a*). This added conduction

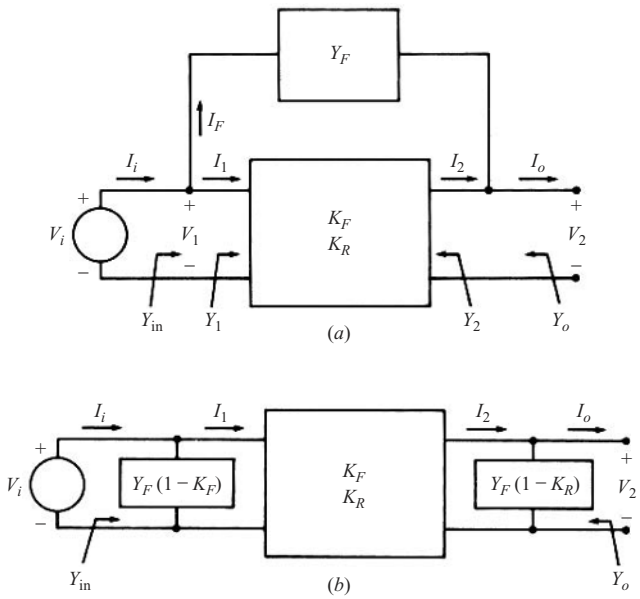


Fig. 8-12

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path generally increases the difficulty of analysis; we would like to replace it with an equivalent shunt element. Referring to Fig. 8-12(*a*) and using KCL, we have

$$Y_{\text{in}} = \frac{I_i}{V_1} = \frac{I_1 + I_F}{V_1} \tag{8.44}$$

But

$$I_F = (V_1 - V_2)Y_F \tag{8.45}$$

Substitution of (*8.45*) into (*8.44*) gives

$$Y_{\text{in}} = \frac{I_1}{V_1} + \frac{(V_1 - V_2)Y_F}{V_1} = Y_1 + (1 - K_F)Y_F \tag{8.46}$$

where $K_F = V_2/V_1$ is obviously the forward voltage-gain ratio of the amplifier.

In a similar manner,

$$Y_o = \frac{-I_o}{V_2} = \frac{-(I_2 + I_F)}{V_2} \tag{8.47}$$

and the use of (*8.45*) in (*8.47*) gives us

$$Y_o = -\left(\frac{I_2}{V_2} + \frac{V_1 - V_2}{V_2}\, Y_F\right) = -[-Y_2 + (K_R - 1)Y_F] = Y_2 + (1 - K_R)Y_F \tag{8.48}$$

where $K_R = V_1/V_2$ is the reverse voltage-gain ratio of the amplifier.

Equations (*8.46*) and (*8.48*) suggest that the feedback admittance Y_F can be replaced with two shunt-connected admittances as shown in Fig. 8-12(*b*). When this two-port network is used to model an amplifier, the voltage gain K_F usually turns out to have a large negative value, so that $(1 - K_F)\, Y_F \approx |K_F|\, Y_F$. Hence, a small feedback capacitance appears as a large shunt capacitance (called the *Miller capacitance*). On the other hand, K_R is typically small so that $(1 - K_R)\, Y_F \approx Y_F$.

8.7. FREQUENCY RESPONSE USING SPICE

SPICE methods offer a frequency sweep option that allows a small-signal, sinusoidal steady-state analysis of a circuit. The frequency sweep is invoked by a control statement of the following format:

.AC DEC *points* *start freq* *end freq*

Node voltages and device currents are inherently complex number values. The magnitudes and phase angles of calculated quantities can be retrieved by the Probe feature of PSpice by appending a *p* and *n*, respectively, to the variable. For example, magnitude and phase angle of the voltage between nodes 2 and 3 are specified by Vm(2,3) and Vp(2,3).

Example 8.9. For the BJT amplifier circuit of Fig. 3-10, assume $C_C \to \infty$. The small-signal equivalent circuit is given by Fig. 8-4 where $R_B = R_1 \| R_2$. Let $h_{oe} = h_{re} = 0$, $h_{fe} = 90$, $R_1 = 1\,\text{k}\Omega$, $R_2 = 16\,\text{k}\Omega$, $R_E = 500\,\Omega$, $C_E = 330\,\mu\text{F}$, $R_C = 1\,\text{k}\Omega$, and $R_L = 10\,\text{k}\Omega$. Use SPICE methods to determine the low-frequency cutoff point.

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The netlist code that follows describes the circuit:

```
Ex8_9.CIR
vi    1 0 AC 0.250V
R1    1 0 1kohm
R2    1 0 16kohm
Vsen 1 2 DC 0V
Rhie 2 3 200ohm
Fhfe 3 4 Vsen 90
RE    3 0 500ohm
CE    3 0 330uF
RC    4 0 1kohm
RL    4 0 10kohm
.AC DEC 25 10Hz 10kHz
.PROBE
.END
```

Execute ⟨Ex8_9.CIR⟩ and use the Probe feature of PSpice to yield the plots of Fig. 8-13. From the marked points, it is seen that the low-frequency cutoff is $f_L = 214.4\,\text{Hz}$, where the voltage gain has a value of $A_{vL} = 289.7$.

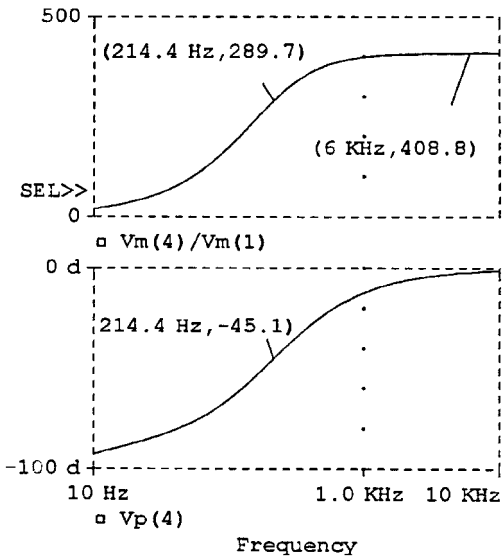


Fig. 8-13

The above example utilized the small-signal equivalent circuit. Small-signal analysis frequency sensitivity can also be implemented using the SPICE model of the transistor directly.

Example 8.10. For the BJT amplifier of Fig. 3-10, let $R_i = R_E = 0$, $R_C = 3\,\text{k}\Omega$, $R_1 = 1\,\text{k}\Omega$, $R_2 = 15\,\text{k}\Omega$, $C_{C1} = C_{C2} = 1\,\mu\text{F}$, and $V_{CC} = 15\,\text{V}$. The transistor can be modeled by the parameters of Example 3.4, except Rb = 10 Ω, Rc = 100 Ω, and Cje = 100 pF. Use SPICE methods to graphically show the voltage gain magnitude and phase angle over the frequency range of 100 Hz to 1 GHz and to determine the low- and high-frequency cutoff points where f_L depends on the value of the bypass capacitor C_E and f_H depends on the BJT junction capacitance values.

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The following netlist code describes the circuit:

```
Ex8_10.CIR
vi  2 0 AC 0.250V
Cc1 2 3 1uF
R2  6 3 15kohm
R1  3 0 1kohm
VCC 6 0 15V
RC  6 4 3kohm
Cc2 4 7 1uF
RL  7 0 5kohm
Q 4  3 0 QPNPG
.MODEL QPNPG PNP(Is=10fA Ikf=150mA Ise=10fA Bf=150
+Br=3 Rb=10ohm Rc=100ohm Va=30V Cjc=10pF Cje=100pF)
.AC DEC 100 100Hz 1GHz
.PROBE
.END
```

Execution of ⟨Ex8_10.CIR⟩ and use of the Probe feature of PSpice results in the plots of Fig. 8-14 where it is seen that the midfrequency range extends from $f_L = 197.3$ Hz to $f_H = 238.3$ MHz.

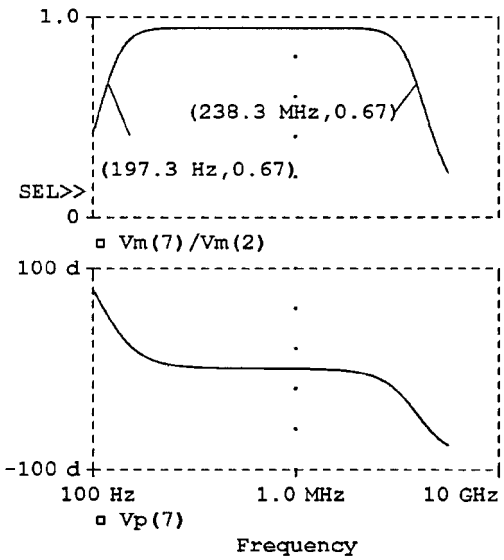


Fig. 8-14

Solved Problems

8.1 Calculate and tabulate the difference between the asymptotic and exact plots of Fig. 8-2, for use in correcting asymptotic plots to exact plots.

The difference ε may be found by subtraction. For the M_{db} plot,

For $0 \le \omega \le \dfrac{1}{\tau}$: $\qquad \varepsilon_{Mdb} = 0 - \{-10 \log [1 + (\omega\tau)^2]\} = 10 \log [1 + (\omega\tau)^2] \qquad (1)$

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For $\omega > \dfrac{1}{\tau}$: $$\varepsilon_{Mdb} = -10\log(\omega\tau)^2 - (-10\log[1+(\omega\tau)^2]) = 10\log[1+1/(\omega\tau)^2] \tag{2}$$

and for the ϕ plot,

For $0 \le \omega \le \dfrac{0.1}{\tau}$: $$\varepsilon_\phi = 0 - (-\tan^{-1}\omega\tau) = \tan^{-1}\omega\tau \tag{3}$$

For $\dfrac{0.1}{\tau} < \omega < \dfrac{10}{\tau}$: $$\varepsilon_\phi = -45^\circ \log 10\omega\tau + \tan^{-1}\omega\tau \tag{4}$$

For $\omega \ge \dfrac{10}{\tau}$: $$\varepsilon_\phi = -90^\circ - (-\tan^{-1}\omega\tau) = \tan^{-1}\omega\tau - 90^\circ \tag{5}$$

Application of (*1*) to (*5*) yields Table 8-1.

Table 8-1 Bode-Plot Corrections

ω	ε_{Mdb}	ε_ϕ
$0.1/\tau$	0.04	5.7°
$0.5/\tau$	1	−4.9°
$0.76/\tau$	2	−2.4°
$1/\tau$	3	0°
$1.32/\tau$	2	2.4°
$2/\tau$	1	4.9°
$10/\tau$	0.04	−5.7°

8.2 The s-domain transfer function for a system can be written in the form

$$T(s) = \frac{K_b(\tau_{z1}s+1)(\tau_{z2}s+1)\cdots}{s^n(\tau_{p1}s+1)(\tau_{p2}s+1)\cdots} \tag{1}$$

where n may be positive, negative, or zero. Show that the Bode plot (for M_{db} only) may be generated as a composite of individual Bode plots for three basic types of terms.

The frequency transfer function corresponding to (*1*) is

$$T(j\omega) = \frac{K_b(1+j\omega\tau_{z1})(1+j\omega\tau_{z2})\cdots}{(j\omega)^n(1+j\omega\tau_{p1})(1+j\omega\tau_{p2})\cdots} \tag{2}$$

From definition 3 of Section 8.2,

$$M_{db} = 20\log|T(j\omega)| = 20\log\left[\frac{K_b|1+j\omega\tau_{z1}||1+j\omega\tau_{z2}|\cdots}{|(j\omega)^n||1+j\omega\tau_{p1}||1+j\omega\tau_{p2}|\cdots}\right] \tag{3}$$

which may be written as

$$\begin{aligned} M_{db} = {} & 20\log K_b + 20\log|1+j\omega\tau_{z1}| + 20\log|1+j\omega\tau_{z2}| + \cdots \\ & - 20n\log|j\omega| - 20\log|1+j\omega\tau_{p1}| - 20\log|1+j\omega\tau_{p2}| - \cdots \end{aligned} \tag{4}$$

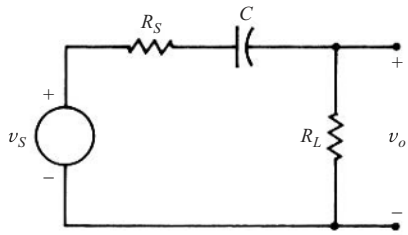
It is apparent from (*4*) that the Bode plot of $T(j\omega)$ can be formed by point-by-point addition of the plots of three types of terms:

1. A frequency-invariant or gain-constant term K_b whose Bode plot is a horizontal line at $M_{db} = 20\log K_b$.

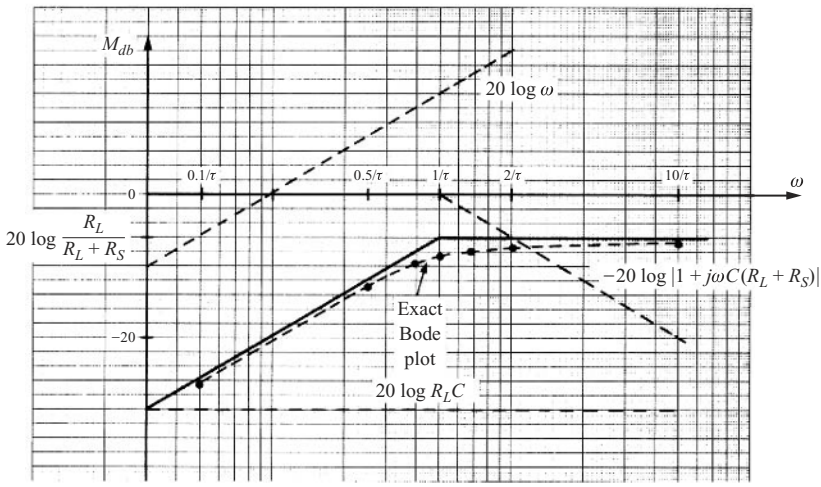
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2. Poles or zeros of multiplicity n, $(j\omega)^{\pm n}$, whose amplitude ratio is $M_{db} = \pm 20n \log \omega$, where the plus sign corresponds to zeros and the minus sign to poles of the transfer function. (See Example 8.3.)
3. First-order lead and lag factors, $(1 + j\omega\tau)^{\pm n}$, as discussed in Examples 8.1 and 8.2. They are usually approximated with asymptotic Bode plots; if greater accuracy is needed, the asymptotic plots are corrected using Table 8-1.

8.3 The circuit of Fig. 8-15(a) is driven by a sinusoidal source v_S. (a) Sketch the asymptotic Bode plot (M_{db} only) associated with the Laplace-domain transfer function $T(s) = V_o/V_S$. (b) Use Table 8-1 to correct asymptotic plot, so as to show the exact Bode plot.



(a)



(b)

Fig. 8-15

(a) By voltage division,

$$V_o = \frac{R_L}{R_L + R_S + 1/sC} V_S \tag{1}$$

so that

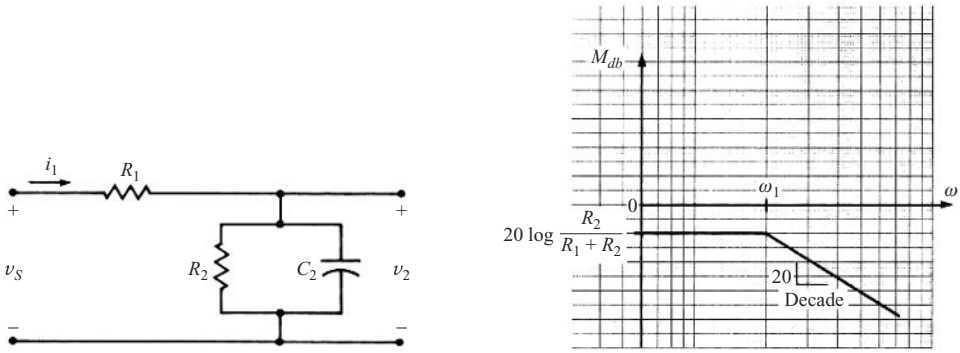
$$\frac{V_o}{V_S} = \frac{sR_L C}{1 + sC(R_L + R_S)} = \frac{K_b s}{1 + \tau s} \tag{2}$$

Using the result of Problem 8.2, we recognize (2) as the combination of a first-order lag, a constant gain, and a zero of multiplicity 1. The components of the asymptotic Bode plot are shown dashed in Fig. 8-15(b), and the composite is solid. For purposes of illustration, it was assumed that $1/[C(R_L + R_S)] > 1$, which is true in most cases.

(b) The correction factors of Table 8-1 lead to the exact Bode plot as drawn in Fig. 8-15(b).

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8.4 Sketch the asymptotic Bode plot (M_{db} only) associated with the output-to-input voltage ratio of the circuit in Fig. 8-16(*a*).



(*a*) (*b*)

Fig. 8-16

By voltage division,

$$V_2 = \frac{R_2 \| (1/sC_2)}{R_1 + R_2 + 1/sC_2} V_s = \frac{\dfrac{R_2}{sR_2C_2+1}}{R_1 + \dfrac{R_2}{sR_2C_2+1}} V_s$$

and the Laplace-domain transfer function is

$$T(s) = \frac{V_2}{V_S} = \frac{R_2/(R_1+R_2)}{s\left(\dfrac{R_1R_2}{R_1+R_2}\right)C+1} = \frac{K_b}{sR_{eq}C_2+1}$$

From $T(s)$, it is apparent that the circuit forms a low-pass filter with low-frequency gain $T(0) = R_2/(R_1+R_2)$ and a corner frequency at $\omega_1 = 1/\tau_1 = 1/R_{eq}C_2$. Its Bode plot is sketched in Fig. 8-16(*b*).

8.5 For the amplifier of Fig. 3-10, assume that $C_C \to \infty$, $h_{re} = h_{oe} = 0$, and $R_i = 0$. The bypass capacitor C_E cannot be neglected. Find expressions for (*a*) the current-gain ratio $A_i(s)$, (*b*) the current-gain ratio at low frequencies, and (*c*) the midfrequency current-gain ratio. (*d*) Determine the low-frequency cutoff point, and sketch the asymptotic Bode plot (M_{db} only).

(*a*) The small-signal low-frequency equivalent circuit is given in Fig. 8-4. By current division for Laplace-domain quantities,

$$I_b = \frac{R_B}{R_B + h_{ie} + Z_E} I_i \tag{1}$$

where

$$Z_E = R_E \| \frac{1}{sC_E} = \frac{R_E}{sR_EC_E+1} \tag{2}$$

Also

$$I_L = \frac{-R_C}{R_C + R_L} h_{fe} I_b \tag{3}$$

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Substitution of (*1*) into (*3*) gives the current-gain ratio as

$$\frac{I_L}{I_i} = \frac{-R_C}{R_C + R_L} \frac{h_{fe} R_B}{R_B + h_{ie} + Z_E} \tag{4}$$

Using (*2*) in (*4*) and rearranging leads to the desired current-gain ratio:

$$A_i(s) = \frac{I_L}{I_i} = \frac{\dfrac{-h_{fe} R_C R_B}{(R_C + R_L)(R_E + R_B + h_{ie})} (sR_E C_E + 1)}{s \dfrac{R_E C_E (R_B + h_{ie})}{R_E + R_B + h_{ie}} + 1} \tag{5}$$

(*b*) The low-frequency current-gain ratio follows from letting $s \to 0$ in (*5*):

$$A_i(0) = \lim_{s \to 0} \frac{I_L}{I_i} = \frac{-h_{fe} R_C R_B}{(R_C + R_L)(R_E + R_B + h_{ie})} \tag{6}$$

(*c*) The midfrequency current-gain ratio is obtained by letting $s \to \infty$ in (*5*):

$$A_i(\infty) = \lim_{s \to \infty} \frac{I_L}{I_i} = \frac{-h_{fe} R_C R_B}{(R_C + R_L)(R_B + h_{ie})} \tag{7}$$

(*d*) Inspection of (*5*) shows that the Laplace-domain transfer function is of the form

$$A_i(s) = K_b \frac{\tau_1 s + 1}{\tau_2 s + 1}$$

where $$\omega_1 = \frac{1}{\tau_1} = \frac{1}{R_E C_E} \quad \text{and} \quad \omega_2 = \frac{1}{\tau_2} = \frac{R_E + R_B + h_{ie}}{R_E C_E (R_B + h_{ie})} \tag{8}$$

With ω_1 and ω_2 as given by (*8*) and with

$$M_{dbL} = 20 \log A_i(0) \quad \text{and} \quad M_{dbM} = 20 \log A_i(\infty)$$

the Bode plot is identical to that of Fig. 8-5. Since $\omega_2 > \omega_1$, ω_2 is closer to the midfrequency region and thus is the low-frequency cutoff point.

8.6 In the amplifier of Fig. 3-10, $C_C \to \infty$, $R_i = 0$, $R_E = 1\,\text{k}\Omega$, $R_1 = 3.2\,\text{k}\Omega$, $R_2 = 17\,\text{k}\Omega$, $R_L = 10\,\text{k}\Omega$, and $h_{oe} = h_{re} = 0$. The transistors used are characterized by $75 \le h_{fe} \le 100$ and $300 \le h_{ie} \le 1000\,\Omega$. (*a*) By proper selection of R_C and C_E, design an amplifier with low-frequency cutoff $f_L \le 200\,\text{Hz}$ and high-frequency voltage gain $|A_v| \ge 50$. (*b*) For the finished design, determine the low-frequency voltage-gain ratio if h_{ie} and h_{fe} have median values.

(*a*) According to (*8.17*), the worst-case transistor parameters for high $A_v(\infty)$ are minimum h_{fe} and maximum h_{ie}. Using those parameter values allows us to determine a value for the parallel combination of R_C and R_L:

$$R_{eq} = R_C \| R_L \ge |A_v(\infty)| \frac{h_{ie}}{h_{fe}} = 50 \frac{1000}{75} = 666.7\,\Omega$$

Then $$R_C = \frac{R_{eq} R_L}{R_L - R_{eq}} \ge \frac{(666.7)(10{,}000)}{9333.3} = 714.3\,\Omega$$

Now, from (*8.20*), for $f_L \le 200\,\text{Hz}$,

$$C_E \ge \frac{h_{ie} + (h_{fe} + 1) R_E}{\omega_L R_E h_{ie}} = \frac{300 + (101)(1000)}{2\pi(200)(1000)(300)} = 268.7\,\mu\text{F}$$

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(*b*) By (*8.16*),

$$A_v(0) = -\frac{h_{fe}R_{eq}}{h_{ie} + (h_{fe}+1)R_E} = -\frac{\left(\frac{100+75}{2}\right)(666.7)}{\frac{300+1000}{2} + \left(\frac{100+75}{2}+1\right)(1000)} = -0.654$$

8.7 Let $C_1, C_E \to \infty$ in the capacitor-coupled amplifier of Fig. 6-22. Assume $h_{oe1} = h_{re1} = h_{oe2} = h_{re2} = 0$. Find an expression for the voltage-gain ratio $A_v(s)$.

The first-stage amplifier can be replaced with a Thévenin equivalent, and the second stage represented by its input impedance, as shown in Fig. 8-17. A_v' follows from voltage division and (*6.46*) if R_L, h_{fe}, and h_{ie} are replaced with R_{C1}, h_{fe1}, and h_{ie1}, respectively:

$$A_v' = \frac{R_{eq}}{R_{eq}+R_i}\,\frac{-h_{fe1}R_{C1}}{h_{ie1}} = -\frac{h_{fe1}R_{C1}R_{eq}}{h_{ie1}(R_{eq}+R_i)} \tag{1}$$

where
$$R_{eq} = h_{ie1} \| R_{B1} = h_{ie1} \| R_{11} \| R_{12} = \frac{h_{ie1}R_{11}R_{12}}{h_{ie1}(R_{11}+R_{12}) + R_{11}R_{12}} \tag{2}$$

Z_{o1} is given by (*6.50*) with h_{oe} replaced with R_{C1} (and with $h_{re1} = h_{oe1} = 0$):

$$Z_{o1} = R_{C1} \tag{3}$$

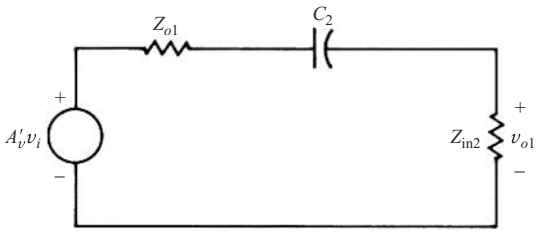


Fig. 8-17

The second-stage input impedance is given by (*6.47*) if h_{ie} is replaced with $h_{ie2} \| R_{B2} = h_{ie2} \| R_{21} \| R_{22}$:

$$Z_{\text{in2}} = \frac{h_{ie2}R_{B2}}{h_{ie2}+R_{B2}} = \frac{h_{ie2}R_{21}R_{22}}{h_{ie2}(R_{21}+R_{22}) + R_{21}R_{22}} \tag{4}$$

Now, from (*2*) of Problem 8.3,

$$\frac{V_{o1}}{A_v'V_i} = \frac{sZ_{\text{in2}}C_2}{sC_2(Z_{\text{in2}}+Z_{o1})+1} \tag{5}$$

and rearranging yields the first-stage gain as

$$A_{v1} = \frac{V_{o1}}{V_i} = A_v'\,\frac{sZ_{\text{in2}}C_2}{sC_2(Z_{\text{in2}}+Z_{o1})+1} \tag{6}$$

The second-stage gain follows directly from (*6.46*) if R_L is replaced with R_{C2}:

$$A_{v2} = -\frac{h_{fe2}R_{C2}}{h_{ie2}}$$

Consequently, the overall gain is

$$A_v = A_{v1}A_{v2} = -A_v'\,\frac{sZ_{\text{in}}C_2}{sC_2(Z_{\text{in2}}+Z_{o1})+1}\,\frac{h_{fe2}R_{C2}}{h_{ie2}} \tag{7}$$

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Substituting (*1*) into (*7*) and simplifying yield the desired gain:

$$A_v(s) = \frac{h_{fe1}h_{fe2}R_{C1}R_{C2}R_{eq}}{h_{ie1}h_{ie2}(R_{eq}+R_i)} \frac{sZ_{\text{in2}}C_2}{sC_2(Z_{\text{in2}}+Z_{o1})+1} \tag{8}$$

8.8 In the cascaded amplifier of Problem 8.7 (Fig. 6-22 with $C_1, C_E \to \infty$), let $h_{ie1} = h_{ie2} = 1500\,\Omega$, $h_{fe1} = h_{fe2} = 40$, $C_2 = 1\,\mu\text{F}$, $R_i = 1\text{k}\Omega$, $R_{C1} = 10\,\text{k}\Omega$, $R_{C2} = 20\,\text{k}\Omega$, and $R_{B1} = R_{B2} = 5\,\text{k}\Omega$. Determine (*a*) the low-frequency gain, (*b*) the midfrequency gain, and (*c*) the low-frequency cutoff point.

(*a*) Letting $s \to 0$ in (*8*) of Problem 8.7 makes apparent the fact that the low-frequency gain $A_v(0) = 0$.

(*b*) The midfrequency gain is determined by letting $s \to \infty$ in (*8*) of Problem 8.7:

From (*2*), (*3*), and (*4*) of Problem 8.7,

$$A_v(\infty) = \lim_{s\to\infty} A_v(s) = \frac{h_{fe1}h_{fe2}R_{C1}R_{C2}R_{eq}}{h_{ie1}h_{ie2}(R_{eq}+R_i)} \frac{Z_{\text{in2}}}{Z_{\text{in2}}+Z_{o1}}$$

$$R_{eq} = \frac{h_{ie1}R_{B1}}{h_{ie1}+R_{B1}} = \frac{(1500)(5000)}{6500} = 1153.8\,\Omega$$

$$Z_{o1} = R_{C1} = 10\,\text{k}\Omega$$

and

$$Z_{\text{in2}} = \frac{h_{ie2}R_{B2}}{h_{ie2}+R_{B2}} = \frac{(1500)(5000)}{6500} = 1153.8\,\Omega$$

Then

$$A_v(\infty) = \frac{(40)(40)(10\times10^3)(20\times10^3)(1153.8)}{(1500)(1500)(2153.8)} \frac{1153.8}{1153.8+10\times10^3} = 7881.3$$

(*c*) The low-frequency cutoff point is computed from the lag term in (*8*) of Problem 8.7:

$$f_L = \frac{\omega_L}{2\pi} = \frac{1}{2\pi C_2(Z_{\text{in2}}+Z_{o1})} = \frac{1}{2\pi(1\times10^{-6})(1153.8+10\times10^3)} = 14.3\,\text{Hz}$$

8.9 The two coupling capacitors in the CB amplifier of Fig. 6-15 are identical and cannot be neglected. Assume $h_{rb} = h_{ob} = 0$. (*a*) Find an expression for the voltage-gain ratio V_L/V_S. (*b*) Find an expression for the midfrequency voltage-gain ratio.

(*a*) The small-signal low-frequency equivalent circuit is given in Fig. 8-18. Applying Ohm's law in the Laplace domain, we obtain

$$I_S = \frac{V_S}{1/sC_C + R_E h_{ib}/(R_E+h_{ib})} = \frac{sC_C V_S}{sC_C R_E h_{ib}/(R_E+h_{ib})+1}$$

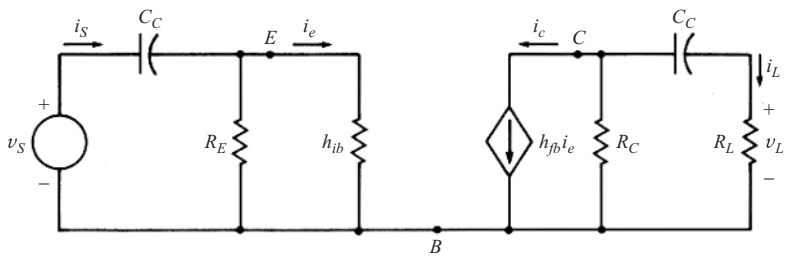


Fig. 8-18

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Voltage division then gives

$$I_e = \frac{R_E}{h_{ib} + R_E} I_S = \frac{R_E}{h_{ib} + R_E} \frac{sC_C}{sC_C R_E h_{ib}/(R_E + h_{ib}) + 1} V_S \tag{1}$$

By current division at the output,

$$V_L = R_L I_L = -R_L \frac{R_C}{R_C + 1/sC_C + R_L} h_{fb} I_e = -\frac{sh_{fb} R_L R_C C_C I_e}{sC_C(R_L + R_C) + 1} \tag{2}$$

Substituting (*1*) into (2) and rearranging lead to the desired voltage-gain ratio:

$$A_v(s) = \frac{V_L}{V_S} = -\frac{R_E R_L R_C h_{fb} C_C^2 s^2}{(h_{ib} + R_E)[sC_C R_E h_{ib}/(R_E + h_{ib}) + 1][sC_C(R_L + R_C) + 1]} \tag{3}$$

(*b*) Letting $s \to \infty$ in (*3*) leads to the midfrequency gain:

$$A_v(\infty) = -\frac{R_L R_C h_{fb}}{h_{ib}(R_L + R_C)} \tag{4}$$

8.10 The two coupling capacitors in the CB amplifier of Fig. 6-15 are identical. Also, $h_{rb} = h_{ob} = 0$. (*a*) Find an expression for the current-gain ratio $A_i(s)$ that is valid at any frequency. (*b*) Find an expression for the midfrequency current-gain ratio.

(*a*) The low-frequency equivalent circuit is displayed in Fig. 8-18. By current division,

$$I_e = \frac{R_E}{h_{ib} + R_E} I_S \tag{1}$$

and

$$I_L = -\frac{R_C}{R_C + 1/sC_C + R_L} h_{fb} I_e = -\frac{sh_{fb} R_L R_C C_C I_e}{sC_C(R_L + R_C) + 1} \tag{2}$$

Substituting (*1*) into (*2*) and dividing by I_S give the desired current-gain ratio:

$$A_i(s) = \frac{I_L}{I_i} = -\frac{sh_{fb} R_L R_C R_E C_C}{(h_{ib} + R_E)[sC_C(R_L + R_C) + 1]} \tag{3}$$

(*b*) The midfrequency current-gain ratio is found by letting $s \to \infty$ in (*3*):

$$A_i(\infty) = -\frac{h_{fb} R_L R_C R_E}{(h_{ib} + R_E)(R_L + R_C)} \tag{4}$$

8.11 On a common set of axes, sketch the asymptotic Bode plots (M_{db} only) for the voltage- and current-gain ratios of the CB amplifier of Fig. 6-15, and then correct them to exact plots. Assume that the coupling capacitors are identical and that, for typical values, $1 \ll C_C(R_E \| h_{ib}) \ll C_C(R_L + R_E)$.

The Laplace-domain transfer functions that serve as bases for Bode plots of the voltage- and current-gain ratios are, respectively, (*3*) of Problem 8.9 and (*3*) of Problem 8.10. Under the given assumptions, inspection shows that the two transfer functions share a break frequency at $\omega = 1/[C_C(R_L + R_C)]$ and the voltage-gain transfer function has another at a higher frequency. Moreover, the voltage plot rises at 40 db per decade to its first break point, and the current plot at 20 db per decade. With

$$\omega_{1v} = \omega_{1i} = \omega_{Li} = \frac{1}{C_C(R_L + R_C)} \qquad \text{and} \qquad \omega_{2v} = \omega_{Lv} = \frac{R_E + h_{ib}}{C_C R_E h_{ib}}$$

the low-frequency asymptotic Bode plots of voltage and current gain are sketched in Fig. 8-19. The given assumption assures a separation of at least a decade between ω_{1v} and ω_{2v} and between $\omega = 1$ and ω_{1v}. Since the parameter values are not known, the sketches were made under the assumption that $K_b = 1$ in both plots. When values become known, the Bode plots must be shifted upward by

$$20 \log K_{bv} = 20 \log \frac{R_E R_L R_C h_{fb} C_C^2}{h_{ib} + R_E} \quad \text{for the voltage plot}$$

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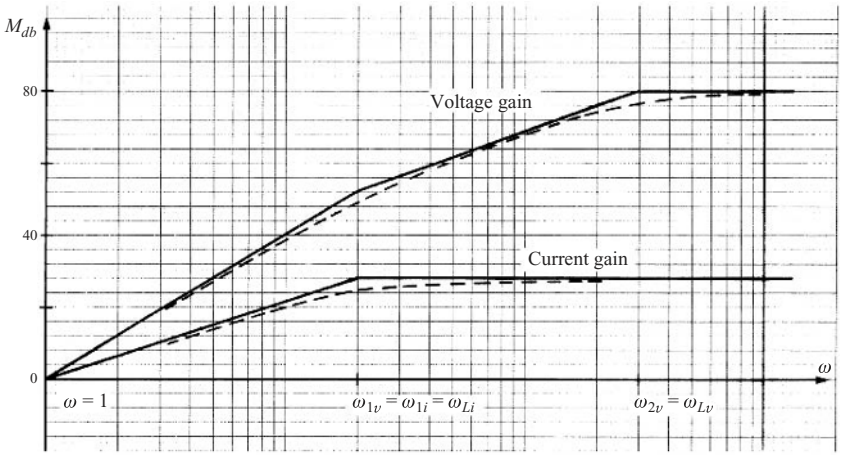


Fig. 8-19

and $$20 \log K_{bi} = 20 \log \frac{h_{fb} R_L R_C R_E C_C}{h_{ib} + R_E} \quad \text{for the current plot}$$

Correction of the asymptotic plot requires only the application of Table 8-1. The exact plots are shown dashed.

8.12 For the CE amplifier of Fig. 3-10, determine (*a*) Z'_{in}, (*b*) Z_{in}, and (*c*) Z_o if $C_C \to \infty$ but C_E cannot be neglected.

(*a*) The small-signal low-frequency equivalent circuit is given in Fig. 8-4. Using (*8.11*) and (*8.13*), we have

$$Z'_{\text{in}} = \frac{V_i}{I_b} = h_{ie} + (h_{fe} + 1) Z_E = \frac{s h_{ie} R_E C_E + h_{ie} + (h_{fe} + 1) R_E}{s R_E C_E + 1} \tag{1}$$

(*b*) $$Z_{\text{in}} = R_B \| Z'_{\text{in}} = \frac{R_B Z'_{\text{in}}}{R_B + Z'_{\text{in}}} \tag{2}$$

Substituting (*1*) into (*2*) and rearranging give

$$Z_{\text{in}} = \frac{R_B [s h_{ie} R_E C_E + h_{ie} + (h_{fe} + 1) R_E]}{s R_E C_E (R_B + h_{ie}) + R_B + h_{ie} + (h_{fe} + 1) R_E} \tag{3}$$

(*c*) With voltage source v_i deactivated (shorted), KVL requires that

$$I_b = \frac{-h_{fe} I_b (Z_E \| h_{ie})}{h_{ie}}$$

so that $$\left[1 + \frac{h_{fe} Z_E h_{ie}}{h_{ie}(Z_E + h_{ie})}\right] I_b = 0 \tag{4}$$

Since (*4*) can be satisfied in general only by $I_b = 0$, the output impedance is simply

$$Z_o = R_C \tag{5}$$

In this particular case, (*3*) shows that the input impedance is frequency-dependent, while (*5*) shows that the output impedance is independent of frequency. In general, however, the output impedance does depend on frequency, through a finite-valued coupling capacitor C_C. (See Problem 8.13.)

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8.13 To examine the combined effects of coupling and bypass capacitors, let the input coupling capacitor be infinitely large while the output coupling capacitor and the bypass capacitor have practical values in the CE amplifier of Fig. 3-10. For simplicity, assume $h_{re} = h_{oe} = 0$ and $R_B \gg Z'_{\text{in}}$. (*a*) Find the voltage-gain ratio $A_v(s) = v_L/v_i$. (*b*) If $C_E = 200\,\mu\text{F}$, $C_C = 10\,\mu\text{F}$, $R_i = R_E = 100\,\Omega$, $R_C = R_L = 2\,\text{k}\Omega$, $h_{ie} = 1\,\text{k}\Omega$, and $h_{fe} = 100$, determine what parameters control the low-frequency cutoff point and whether it is below 100 Hz. (*c*) Find an expression for the output impedance Z_o.

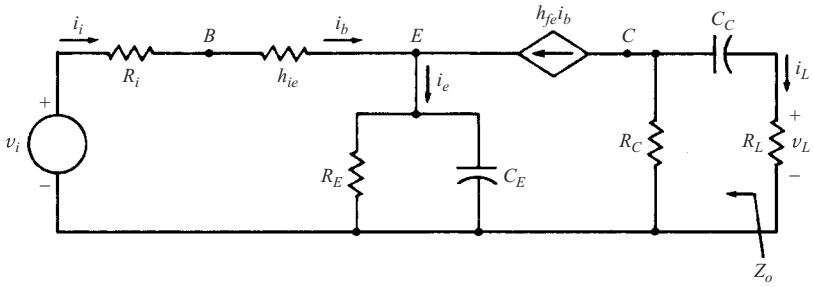


Fig. 8-20

(*a*) The small-signal equivalent circuit is given in Fig. 8-20. We first define

$$Z_E = R_E \| \frac{1}{sC_E} = \frac{R_E}{sR_EC_E + 1} \tag{1}$$

Then, by KCL,

$$I_e = I_b + h_{fe}I_b = (h_{fe} + 1)I_b \tag{2}$$

KVL around the input mesh requires that

$$V_i = (R_i + h_{ie})I_b + Z_EI_e \tag{3}$$

Substituting (*2*) into (*3*) and solving for I_b yields

$$I_b = \frac{V_i}{R_i + h_{ie} + (h_{fe} + 1)Z_E} \tag{4}$$

Current division at the collector node gives

$$I_L = -\frac{R_C}{R_C + R_L + 1/sC_C}\,h_{fe}I_b \tag{5}$$

and Ohm's law and (*5*) yield

$$V_L = R_LI_L = -\frac{R_LR_C}{R_C + R_L + 1/sC_C}\,h_{fe}I_b \tag{6}$$

Substituting (*4*) and (*1*) into (*6*) and rearranging now lead to the desired voltage-gain ratio:

$$A_v(s) = \frac{V_L}{V_i} = -\frac{\dfrac{h_{fe}R_LR_CC_C}{(h_{fe} + 1)R_E + h_{ie} + R_i}\,s(sR_EC_E + 1)}{[sC_C(R_C + R_L) + 1]\left[s\,\dfrac{C_ER_E(R_i + h_{ie})}{(h_{fe} + 1)R_E + R_i + h_{ie}} + 1\right]} \tag{7}$$

(*b*) The Laplace-domain transfer function (*7*) is of the form

$$T(s) = \frac{-K_bs(\tau_2s + 1)}{(\tau_1s + 1)(\tau_3s + 1)}$$

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where
$$\omega_1 = \frac{1}{\tau_1} = \frac{1}{C_C(R_C + R_L)} = \frac{1}{(10 \times 10^{-6})(4000)} = 25\,\text{rad/s}$$
$$\omega_2 = \frac{1}{\tau_2} = \frac{1}{R_E C_E} = \frac{1}{(100)(200 \times 10^{-6})} = 50\,\text{rad/s}$$
$$\omega_3 = \frac{1}{\tau_3} = \frac{(h_{fe}+1)R_E + R_i + h_{ie}}{C_E R_E (R_i + h_{ie})} = \frac{(101)(100) + 100 + 1000}{(200 \times 10^{-6})(100)(1100)} = 509.1\,\text{rad/s}$$

Since there is at least a decade of frequency (in which the gain can attenuate from its midfrequency value) between ω_3 and the other (lower) break frequencies, ω_3 must be the low-frequency cutoff ω_L. Then

$$f_L = \frac{\omega_3}{2\pi} = \frac{509.1}{2\pi} = 81.02\,\text{Hz} < 100\,\text{Hz}$$

(*c*) As in Problem 8.12, $I_b = 0$ if v_i is deactivated; a driving-point source replacing R_L would then see a frequency-dependent output impedance given by

$$Z_o = Z_{dp} = R_C + \frac{1}{sC_C} \tag{8}$$

8.14 Assume that the coupling capacitors in the CS MOSFET amplifier of Fig. 4-25 are identical. Determine the voltage-gain ratio (*a*) for any frequency and (*b*) for midfrequency operation.

(*a*) The equivalent circuit is drawn in Fig. 8-21. By voltage division,

$$V_{gs} = \frac{R_G}{R_G + 1/sC_C} V_i = \frac{sR_G C_C}{sR_G C_C + 1} V_1 \qquad \text{where} \qquad R_G = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{1}$$

Current division at the drain node yields

$$I_L = -\frac{R_D \| r_{ds}}{R_D \| r_{ds} + 1/sC_C + R_L} g_m V_{gs} = -\frac{sC_C[R_D r_{ds}/(R_D + r_{ds})]g_m V_{gs}}{sC_C[R_D r_{ds}/(R_D + r_{ds}) + R_L] + 1} \tag{2}$$

from which

$$V_o = R_L I_L = -\frac{sg_m R_D R_L r_{ds} C_C/(R_D + r_{ds})}{sC_C[R_D r_{ds}/(R_D + r_{ds}) + R_L] + 1} V_{gs} \tag{3}$$

Substitution of (*1*) into (*3*) and rearrangement then give

$$A_v(s) = \frac{V_o}{V_i} = -\frac{s^2 g_m R_G R_D R_L r_{ds} C_C^2/(R_D + r_{ds})}{\left[sC_C\left(\dfrac{R_D r_{ds}}{R_D + r_{ds}} + R_L\right) + 1\right][sC_C R_G + 1]} \tag{4}$$

(*b*) Since high-frequency capacitances have not been modeled, the midfrequency gain follows from letting $s \to \infty$ in (*4*):

$$A_{\text{mid}} = A_v(\infty) = -\frac{g_m R_D R_L r_{ds}}{R_D r_{ds} + R_L(R_D + r_{ds})}$$

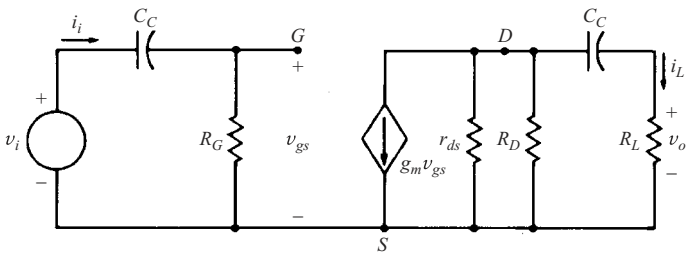


Fig. 8-21

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8.15 For the CS JFET amplifier of Fig. 7-2, (*a*) find an expression for the voltage-gain ratio $A_v(s)$ and (*b*) determine the low-frequency cutoff point.

(*a*) The low-frequency equivalent circuit is shown in Fig. 8-22. By KVL,

$$I_d = \frac{\mu V_{gs}}{(R_S \| 1/sC_S) + r_{ds} + R_D} = \frac{\mu(sR_SC_S + 1)V_{gs}}{sC_SR_S(R_D + r_{ds}) + R_S + R_D + r_{ds}} \tag{1}$$

But KVL requires that

$$V_{gs} = V_i - I_D\left(R_S \| \frac{1}{sC_S}\right) = V_i - \frac{R_S I_D}{sR_SC_S + 1} \tag{2}$$

Substituting (*1*) into (*2*) and solving for V_{gs} give

$$V_{gs} = \frac{sC_SR_S(R_D + r_{ds}) + R_S + R_D + r_{ds}}{sC_SR_S(R_D + r_{ds}) + R_D + r_{ds} + (\mu + 1)R_S} V_i \tag{3}$$

Now, by Ohm's law and (*1*),

$$V_o = -R_D I_D = -\frac{\mu R_D(sR_SC_S + 1)V_{gs}}{sC_SR_S(R_D + r_{ds}) + R_S + R_D + r_{ds}} \tag{4}$$

Substituting V_{gs} as given by (*3*) into (*4*) and rearranging yield, finally,

$$A_v(s) = \frac{V_o}{V_i} = -\frac{\mu R_D}{R_D + r_{ds} + (\mu + 1)R_S} \frac{sR_SC_S + 1}{s\dfrac{C_SR_S(R_D + r_{ds})}{R_D + r_{ds} + (\mu + 1)R_S} + 1} \tag{5}$$

(*b*) It is apparent that the low-frequency cutoff is the larger of the two break frequencies; from (*5*), it is

$$\omega_L = \frac{R_D + r_{ds} + (\mu + 1)R_S}{C_SR_S(R_D + r_{ds})}$$

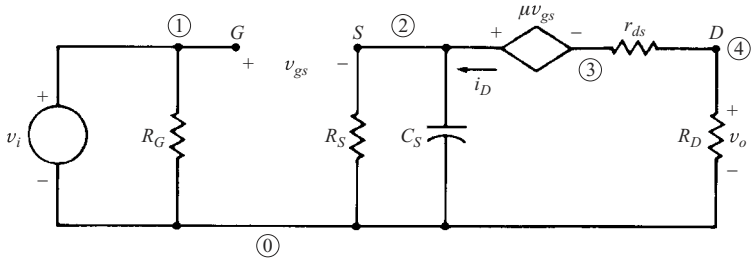


Fig. 8-22

8.16 The hybrid-π equivalent circuit for the CE amplifier of Fig. 3-10 with the output shorted is shown in Fig. 8-23. (*a*) Find an expression for the so-called *β cutoff frequency* f_β, which is simply the high-frequency current-gain cutoff point of the transistor with the collector and emitter terminals shorted. (*b*) Evaluate f_β if $r_x = 100\,\Omega$, $r_\pi = 1\,\text{k}\Omega$, $C_\mu = 3\,\text{pF}$, and $C_\pi = 100\,\text{pF}$.

(*a*) Ohm's law gives

$$V_{b'e} = \frac{I_b}{g_\pi + s(C_\pi + C_\mu)} \qquad \text{where} \qquad g_\pi = \frac{1}{r_\pi} \tag{1}$$

But with the collector and emitter terminals shorted,

$$I_L = -g_m V_{b'e} \tag{2}$$

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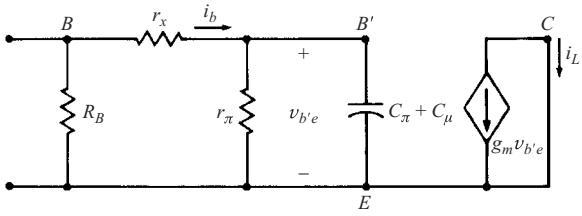


Fig. 8-23

Substituting (*1*) into (*2*) and rearranging give the current-gain ratio

$$\frac{I_L}{I_b} = -\frac{g_m}{g_\pi + s(C_\pi + C_\mu)} = -\frac{g_m r_\pi}{s r_\pi (C_\pi + C_\mu) + 1} \tag{3}$$

From (*3*), the β cutoff frequency is seen to be

$$f_\beta = \frac{\omega_\beta}{2\pi} = \frac{1}{2\pi r_\pi (C_\pi + C_\mu)} \tag{4}$$

(*b*) Substituting the given high-frequency parameters in (*4*) yields

$$f_\beta = \frac{1}{2\pi(1000)(103 \times 10^{-12})} = 1.545\,\text{MHz}$$

8.17 Apply the hybrid-π high-frequency model to the CB amplifier of Fig. 6-15(*b*): (*a*) Find an expression for the high-frequency voltage-gain ratio. (*b*) Describe the high-frequency behavior of the CB amplifier.

(*a*) Use of the hybrid-π model of Fig. 8-8 results in the high-frequency small-signal equivalent circuit of Fig. 8-24. The coupling capacitors are assumed to be short circuits at high frequency. For typical values, $r_x \ll 1/sC_\pi, r_\pi, 1/sC_\mu$ for frequencies near the break frequencies; thus, letting $r_x = 0$ introduces little error (but considerable simplicity).

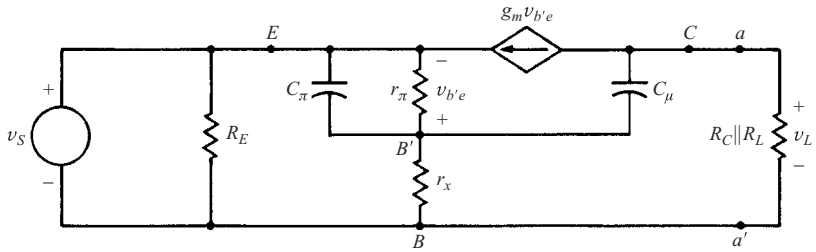


Fig. 8-24

A Thévenin equivalent can be found for the network to the left of terminal pair a, a'. With $r_x = 0$, current from the dependent source flows only through C, so

$$V_{Th} = -\frac{1}{sC_\mu} g_m V_{b'e} \tag{1}$$

By the method of node voltages,

$$\frac{V_S + V_{b'e}}{R_S} + g_m V_{b'e} + V_{b'e}(sC_\pi + G_E + g_\pi) = 0 \tag{2}$$

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Solving (*2*) for $V_{b'e}$ and substituting the result into (*1*) yield

$$V_{Th} = \frac{g_m V_S}{sC_\mu[1 + R_S g_m + R_S(sC_\pi + G_E + g_\pi)]} \tag{3}$$

Deactivating (shorting) V_S also shorts E to B'. Consequently, $V_{b'e} = 0$, the dependent current source is open-circuited, and $Z_{Th} = 1/sC_\mu$.

Now, the Thévenin equivalent and voltage division lead to

$$V_L = \frac{R_C \| R_L}{R_C \| R_L + Z_{Th}} V_{Th} \tag{4}$$

Substitution of (*3*) into (*4*) and rearrangement give the desired voltage-gain ratio:

$$A_v = \frac{V_L}{V_S} = \frac{g_m R_C \| R_L}{[sC_\mu(R_C \| R_L) + 1][sC_\pi R_S + R_S(g_m + g_\pi + G_E) + 1]} \tag{5}$$

(*b*) Since (*5*) involves the upper frequency range, it describes the amplifier as a low-pass (midfrequency) filter with break frequencies at

$$\omega_1 = \frac{1}{C_\mu(R_C \| R_L)} \qquad \text{and} \qquad \omega_2 = \frac{R_S(g_m + g_\pi + G_E) + 1}{C_\pi R_S} \tag{6}$$

8.18 (*a*) Apply the results of Section 8.6 to the small-signal equivalent circuit of Fig. 8-9(*a*) to determine the Miller capacitance. (*b*) Using the Miller capacitance, draw the associated equivalent circuit and from it find an expression for the high-frequency voltage-gain ratio.

(*a*) First, the gain K_F must be found with capacitor C_μ and load resistor R_L removed. Since

$$V_L = -g_m V_{b'e} R_C$$

the desired gain is

$$K_F = \frac{V_L}{V_{b'e}} = -g_m R_C \tag{1}$$

The Miller capacitance C_M is the input shunt capacitance suggested by (*8.46*):

$$C_M = (1 - K_F)\frac{Y_F}{s} = (1 + g_m R_C)C_\mu \tag{2}$$

since comparison of Figs. 8-9(*a*) and 8-12(*a*) shows that C_μ forms a feedback path analogous to Y_F.

(*b*) The output shunt capacitance, as suggested by (*8.48*), must also be determined. Since $h_{re} = 0$ underlies the hybrid-π model, the reverse voltage-gain ratio $K_R = 0$, hence:

$$Y_o = Y_2 + (1 - K_R)Y_F \approx Y_2 + Y_F = Y_2 + sC_\mu \tag{3}$$

Comparison of Fig. 8-9(*a*) with Fig. 8-12(*b*) and the use of (*1*) to (*3*) lead to the equivalent circuit of Fig. 8-25. Let

$$C_{eq} = C_M + C_\pi = (1 + g_m R_C)C_\mu + C_\pi$$

Then, by voltage division,

$$V_{b'e} = \frac{r_\pi/(sr_\pi C_{eq} + 1)}{r_x + r_\pi/(sr_\pi C_{eq} + 1)} V_s = \frac{r_\pi/(r_x + r_\pi)}{s(r_x \| r_\pi)C_{eq} + 1} V_s \tag{4}$$

and by Ohm's law,

$$V_L = -\frac{R_C \| R_L}{s(R_C \| R_L)C_\mu + 1} g_m V_{b'e} \tag{5}$$

Substitution of (*4*) into (*5*) and rearrangement yield the desired voltage-gain ratio:

$$A_v(s) = \frac{V_L}{V_s} = -\frac{g_m(R_C \| R_L)r_\pi/(r_x + r_\pi)}{[s(R_C \| R_L)C_\mu + 1][s(r_x \| r_\pi)C_{eq} + 1]}$$

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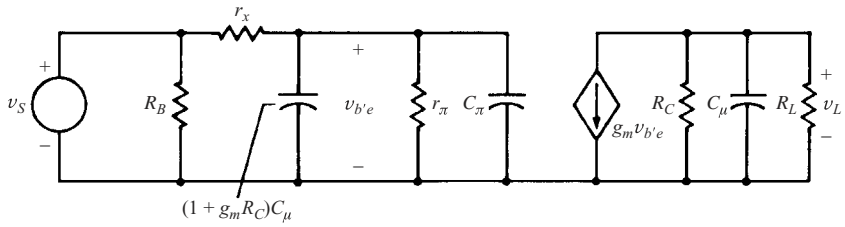


Fig. 8-25

8.19 (*a*) Apply the results of Section 8.6 to the small-signal equivalent circuit of Fig. 8-11 to determine the Miller admittance. (*b*) Utilizing the Miller admittance, draw the high-frequency small-signal equivalent circuit and determine the voltage-gain ratio.

(*a*) With load resistor R_L and feedback capacitor C_{gd} removed from the circuit of Fig. 8-11, the forward gain K_F follows from an application of Ohm's law:

$$K_F = \frac{V_L}{V_{gs}} = -\frac{g_m(r_{ds} \| R_D)}{s(r_{ds} \| R_D)C_{ds} + 1} \tag{1}$$

The Miller admittance suggested by (*8.46*) is

$$Y_M = (1 - K_F)Y_F = \left[1 + \frac{g_m(r_{ds} \| R_D)}{s(r_{ds} \| R_D)C_{ds} + 1}\right] s\, C_{gd} \tag{2}$$

In the frequency range of interest and for typical values of r_{ds}, R_D, and C_{ds}, generally $|s(r_{ds} \| R_D)C_{ds}| \ll 1$; thus, the Miller admittance can be synthesized as a capacitor with value

$$C_M = \frac{Y_M}{s} = [1 + g_m(r_{ds} \| R_D)]C_{gd} \tag{3}$$

(*b*) Since there is no feedback of output voltage to the input network of Fig. 8-11, $K_R = 0$. Hence, the output admittance, as suggested by (*8.48*), is simply

$$(1 - K_R)Y_F = Y_F = sC_{gd} \tag{4}$$

The equivalent circuit of Fig. 8-11 can be converted to the form of Fig. 8-12(*b*), as displayed in Fig. 8-26. By Ohm's law,

$$V_L = -\frac{g_m V_{gs}}{s(C_{ds} + C_{gd}) + g_{ds} + G_D + G_L} \tag{5}$$

Since $V_{gs} = V_i$, the required voltage-gain ratio follows as

$$A_v(s) = \frac{V_L}{V_i} = -\frac{g_m}{s(C_{ds} + C_{gd}) + g_{ds} + G_D + G_L} \tag{6}$$

As long as the source resistance is negligible, A_v is independent of C_M. (See Problem 8.25.)

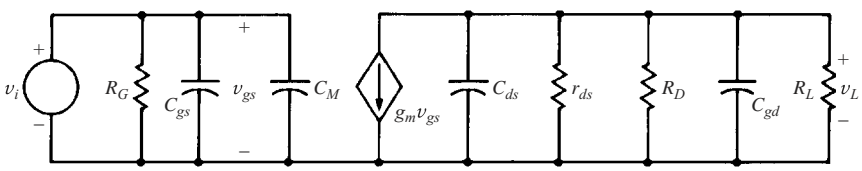


Fig. 8-26

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8.20 The high-frequency equivalent circuit for the CS JFET amplifier of Fig. 4-5 is given by Fig. 8-11. Let $R_G = 1\,\text{M}\Omega$, $R_L = R_D = 2\,\text{k}\Omega$, $r_{ds} = 50\,\text{k}\Omega$, $g_m = 0.016\,\text{S}$, $C_{gs} = 3\,\text{pF}$, $C_{ds} = 1\,\text{pF}$, and $C_{gd} = 2.7\,\text{pF}$. By SPICE methods, determine the voltage gain for a 50 MHz impressed signal.

The netlist code below describes the circuit:

```
Prb8_20.CIR
vi  1 0 AC 0.25V
RG  1 0 1Megohm
Cgs 1 0 3pF
Cgd 1 2 2.7pF
Ggm 2 0 (1,0) 0.016
rds 2 0 50kohm
Cds 2 0 1pF
RD  2 0 2kohm
RL  2 0 2kohm
.AC DEC 100 1MegHz 100MegHz
.PROBE
.END
```

Execute ⟨Prb8_20.CIR⟩ and use the Probe feature of PSpice to give Fig. 8-27. From the marked points, it is seen that the voltage gain at 50 MHz is

$$A_v = 10.36\angle 128.2^\circ$$

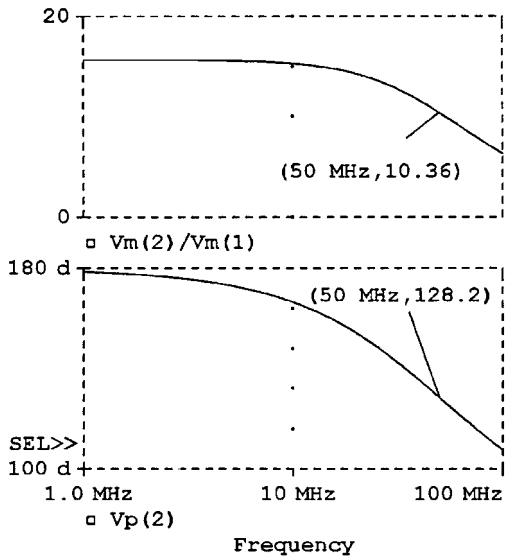


Fig. 8-27

8.21 For the CG JFET amplifier of Fig. 4-28, let $V_{DD} = 15\,\text{V}$, $R_1 = R_2 = 10\,\text{k}\Omega$, $R_D = 500\,\Omega$, $R_S = 2\,\text{k}\Omega$, and $C_{C1} = C_{C2} = 15\,\mu\text{F}$. Add a load resistor $R_L = 15\,\text{k}\Omega$. The JFET is modeled by the parameters of Problem 4.4. Use SPICE methods to implement a wide frequency range study to determine low- and high-frequency cutoff points for this amplifier.

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The following netlist code describes the amplifier circuit:

```
Prb8_21.CIR
vi  1 0 AC 0.25V
CC1 1 2 15uF
RS  2 0 2kohm
J 3  4 2 NJFET
.MODEL NJFET NJF( Vto=-4V Beta=0.0005ApVsq
+ Rd=1ohm Rs=1ohm CGS=2pF CGD=2pF)
R1  4 5 10kohm
R2  4 0 10kohm
RD  3 5 500ohm
VDD 5 0 15V
CC2 3 6 15uF
RL  6 0 15kohm
.AC DEC 100 10Hz 50MegHz
.PROBE
.END
```

Execute ⟨Prb8_21.CIR⟩ and use the Probe feature of PSpice to yield the gain magnitude plot of Fig. 8-28. The marked points show the cutoff frequencies to be $f_L = 36.4\,\text{Hz}$ and $f_H = 9.9\,\text{MHz}$.

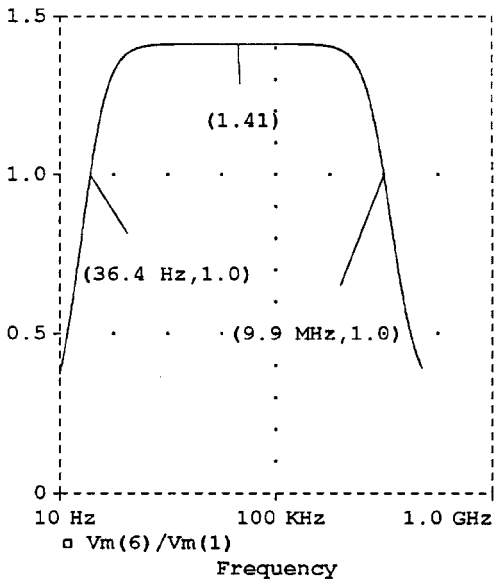


Fig. 8-28

Supplementary Problems

8.22 Show that if two linear networks are connected in cascade to form a new network such that $T(j\omega) = T_1(j\omega)T_2(j\omega)$, then the composite Bode plot is obtained by adding the individual amplitude ratios M_{db1} and M_{db2} and phase angles (ϕ_1 and ϕ_2) associated with $T_1(j\omega)$ and $T_2(j\omega)$ at each frequency.

8.23 Show that (*8.3*) follows from the evaluation of k_1 and k_2 of (*8.2*).

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8.24 An amplifier has a Laplace-domain transfer function (voltage-gain ratio) given by

$$A_v(s) = \frac{V_o}{V_i} = \frac{K_s}{(s+100)(s+10^5)}$$

(*a*) If an asymptotic Bode plot of $A_v(j\omega)$ is made, over what values of frequency (in the midfrequency range) is the gain constant in amplitude? (*b*) Find the midfrequency gain in decibels if $K_s = 10^8$. (*c*) Within 2 percent accuracy, over what range of frequencies is the exact gain constant?

Ans. (*a*) $100 \le \omega \le 10^5$ rad/s; (*b*) $M_{dbM} = 60$ db; (*c*) $M_{db} \ge 58.8$ db for $500 \le \omega \le 5 \times 10^4$ rad/s

8.25 In Problem 8.19, the gain of the FET amplifier does not depend on the Miller capacitance C_M; however, the situation changes if the source resistance is nonzero. (*a*) Add a source resistance R_i to Fig. 8-26, and find an expression for the voltage-gain ratio. (*b*) Evaluate the gain for $R_i = 0$ and for $R_i = 100\,\Omega$ if $C_{gs} = 3$ pF, $C_{ds} = 1$ pF, $C_{gd} = 2.7$ pF, $r_{ds} = 50\,\text{k}\Omega$, $g_m = 0.016$ S, $R_L = R_D = 2\,\text{k}\Omega$, $R_G = 1\,\text{M}\Omega$, and $f = 50$ MHz.

Ans. (*a*) $$A_v(s) = \frac{-g_m R_G/(R_i + R_G)}{[s(C_{ds} + C_{dg}) + g_{ds} + G_D + G_L][s(R_G \| R_i)(C_{gs} + C_M) + 1]}$$

(*b*) For $R_i = 0$, $A_v = 10.348|\underline{131.53}^\circ$; for $R_i = 100$, $A_v = 3.49|\underline{61.26}^\circ$

8.26 Consider the high-pass filter circuit of Fig. 8-15(*a*). (*a*) Show that as ω becomes large, the amplitude ratio M_{db} actually approaches $20\log[R_L/(R_L + R_S)]$ as indicated in Fig. 8-15(*b*). (*b*) Show that $|M^2(j\omega_L)|$, where $\omega_L = 1/C(R_L + R_S)$, has the value $\frac{1}{2}|M^2(j\infty)| = \frac{1}{2}[R_L/(R_L + R_S)]^2$.

8.27 In the high-pass filter circuit of Fig. 8-15(*a*), the source impedance $R_S = 5\,\text{k}\Omega$. If the circuit is to have a high-frequency gain of 0.75 and a break or cutoff frequency of 100 rad/s, size R_L and C.

Ans. $R_L = 15\,\text{k}\Omega$, $C = 0.5\,\mu\text{F}$

8.28 In the circuit of Fig. 3-20, replace V_S with a sinusoidal source to give the small-signal circuit of Fig. 8-6. (*a*) If the impedance of the coupling capacitor is not negligible, find the current-gain ratio $A_i(s) = I_L/I_S$. (*b*) Determine the low-frequency cutoff point.

Ans. (*a*) $A_i = h_{fe}R_B/(R_B + h_{ie})$; (*b*) the gain is independent of frequency down to $f = 0$

8.29 Show that the *RC* network of Fig. 8-29 is a high-pass filter. Determine its low-frequency cutoff point.

Ans. $$\frac{V_o}{V_S} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \frac{sR_2R_3C_3/(R_2 + R_3) + 1}{s(R_1 + R_2)R_3C_3/(R_1 + R_2 + R_3) + 1} \qquad \omega_L = \frac{R_1 + R_2 + R_3}{(R_1 + R_2)R_3C_3}$$

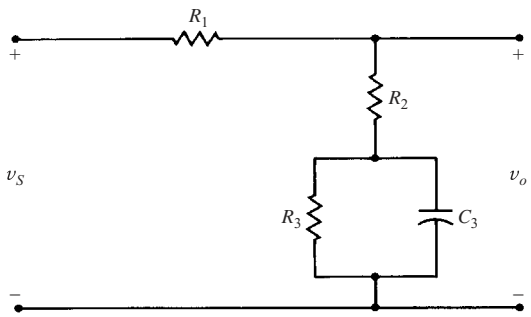


Fig. 8-29

8.30 The amplifier of Fig. 3-10 is modeled for small-signal operation by Fig. 8-4. Let $C_C \to \infty$, $C_E = 100\,\mu\text{F}$, $R_E = 100\,\Omega$, $R_C = R_L = 2\,\text{k}\Omega$, $h_{ie} = 200\,\Omega$ and $h_{fe} = 75$. Determine (*a*) the low-frequency voltage gain, (*b*) the midfrequency gain, and (*c*) the low-frequency cutoff point.

Ans. (*a*) -9.62; (*b*) -375; (*c*) 3750 rad/s

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8.31 For the amplifier of Fig. 3-10, show that if the source internal impedance R_i is not negligible, but $R_i \ll R_B = R_1 \| R_2$, then the low-frequency cutoff point is given by

$$\omega_L = \frac{(h_{ie} + R_i) + (h_{fe} + 1)R_E}{R_E C_E (h_{ie} + R_i)}$$

8.32 Show that, for the amplifier of Fig. 3-10 as described in Problem 8.5, if $R_B \gg R_E + h_{ie}$, then the current-gain ratio becomes independent of frequency.

8.33 In the amplifier of Fig. 3-10, let $C_C \to \infty$, $C_E = 100\,\mu\text{F}$, $R_E = 20\,\text{k}\Omega$, $h_{ie} = 100\,\Omega$, $h_{fe} = 75$, $R_C = R_L = 2\,\text{k}\Omega$, $R_1 = 2\,\text{k}\Omega$, and $R_2 = 20\,\text{k}\Omega$. Determine (*a*) the low-frequency current gain, (*b*) the midfrequency current gain, and (*c*) the low-frequency cutoff point.
Ans. (*a*) -3.11; (*b*) -35.54; (*c*) 5.71 rad/s

8.34 In the amplifier of Problem 8.6, let $R_i = 500\,\Omega$ and all else remain unchanged. Determine the value of the emitter bypass capacitor required to ensure that $f_L \le 200\,\text{Hz}$. Compare your result with that of Problem 8.6 to see that consideration of the source internal impedance allows the use of a smaller bypass capacitor. (*Hint*: See Problem 8.31.) *Ans.* $C_E \ge 101.3\,\mu\text{F}$

8.35 In the amplifier of Fig. 3-10, $C_C \to \infty$, $R_i = 500\,\Omega$, $R_E = 30\,\text{k}\Omega$, $R_1 = 3.2\,\text{k}\Omega$, $R_2 = 17\,\text{k}\Omega$, $R_L = 10\,\text{k}\Omega$, $h_{oe} = h_{re} = 0$, $h_{fe} = 100$, and $h_{ie} = 100\,\Omega$. Determine R_C and C_E so that the amplifier has a midfrequency current-gain ratio $|A_i| \ge 30$ with low-frequency cutoff $f_L \ge 20\,\text{Hz}$. (*Hint*: See Problem 8.5.)
Ans. $R_C \ge 4517.8\,\Omega$, $C_E \ge 3.13\,\mu\text{F}$

8.36 In the CE amplifier of Fig. 3-10, let $C_C \to \infty$, $C_E = 100\,\mu\text{F}$, $R_E = 100\,\Omega$, $R_i = 0$, $R_B = 5\,\text{k}\Omega$, $R_C = R_L = 2\,\text{k}\Omega$, $h_{oe} = h_{re} = 0$, $h_{fe} = 75$, and $h_{ie} = 1\,\text{k}\Omega$. The small-signal ac equivalent circuit is given by Fig. 8-4. If a sinusoidal signal $v_i = V_m \sin \omega t$ is impressed (with $\omega = 400$ rad/s), determine (*a*) the phase angle between v_i and i_i, (*b*) the phase shift between input and output voltages, and (*c*) the phase shift between input and output currents.
Ans. (*a*) Current leads voltage by 35.52°; (*b*) output voltage lags input voltage by 128.98°; (*c*) output current lags input current by 180°

8.37 In the amplifier of Problem 8.13, let $C_E = 200\,\mu\text{F}$, $C_C = 10\,\mu\text{F}$, $R_E = 50\,\Omega$, $R_C = R_L = 2\,\text{k}\Omega$, $R_i = 100$, $h_{re} = h_{oe} = 0$, $h_{ie} = 1\,\text{k}\Omega$, and $h_{fe} = 50$. (*a*) Sketch the asymptotic Bode plot (M_{db} only) for the voltage-gain ratio. (*b*) Is the 3-db attenuation point below 40 Hz?
Ans. (*a*) $A_v(s) = -0.548s(0.01s + 1)/[(0.04s + 1)(0.00301s + 1)]$. The associated Bode plot is given in Fig. 8-30; (*b*) no, because $M_{db}(j\infty) - M_{db}(j80\pi) = 3.79\,\text{db}$

8.38 In the CE amplifier of Example 8.7, let $g_m = 0.035\,\text{S}$, $r_\pi = 8\,\text{k}\Omega$, $r_x = 30\,\Omega$, $R_C = R_L = 10\,\text{k}\Omega$, $C_\pi = 10\,\text{pF}$, and $C_\mu = 2\,\text{pF}$. (*a*) Determine the high-frequency cutoff point. (*b*) Find the midfrequency gain.
Ans. (*a*) $f_H = 16.49\,\text{MHz}$; (*b*) $A_{v\text{mid}} = -174.3$

8.39 In the CB amplifier of Problem 8.17, let $R_S = 100\,\Omega$, $R_E = 1\,\text{k}\Omega$, $R_C = R_L = 10\,\text{k}\Omega$, $C_\mu = 2\,\text{pF}$, $C_\pi = 40\,\text{pF}$, $g_m = 0.035\,\text{S}$, and $r_\pi = 5\,\text{k}\Omega$. Determine (*a*) the midfrequency gain and (*b*) the high-frequency cutoff point. *Ans.* (*a*) $A_{v\text{mid}} = 37.88$; (*b*) $f_H = 15.91\,\text{MHz}$

8.40 Add a source resistance R_i to the high-frequency small-signal equivalent circuit for the CS amplifier given by Fig. 8-11. Let $C_{gs} = 3\,\text{pF}$, $C_{ds} = 1\,\text{pF}$, $C_{gd} = 2.7\,\text{pF}$, $r_{ds} = 50\,\text{k}\Omega$, $g_m = 0.016\,\text{S}$, $R_L = R_D = 2\,\text{k}\Omega$, and $R_G = 1\,\text{M}\Omega$. Determine the high-frequency cutoff point (*a*) with $R_i = 0$ and (*b*) with $R_i = 100$.
Ans. (*a*) $f_H = 43.875\,\text{MHz}$; (*b*) $f_H = 13.69\,\text{MHz}$

8.41 For the hybrid-π model of a CB BJT amplifier circuit given by Fig. 8-24, let $R_E = 200\,\Omega$, $R_C = R_L = 10\,\text{k}\Omega$, $r_x = 25\,\Omega$, $r_\pi = 5\,\text{k}\Omega$, $g_m = 0.02\,\text{S}$, and $C_\mu = C_\pi = 2\,\text{pF}$. Use SPICE methods to determine the midfrequency voltage gain and the high-frequency cutoff point. (*Netlist code available at the author's website.*)
Ans. $A_{v\text{mid}} = 100$, $f_H = 16.1\,\text{MHz}$

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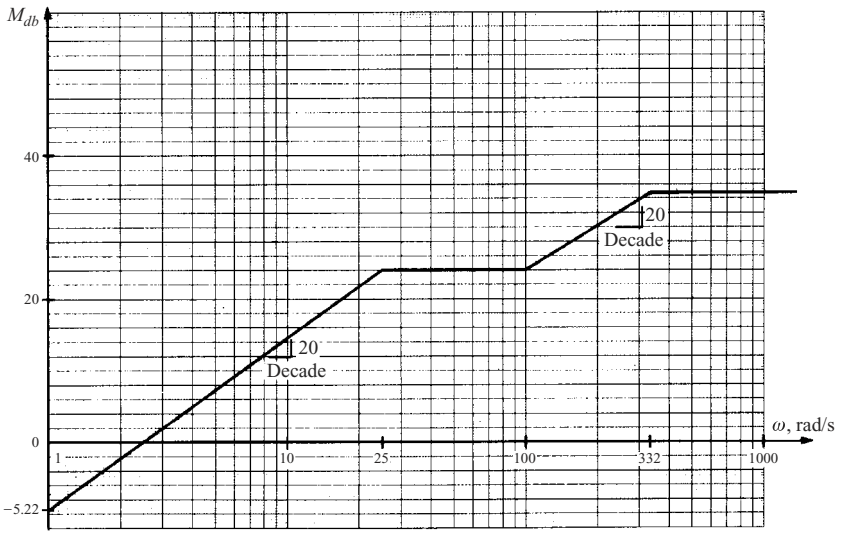


Fig. 8-30

8.42 The CS JFET amplifier of Fig. 7-2(*a*) is modeled by the equivalent circuit of Fig. 8-22 for low-frequency operation. Let $R_G = 500\,\text{k}\Omega$, $R_S = 500\,\Omega$, $R_D = 3\,\text{k}\Omega$, $C_S = 10\,\mu\text{F}$, $\mu = 60$, and $r_{ds} = 30\,\text{k}\Omega$. Use SPICE methods to determine the low-frequency cutoff point. (*Netlist code available at the author's website.*)
Ans. $f_L = 40.9\,\text{Hz}$

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CHAPTER 9

Operational Amplifiers

9.1. INTRODUCTION

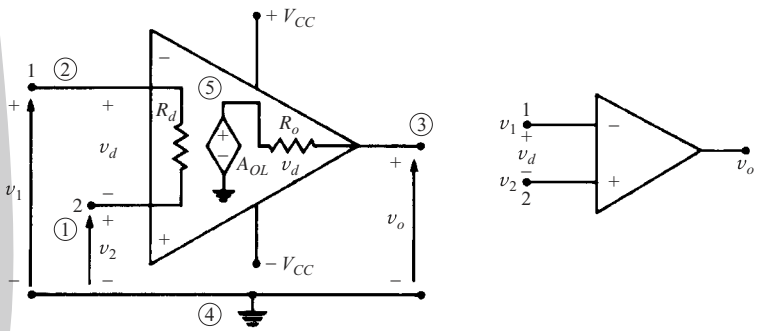
The name *operational amplifier* (op amp) was originally given to an amplifier that could be easily modified by external circuitry to perform mathematical operations (addition, scaling, integration, etc.) in analog-computer applications. However, with the advent of solid-state technology, op amps have become highly reliable, miniaturized, temperature-stabilized, and consistently predictable in performance; they now figure as fundamental building blocks in basic amplification and signal conditioning, in active filters, function generators, and switching circuits.

9.2. IDEAL AND PRACTICAL OP AMPS

An op amp amplifies the difference $v_d \equiv v_1 - v_2$ between two input signals (see Fig. 9-1), exhibiting the open-loop voltage gain

$$A_{OL} \equiv \frac{v_o}{v_d} \tag{9.1}$$

In Fig. 9-1, terminal 1 is the *inverting input* (labeled with a minus sign on the actual amplifier); signal v_1 is amplified in magnitude and appears phase-inverted at the output. Terminal 2 is the *noninverting input* (labeled with a plus sign); output due to v_2 is phase-preserved.



(*a*) Complete representation (*b*) Simplified representation

Fig. 9-1 Operational amplifier

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In magnitude, the open-loop voltage gain in op amps ranges from 10^4 to 10^7. The maximum magnitude of the output voltage from an op amp is called its *saturation voltage*; this voltage is approximately 2 V smaller than the power-supply voltage. In other words, the amplifier is linear over the range

$$-(V_{CC} - 2) < v_o < V_{CC} - 2\,\text{V} \tag{9.2}$$

The *ideal* op amp has three essential characteristics which serve as standards for assessing the goodness of a *practical* op amp:

1. The open-loop voltage gain A_{OL} is negatively infinite.
2. The input impedance R_d between terminals 1 and 2 is infinitely large; thus, the input current is zero.
3. The output impedance R_o is zero; consequently, the output voltage is independent of the load.

Figure 9-1(*a*) models the practical characteristics.

Example 9.1. An op amp has saturation voltage $V_{o\text{sat}} = 10\,\text{V}$, an open-loop voltage gain of -10^5, and input resistance of 100 kΩ. Find (*a*) the value of v_d that will just drive the amplifier to saturation and (*b*) the op amp input current at the onset of saturation.

(*a*) By (*9.1*),

$$v_d = \frac{\pm V_{o\text{sat}}}{A_{OL}} = \frac{\pm 10}{-10^5} = \pm 0.1\,\text{mV}$$

(*b*) Let i_{in} be the current into terminal 1 of Fig. 9-1(*b*); then

$$i_{\text{in}} = \frac{v_d}{R_d} = \frac{\pm 0.1 \times 10^{-3}}{100 \times 10^3} = \pm 1\,\text{nA}$$

In application, a large percentage of negative feedback is used with the operational amplifier, giving a circuit whose characteristics depend almost entirely on circuit elements external to the basic op amp. The error due to treatment of the basic op amp as ideal tends to diminish in the presence of negative feedback.

9.3. INVERTING AMPLIFIER

The *inverting amplifier* of Fig. 9-2 has its noninverting input connected to ground or common. A signal is applied through input resistor R_1, and negative current feedback (see Problem 9.1) is implemented through *feedback resistor* R_F. Output v_o has polarity opposite that of input v_S.

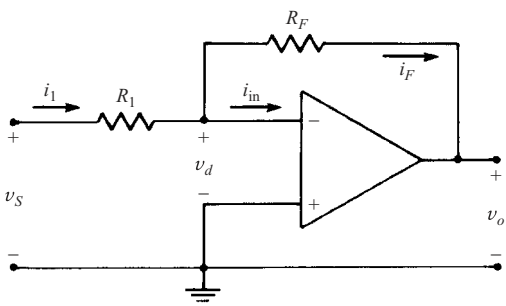


Fig. 9-2 Inverting amplifier

Example 9.2. For the inverting amplifier of Fig. 9-2, find the voltage gain v_o/v_S using (*a*) only characteristic 1 and (*b*) only characteristic 2 of the ideal op amp.

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(*a*) By the method of node voltages at the inverting input, the current balance is

$$\frac{v_S - v_d}{R_1} + \frac{v_o - v_d}{R_F} = i_{\text{in}} = \frac{v_d}{R_d} \tag{9.3}$$

where R_d is the differential input resistance. By (*9.1*), $v_d = v_o/A_{OL}$ which, when substituted into (*9.3*), gives

$$\frac{v_S - v_o/A_{OL}}{R_1} + \frac{v_o - v_o/A_{OL}}{R_F} = \frac{v_o/R_d}{A_{OL}} \tag{9.4}$$

In the limit as $A_{OL} \to -\infty$, (*9.4*) becomes

$$\frac{v_S}{R_1} + \frac{v_o}{R_F} = 0 \qquad \text{so that} \qquad A_v \equiv \frac{v_o}{v_S} = -\frac{R_F}{R_1} \tag{9.5}$$

(*b*) If $i_{\text{in}} = 0$, then $v_d = i_{\text{in}} R_d = 0$, and $i_1 = i_F \equiv i$. The input and feedback-loop equations are, respectively,

$$v_S = iR_1 \qquad \text{and} \qquad v_o = -iR_F$$

whence

$$A_v \equiv \frac{v_o}{v_S} = -\frac{R_F}{R_1} \tag{9.6}$$

in agreement with (*9.5*).

9.4. NONINVERTING AMPLIFIER

The *noninverting amplifier* of Fig. 9-3 is realized by grounding R_1 of Fig. 9-2 and applying the input signal at the noninverting op amp terminal. When v_2 is positive, v_o is positive and current i is positive. Voltage $v_1 = iR_1$ then is applied to the inverting terminal as negative voltage feedback.

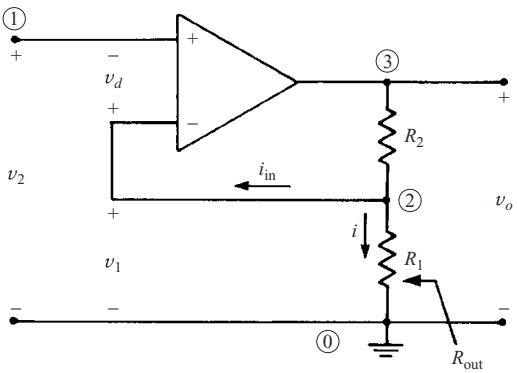


Fig. 9-3 Noninverting amplifier

Example 9.3. For the noninverting amplifier of Fig. 9-3, assume that the current into the inverting terminal of the op amp is zero, so that $v_d \approx 0$ and $v_1 \approx v_2$. Derive an expression for the voltage gain v_o/v_2.

With zero input current to the basic op amp, the currents through R_2 and R_1 must be identical; thus,

$$\frac{v_o - v_1}{R_2} = \frac{v_1}{R_1} \qquad \text{and} \qquad A_v \equiv \frac{v_o}{v_2} \approx \frac{v_o}{v_1} = 1 + \frac{R_2}{R_1} \tag{9.7}$$

9.5. COMMON-MODE REJECTION RATIO

The *common-mode gain* is defined (see Fig. 9-1) as

$$A_{cm} \equiv -\frac{v_o}{v_2} \tag{9.8}$$

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where $v_1 = v_2$ by explicit connection. Usually, A_{cm} is much less than unity ($A_{cm} = -0.01$ being typical). Common-mode gain sensitivity is frequently quantized via the *common-mode rejection ratio* (CMRR), defined as

$$\text{CMRR} = \frac{A_{OL}}{A_{cm}} \tag{9.9}$$

and expressed in decibels as

$$\text{CMRR}_{db} = 20 \log \frac{A_{OL}}{A_{cm}} = 20 \log \text{CMRR} \tag{9.10}$$

Typical values for the CMRR range from 100 to 10,000, with corresponding CMRR_{db} values of from 40 to 80 db.

Example 9.4. Find the voltage-gain ratio A_v of the noninverting amplifier of Fig. 9-3 in terms of its CMRR. Assume $v_1 = v_2$ insofar as the common-mode gain is concerned.

The amplifier output voltage is the sum of two components. The first results from amplification of the difference voltage v_d as given by (*9.1*). The second, defined by (*9.8*), is a direct consequence of the common-mode gain. The total output voltage is, then,

$$v_o = A_{OL} v_d - A_{cm} v_2 \tag{9.11}$$

Voltage division (with $i_{\text{in}} = 0$) gives

$$v_d = v_1 - v_2 = \frac{R_1}{R_1 + R_2} v_o - v_2 \tag{9.12}$$

and substituting (*9.12*) into (*9.11*) and rearranging give

$$v_o \left(1 - \frac{A_{OL} R_1}{R_1 + R_2}\right) = -(A_{OL} + A_{cm}) v_2$$

Then

$$A_v = \frac{v_o}{v_2} = \frac{-(A_{OL} + A_{cm})}{1 - A_{OL} R_1/(R_1 + R_2)} = \frac{-A_{OL}}{1 - A_{OL} R_1/(R_1 + R_2)} - \frac{A_{OL}/\text{CMRR}}{1 - A_{OL} R_1/(R_1 + R_2)} \tag{9.13}$$

9.6. SUMMER AMPLIFIER

The *inverting summer amplifier* (or *inverting adder*) of Fig. 9-4 is formed by adding parallel inputs to the inverting amplifier of Fig. 9-2. Its output is a weighted sum of the inputs, but inverted in polarity. In an ideal op amp, there is no limit to the number of inputs; however, the gain is reduced as inputs are added to a practical op amp (see Problem 9.31).

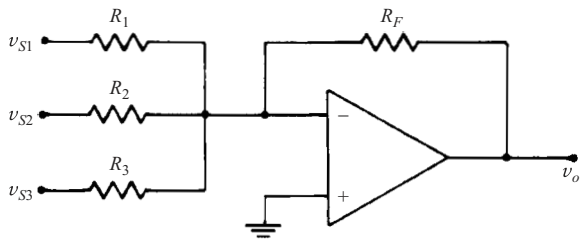


Fig. 9-4 Inverting summer amplifier

Example 9.5. Find an expression for the output of the inverting summer amplifier of Fig. 9-4, assuming the basic op amp is ideal.

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We use the principle of superposition. With $v_{S2} = v_{S3} = 0$, the current in R_1 is not affected by the presence of R_2 and R_3, since the inverting node is a virtual ground (see Problem 9.1). Hence, the output voltage due to v_{S1} is, by (9.5), $v_{o1} = -(R_F/R_1)v_{S1}$. Similarly, $v_{o2} = -(R_F/R_2)v_{S2}$ and $v_{o3} = -(R_F/R_3)v_{S3}$. Then, by superposition,

$$v_o = v_{o1} + v_{o2} + v_{o3} = -R_F\left(\frac{v_{S1}}{R_1} + \frac{v_{S2}}{R_2} + \frac{v_{S3}}{R_3}\right)$$

9.7. DIFFERENTIATING AMPLIFIER

The introduction of a capacitor into the input path of an op amp leads to time differentiation of the input signal. The circuit of Fig. 9-5 represents the simplest *inverting differentiator* involving an op amp. As such, the circuit finds limited practical use, since high-frequency noise can produce a derivative whose magnitude is comparable to that of the signal. In practice, high-pass filtering is utilized to reduce the effects of noise (see Problem 9.7).

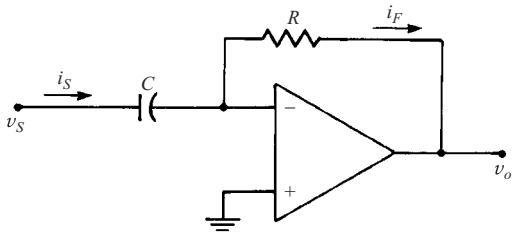


Fig. 9-5 Differentiating amplifier

Example 9.6. Find an expression for the output of the inverting differentiator of Fig. 9-5, assuming the basic op amp is ideal.

Since the op amp is ideal, $v_d \approx 0$, and the inverting terminal is a virtual ground. Consequently, v_S appears across capacitor C:

$$i_S = C\,\frac{dv_S}{dt}$$

But the capacitor current is also the current through R (since $i_{\text{in}} = 0$). Hence,

$$v_o = -I_F R = -i_S R = -RC\,\frac{dv_S}{dt}$$

9.8. INTEGRATING AMPLIFIER

The insertion of a capacitor in the feedback path of an op amp results in an output signal that is a time integral of the input signal. A circuit arrangement for a simple *inverting integrator* is given in Fig. 9-6.

Example 9.7. Show that the output of the inverting integrator of Fig. 9-6 actually is the time integral of the input signal, assuming the op amp is ideal.

If the op amp is ideal, the inverting terminal is a virtual ground, and v_S appears across R. Thus, $i_S = v_S/R$. But, with negligible current into the op amp, the current through R must also flow through C. Then

$$v_o = -\frac{1}{C}\int i_F\,dt = -\frac{1}{C}\int i_S\,dt = -\frac{1}{RC}\int v_S\,dt$$

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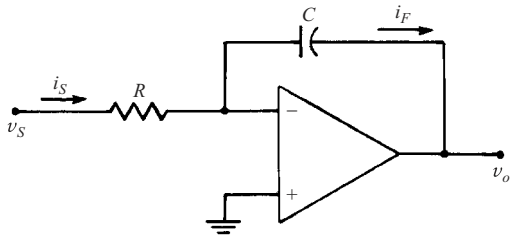


Fig. 9-6 Integrating amplifier

9.9. LOGARITHMIC AMPLIFIER

Analog multiplication can be carried out with a basic circuit like that of Fig. 9-7. Essential to the operation of the logarithmic amplifier is the use of a feedback-loop device that has an exponential terminal characteristic curve; one such device is the semiconductor diode of Chapter 2, which is characterized by

$$i_D = I_o(e^{v_D/\eta V_T} - 1) \approx I_o\, e^{v_D/\eta V_T} \tag{9.14}$$

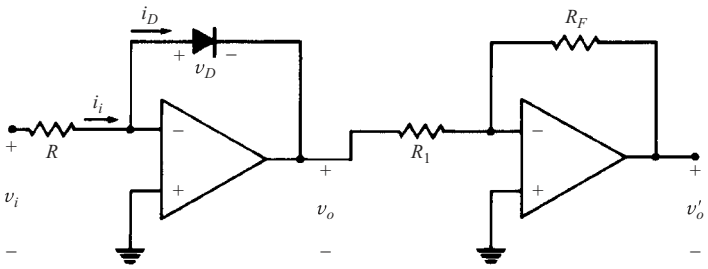


Fig. 9-7 Logarithmic amplifier

A grounded-base BJT can also be utilized, since its emitter current and base-to-emitter voltage are related by

$$i_E = I_S e^{v_{BE}/V_T} \tag{9.15}$$

Example 9.8. Determine the condition under which the output voltage v_o is proportional to the logarithm of the input voltage v_i in the circuit of Fig. 9-7.

Since the op amp draws negligible current,

$$i_i = \frac{v_i}{R} = i_D \tag{9.16}$$

Since $v_D = -v_o$, substitution of (*9.16*) into (*9.14*) yields

$$v_i = RI_o e^{-v_o/V_T} \tag{9.17}$$

Taking the logarithm of both sides of (*9.17*) leads to

$$\ln v_i = \ln RI_o - \frac{v_o}{V_T} \tag{9.18}$$

Under the condition that $\ln RI_o$ is negligible (which can be accomplished by controlling R so that $RI_o \approx 1$), (*9.18*) gives $v_o \approx -V_T \ln v_i$.

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9.10. FILTER APPLICATIONS

The use of op amps in active *RC* filters has increased with the move to integrated circuits. Active filter realizations can eliminate the need for bulky inductors, which do not satisfactorily lend themselves to integrated circuitry. Further, active filters do not necessarily attenuate the signal over the pass band, as do their passive-element counterparts. A simple *inverting*, *first-order*, *low-pass filter* using an op amp as the active device is shown in Fig. 9-8(*a*).

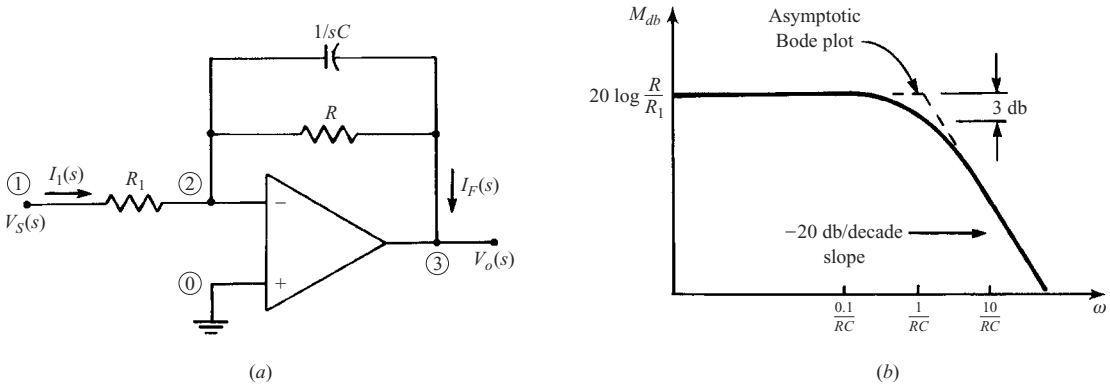


Fig. 9-8 First-order low-pass filter

Example 9.9. (*a*) For the low-pass filter whose *s*-domain (Laplace-transform) representation is given in Fig. 9-8(*a*), find the transfer function (voltage-gain ratio) $A_v(s) = V_o(s)/V_S(s)$. (*b*) Draw the Bode plot (M_{db} only) associated with the transfer function, to show that the filter passes low-frequency signals and attenuates high-frequency signals.

(*a*) The feedback impedance $Z_F(s)$ and the input impedance $Z_1(s)$ are

$$Z_F(s) = \frac{R(1/sC)}{R + (1/sC)} = \frac{R}{sRC + 1} \qquad \text{and} \qquad Z_1(s) = R_1 \tag{9.19}$$

The resistive circuit analysis of Example 9.2 extends directly to the *s* domain; thus,

$$A_v(s) = -\frac{Z_F(s)}{Z_1(s)} = -\frac{R/R_1}{sRC + 1} \tag{9.20}$$

(*b*) Letting $s = j\omega$ in (*9.20*) gives

$$M_{db} \equiv 20 \log |A_v(j\omega)| = 20 \log \frac{R}{R_1} - 20 \log |j\omega RC + 1|$$

A plot of M_{db} is displayed in Fig. 9-8(*b*). The curve is essentially flat below $\omega = 0.1/RC$; thus, all frequencies below $0.1/RC$ are passed with the dc gain R/R_1. A 3-db reduction in gain is experienced at the corner frequency $1/\tau = 1/RC$, and the gain is attenuated by 20 db per decade of frequency change for frequencies greater than $10/RC$.

9.11. FUNCTION GENERATORS AND SIGNAL CONDITIONERS

Frequently in analog system design, the need arises to modify amplifier gain in various ways, to compare signals with a generated reference, or to limit signals depending on their values. Such circuit applications can often be implemented with the high-input-impedance, low-output-impedance and high-gain characteristics of the op amp. The possibilities for op amp circuits are boundless; typically,

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however, nonlinear elements (such as diodes or transistors) are introduced into negative feedback paths, while linear elements are used in the input branches.

Example 9.10. The signal-conditioning amplifier of Fig. 9-9 changes gain depending upon the polarity of v_S. Find the circuit voltage gain for positive v_S and for negative v_S if diode D_2 is ideal.

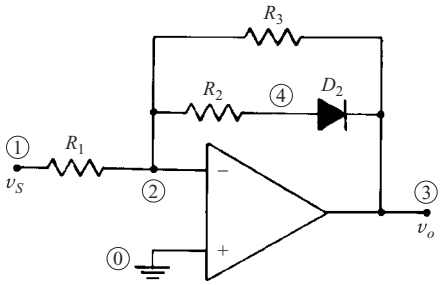


Fig. 9-9

If $v_S > 0$, then $v_o < 0$ and D_2 is forward-biased and appears as a short circuit. The equivalent feedback resistance is then

$$R_{Feq} = \frac{R_2 R_3}{R_2 + R_3}$$

and, by (9.5),

$$A_v = -\frac{R_{Feq}}{R_1} = -\frac{R_2 R_3}{R_1(R_2 + R_3)} \tag{9.21}$$

If $v_S < 0$, then $v_o > 0$ and D_2 is reverse-biased and appears as an open circuit. The equivalent feedback resistance is now $R_{Feq} = R_3$, and

$$A_v = -\frac{R_{Feq}}{R_1} = -\frac{R_3}{R_1} \tag{9.22}$$

9.12. SPICE OP AMP MODEL

Figure 9-1(*a*) presents the equivalent circuit model of the op amp using a VCVS to implement the gain. This circuit is easily realized by SPICE methods using the VCVS model of Fig. 1-2 and Table 1-1. It is frequently convenient to describe the op amp through use of a subcircuit as illustrated by the following netlist code:

```
.SUBCKT  OPAMP  1    2    3    4
*        Model  Inv  Ninv Out  Com
Rd 1 2 500kohm
E  5 4 (1,2) -1e5
Ro 5 3 100ohm
.ENDS OPAMP
```

The nodes are labeled in Fig. 9-1(*a*). Input impedance ($R_d = 500\,\text{k}\Omega$), output impedance ($R_o = 100\,\Omega$), and open-loop voltage gain ($A_{OL} = -1 \times 10^5$) are typical values that can be changed if an application warrants. Also, SPICE libraries usually contain subcircuit models of commercially available op amps that can be utilized.

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Example 9.11. Use SPICE methods to model the noninverting amplifier of Fig. 9-3 if the op amp has the parameter values of the subcircuit OPAMP above. Let $v_S = 0.5\sin(2000\pi t)$ V, $R_1 = 1\,\text{k}\Omega$, and $R_2 = 10\,\text{k}\Omega$. Verify that the voltage gain predicted by (*9.7*) results.

Netlist code describing the circuit is shown below:

```
Ex9_11.CIR
vs 1 0 SIN(0V 0.5V 1kHz)
R1 2 0 1kohm
R2 3 2 10kohm
XA 1 2 3 0 OPAMP
.SUBCKT OPAMP  1    2     3    4
*       Model  Inv  NInv  Out  Com
Rd 1 2 500kohm
E  5 4 (1,2) -le5
Ro 5 3 100ohm
.ENDS OPAMP
.TRAN 1us 2ms
.PROBE
.END
```

Execute ⟨Ex9_11.CIR⟩ and use the Probe feature of PSpice to plot Fig. 9-10. By use of the marked values of Fig. 9-10,

$$A_v = \frac{5.5}{0.5} = 11$$

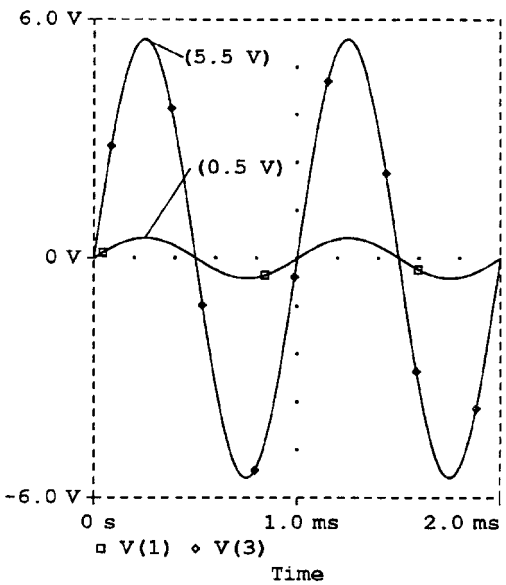


Fig. 9-10

The voltage gain predicted by (*9.7*) is

$$A_v = 1 + \frac{R_2}{R_1} = 1 + \frac{10 \times 10^3}{1 \times 10^3} = 11$$

Hence, (*9.7*) is validated.

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Example 9.12. Model the first-order low-pass filter of Fig. 9-8(*a*) by SPICE methods where the op amp is characterized by the parameters of subcircuit OPAMP. Let $R_1 = 1\,\text{k}\Omega$, $R = 10\,\text{k}\Omega$, and $C = 0.1\,\mu\text{F}$ to give a corner frequency $f_c = 1/2\pi\tau = 1/2\pi RC = 159.1\,\text{Hz}$. Show that the gain magnitude characteristic of Fig. 9-8(*b*) results.

The netlist code that follows describes the circuit where a frequency sweep from 10 Hz to 10 kHz is specified to give a reasonable band on either side of the corner frequency f_c:

```
Ex9_12.CIR
vs 1 0 AC 1V
R1 1 2 1kohm
R  2 3 10kohm
C  2 3 0.1uF
XA 2 0 3 0 OPAMP
.SUBCKT  OPAMP  1    2     3    4
*        Model  Inv  NInv  Out  Com
Rd 1 2 500kohm
E  5 4 (1,2) -1e5
Ro 5 3 100ohm
.ENDS  OPAMP
.AC DEC 200 10Hz 10kHz
.PROBE
.END
```

Execute ⟨Ex9_12.CIR⟩ and use the Probe feature of PSpice to plot the gain magnitude M_{db} as shown in Fig. 9-11. The low-frequency gain magnitude is seen to have the value predicted by the results of Example 9.9.

$$M_{db|_{\omega=0}} = 20\log(R/R_1) = 20\log\left(\frac{10\times 10^3}{1\times 10^3}\right) = 20\,\text{db}$$

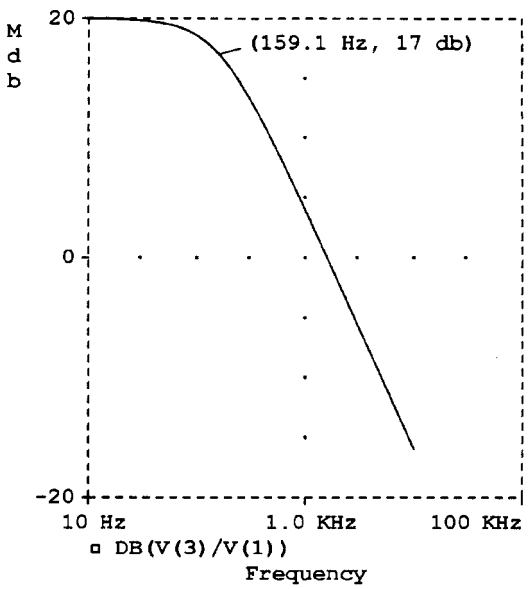


Fig. 9-11

The gain magnitude has decreased from the low-frequency value of 20 db to 17 db (drop of 3 db) at the corner frequency $f_c = 159.1\,\text{Hz}$. Clearly, the gain magnitude decreases by 20 db per decade of frequency for values of high frequency. Hence, the characteristic of Fig. 9-8(*b*) is verified.

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Solved Problems

9.1 For the inverting amplifier of Fig. 9-2: (*a*) Show that as $A_{OL} \to -\infty$, $v_d \to 0$; thus, the inverting input remains nearly at ground potential (and is called a *virtual ground*). (*b*) Show that the current feedback is actually negative feedback.

(*a*) By KVL around the outer loop,

$$v_S - v_o = i_1 R_1 + i_F R_F \tag{1}$$

Using (*9.1*) in (*1*), rearranging, and taking the limit give

$$\lim_{A_{OL}\to-\infty} v_d = \lim_{A_{OL}\to-\infty} \frac{-i_1 R_1 - i_F R_F + v_S}{A_{OL}} = 0 \tag{2}$$

(*b*) The feedback is negative if i_F counteracts i_1; that is, the two currents must have the same algebraic sign. By two applications of KVL, with $v_d \approx 0$,

$$i_1 = \frac{v_S - v_d}{R_1} \approx \frac{v_S}{R_1} \qquad \text{and} \qquad i_F = \frac{-v_o + v_d}{R_F} \approx \frac{-v_o}{R_F}$$

But in an inverting amplifier, v_o and v_S have opposite signs; therefore, i_1 and i_F have like signs.

9.2 (*a*) Use (*9.4*) to derive an exact formula for the gain of a practical inverting op amp. (*b*) If $R_1 = 1\,\text{k}\Omega$, $R_F = 10\,\text{k}\Omega$, $R_d = 1\,\text{k}\Omega$, and $A_{OL} = -10^4$, evaluate the gain of this inverting amplifier. (*c*) Compare the result of part *b* with the ideal op amp approximation given by (*9.5*).

(*a*) Rearranging (*9.4*) to obtain the voltage-gain ratio gives

$$A_v \equiv \frac{v_o}{v_S} = \frac{A_{OL}}{1 + (R_1/R_F)(1 - A_{OL}) + R_1/R_d}$$

(*b*) Substitution of the given values yields

$$A_v = \frac{-10^4}{1 + (1/10)(1 + 10^4) + 1/1} = -9.979$$

(*c*) From (*9.5*),

$$A_{v\text{ideal}} = -\frac{R_F}{R_1} = -10$$

so the error is

$$\frac{-9.979 - (-10)}{-9.979}(100\%) = -0.21\%$$

Note that R_d and A_{OL} are far removed from the ideal, yet the error is quite small.

9.3 A *differential amplifier* (sometimes called a *subtractor*) responds to the difference between two input signals, removing any identical portions (often a bias or noise) in a process called *common-mode rejection*. Find an expression for v_o in Fig. 9-12 that shows this circuit to be a differential amplifier. Assume an ideal op amp.

Since the current into the ideal op amp is zero, a loop equation gives

$$v_1 = v_{S1} - Ri_1 = v_{S1} - R\,\frac{v_{S1} - v_o}{R + R_1}$$

By voltage division at the noninverting node,

$$v_2 = \frac{R_1}{R + R_1}\, v_{S2}$$

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In the ideal op amp, $v_d = 0$, so that $v_1 = v_2$, which leads to

$$v_o = \frac{R_1}{R}(v_{S2} - v_{S1})$$

Thus, the output voltage is directly proportional to the difference between the input voltages.

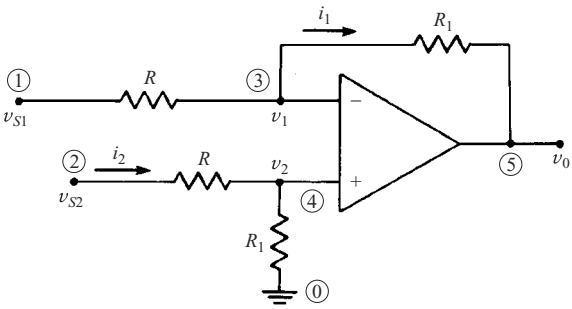


Fig. 9-12 Differential amplifier

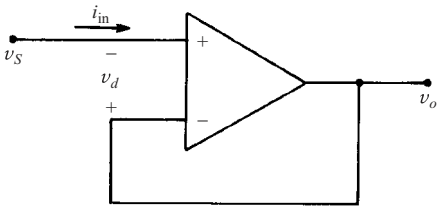


Fig. 9-13 Unity follower

9.4 Find the input impedance Z_1 of the inverting amplifier of Fig. 9-2, assuming the basic op amp is ideal.

Consider v_S a driving-point source. Since the op amp is ideal, the inverting terminal is a virtual ground, and a loop equation at the input leads to

$$v_S = i_1 R_1 + 0 \qquad \text{so that} \qquad Z_1 = \frac{v_S}{i_1} = R_1$$

9.5 The *unity-follower* amplifier of Fig. 9-13 has a voltage gain of 1, and the output is in phase with the input. It also has an extremely high input impedance, leading to its use as an intermediate-stage (*buffer*) amplifier to prevent a small load impedance from loading a source. Assume a practical op amp having $A_{OL} = -10^6$ (a typical value). (*a*) Show that $v_o \approx v_S$. (*b*) Find an expression for the amplifier input impedance, and evaluate it for $R_d = 1\,\text{M}\Omega$ (a typical value).

(*a*) Writing a loop equation and using (*9.1*), we have

$$v_S = v_o - v_d = v_o\left(1 - \frac{1}{A_{OL}}\right)$$

from which

$$v_o = \frac{v_S}{1 - 1/A_{OL}} = \frac{v_S}{1 + 10^{-6}} = 0.999999 v_S \approx v_S$$

(*b*) Considering v_S a driving-point source and using (*9.1*), we have

$$v_S = i_{\text{in}} R_d + v_o = i_{\text{in}} R_d - A_{OL} v_d = i_{\text{in}} R_d (1 - A_{OL})$$

and

$$Z_{\text{in}} = \frac{v_S}{i_{\text{in}}} = R_d(1 - A_{OL}) \approx -A_{OL} R_d = -(-10^6)(10^6) = 1\,\text{T}\Omega$$

9.6 Find an expression for the output v_o of the amplifier circuit of Fig. 9-14. Assume an ideal op amp. What mathematical operation does the circuit perform?

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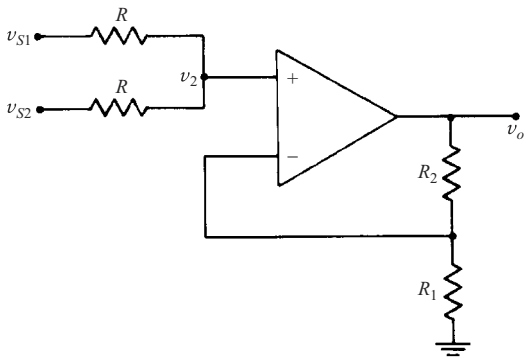


Fig. 9-14

The principle of superposition is applicable to this linear circuit. With $v_{S2} = 0$ (shorted), the voltage appearing at the noninverting terminal is found by voltage division to be

$$v_2 = \frac{R}{R+R}\, v_{S1} = \frac{v_{S1}}{2} \tag{1}$$

Let v_{o1} be the value of v_o with $v_{S2} = 0$. By the result of Example 9.3 and (*1*),

$$v_{o1} = \left(1 + \frac{R_2}{R_1}\right) v_2 = \left(1 + \frac{R_2}{R_1}\right) \frac{v_{S1}}{2}$$

Similarly, with $v_{S1} = 0$,

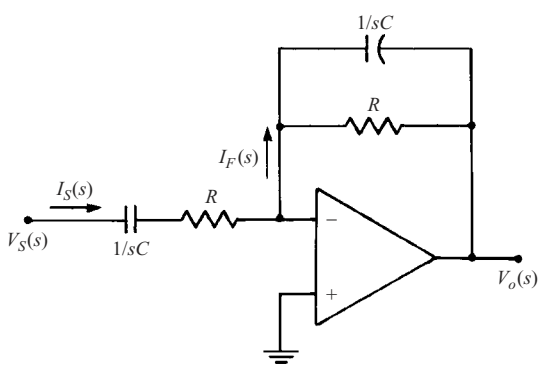
$$v_{o2} = \left(1 + \frac{R_2}{R_1}\right) \frac{v_{S2}}{2}$$

By superposition, the total output is then

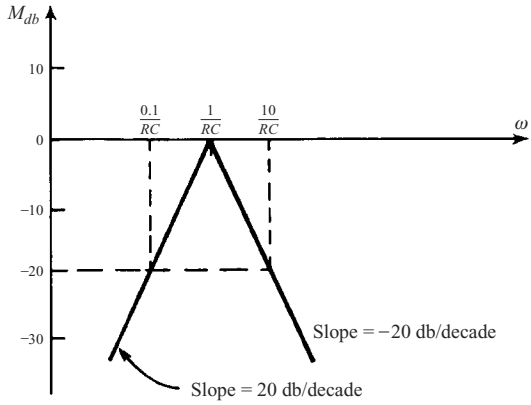
$$v_o = v_{o1} + v_{o2} = \frac{1}{2}\left(1 + \frac{R_2}{R_1}\right)(v_{S1} + v_{S2})$$

The circuit is a noninverting adder.

9.7 The circuit of Fig. 9-15(*a*) (represented in the *s* domain) is a more practical differentiator than that of Fig. 9-5, because it will attenuate high-frequency noise. (*a*) Find the *s*-domain transfer



(*a*)



(*b*)

Fig. 9-15

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function relating V_o and V_S. (*b*) Sketch the Bode plot (M_{db} only), and how high-frequency noise effects are reduced. Assume an ideal op amp.

(*a*) In an ideal op amp the inverting terminal is a virtual ground, so $I_S(s) = -I_F(s)$. As in Example 9.9,

$$Z_F(s) = \frac{R}{sRC+1}$$

Then $$I_F(s) = \frac{V_o(s)}{Z_F(s)} = \frac{sRC+1}{R}\,V_o(s)$$

But $$V_S(s) = I_S(s)Z_{\text{in}}(s) = -I_F(s)Z_{\text{in}}(s) = -\frac{sRC+1}{R}\,V_o(s)\,\frac{sRC+1}{sC}$$

whence $$A(s) \equiv \frac{V_o(s)}{V_S(s)} = -\frac{sRC}{(sRC+1)^2}$$

(*b*) From the result of part *a*,

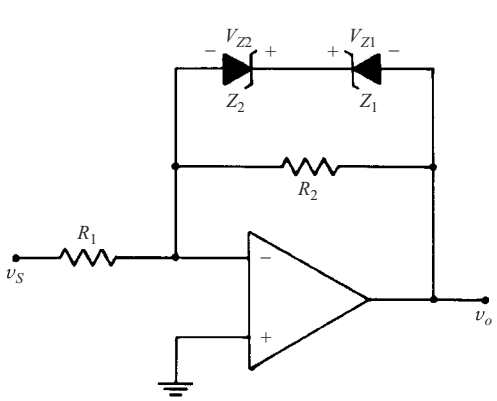
$$M_{db} \equiv 20\log|A(j\omega)| = 20\log\omega RC - 40\log|j\omega RC+1| \approx \begin{cases} 20\log\omega RC & \text{for } \omega RC \le 1 \\ -20\log\omega RC & \text{for } \omega RC \ge 1 \end{cases}$$

Figure 9-15(*b*) is a plot of this approximate (asymptotic) expression for M_{db}. For a true differentiator, we would have

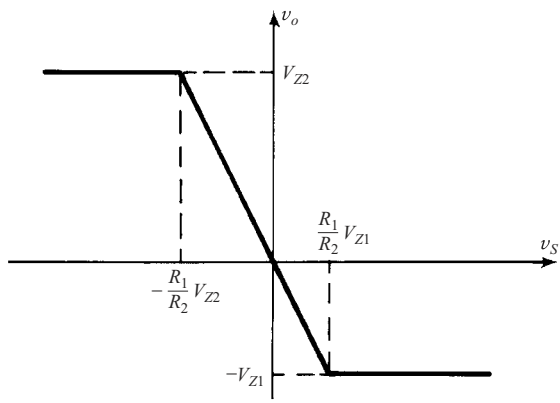
$$v_o = K\frac{dv_S}{dt} \qquad \text{or} \qquad V_o = sKV_S$$

which would lead to $M_{db} = 20\log\omega K$. Thus the practical circuit differentiates only components of the signal whose frequency is less than the break frequency $f_1 \equiv 1/2\pi RC$ Hz. Spectral components above the break frequency—including (and especially) noise—will be attenuated; the higher the frequency, the greater the attenuation.

9.8 In analog signal processing, the need often arises to introduce a *level clamp* (linear amplification to a desired output level or value and then no further increase in output level as the input continues to increase). One level-clamp circuit, shown in Fig. 9-16(*a*), uses series Zener diodes in a negative feedback path. Assuming ideal Zeners and op amp, find the relationship between v_o and v_S. Sketch the results on a transfer characteristic.



(*a*)



(*b*)

Fig. 9-16

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Since the op amp is ideal, the inverting terminal is a virtual ground, and v_o appears across the parallel-connected feedback paths. There are two distinct possibilities:

Case I: $v_S > 0$. For $v_o < 0$, Z_2 is forward-biased and Z_1 reverse-biased. The Zener feedback path is an open circuit until $v_o = -V_{Z1}$; then Z_1 will limit v_o at $-V_{Z1}$ so that no further negative excursion is possible.

Case II: $v_S < 0$. For $v_o > 0$, Z_1 is forward-biased and Z_2 reverse-biased. The Zener feedback path acts as an open circuit until v_o reaches V_{Z2}, at which point Z_2 limits v_o to that value. In summary, for both cases,

$$v_o = \begin{cases} V_{Z2} & \text{for } v_S < -\dfrac{R_1}{R_2} V_{Z2} \\ -\dfrac{R_2}{R_1} v_S & \text{for } -\dfrac{R_1}{R_2} V_{Z2} \le v_S \le \dfrac{R_1}{R_2} V_{Z1} \\ -V_{Z1} & \text{for } v_S > \dfrac{R_1}{R_2} V_{Z1} \end{cases}$$

Figure 9-16(*b*) gives the transfer characteristic.

9.9 The circuit of Fig. 9-17 is an *adjustable-output voltage regulator*. Assume that the basic op amp is ideal. Regulation of the Zener is preserved if $i_Z \ge 0.1 I_Z$ (Section 2.10). (*a*) Find the regulated output v_o in terms of V_Z. (*b*) Given a specific Zener diode and the values of R_S and R_1, over what range of V_S would there be no loss of regulation?

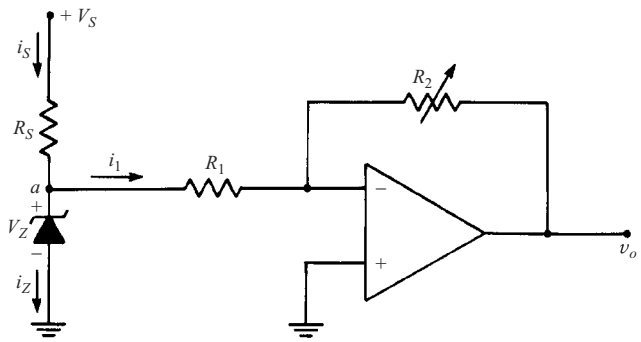


Fig. 9-17

(*a*) Since V_Z is the voltage at node *a*, (*9.5*) gives

$$v_o = -\frac{R_2}{R_1} V_Z$$

So long as $i_Z \ge 0.1 I_Z$, a regulated value of v_o can be achieved by adjustment of R_2.

(*b*) Regulation is preserved and the diode current $i_Z = i_S - i_1$ does not exceed its rated value I_Z if

$$0.1 I_Z \le i_S - i_1 \le I_Z \qquad \text{or} \qquad 0.1 I_Z \le \frac{V_S - V_Z}{R_S} - \frac{V_Z}{R_1} \le I_Z$$

or

$$0.1 I_Z R_S + \left(1 + \frac{R_S}{R_1}\right) V_Z \le V_S \le I_Z R_S + \left(1 + \frac{R_S}{R_1}\right) V_Z$$

9.10 The circuit of Fig. 9-18(*a*) is a *limiter*; it reduces the signal gain to some limiting level rather than imposing the abrupt clamping action of the circuit of Problem 9.8. (*a*) Determine the limiting value V_ℓ of v_o at which the diode *D* becomes forward-biased, thus establishing a second feedback

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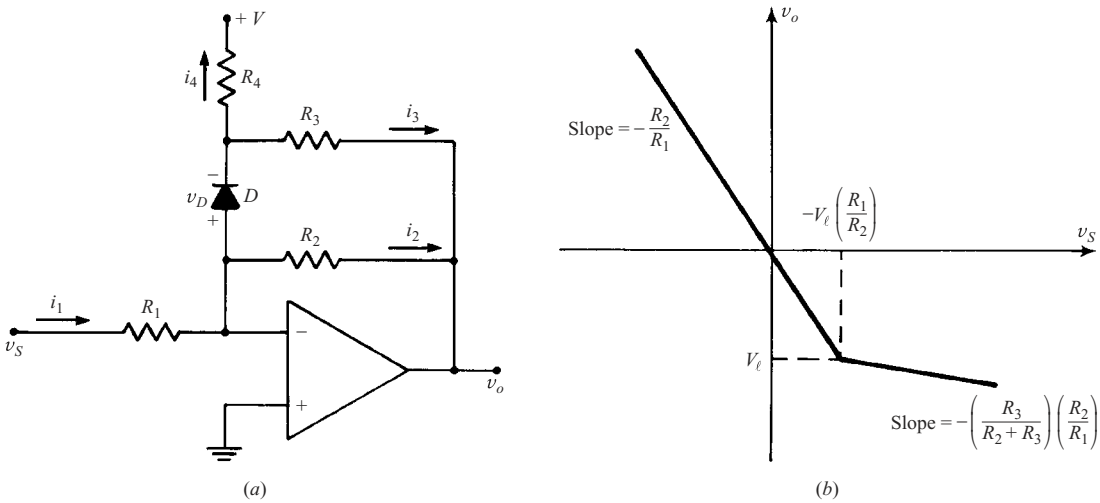


Fig. 9-18

path through R_3. Assume an ideal op amp and a diode characterized by Fig. 2-2(*a*). (*b*) Determine the relationship between v_o and v_S, and sketch the transfer characteristic.

(*a*) The diode voltage v_D is found by writing a loop equation. Since the inverting input is a virtual ground, v_o appears across R_2 and

$$v_D = -v_o - i_3 R_3 = v_o - \frac{V - v_o}{R_3 + R_4} R_3 \tag{1}$$

When $v_D = 0$, $v_o = V_\ell$, and (*1*) gives

$$V_\ell = -\frac{R_3}{R_4} V \tag{2}$$

(*b*) For $v_o > V_\ell$, the diode blocks and R_2 constitutes the only feedback path. Since $i_1 = i_2$,

$$\frac{v_S}{R_1} = -\frac{v_o}{R_2} \tag{3}$$

For $v_o \le V_\ell$, the diode conducts and the parallel combination of R_2 and R_3 forms the feedback path. Since now $i_1 = i_2 + i_3 + i_4$,

$$\frac{v_S}{R_1} = -\left(\frac{v_o}{R_2} + \frac{v_o}{R_3} + \frac{V}{R_4}\right) \tag{4}$$

It follows from (*2*), (*3*), and (*4*) that

$$v_o = \begin{cases} -\dfrac{R_2}{R_1} v_S & \text{for } v_S < \dfrac{R_1 R_3}{R_2 R_4} V \\ -\dfrac{R_3}{R_2 + R_3}\dfrac{R_2}{R_1} v_S - \dfrac{R_2}{R_2 + R_3}\dfrac{R_3}{R_4} V & \text{for } v_S \ge \dfrac{R_1 R_3}{R_2 R_4} V \end{cases}$$

This transfer characteristic is plotted in Fig. 9-18(*b*).

9.11 What modifications and specifications will change the circuit of Fig. 9-16(*a*) into a 3-V square-wave generator, if $v_S = 0.02 \sin \omega t$ V? Sketch the circuit transfer characteristic and the input and output waveforms.

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Modify the circuit by removing R_2, and specify Zener diodes such that $V_{Z1} = V_{Z2} = 3\,\text{V}$. The transfer characteristic of Fig. 9-16(*b*) will change to that of Fig. 9-19(*a*). The time relationship between v_S and v_o will be that displayed in Fig. 9-19(*b*).

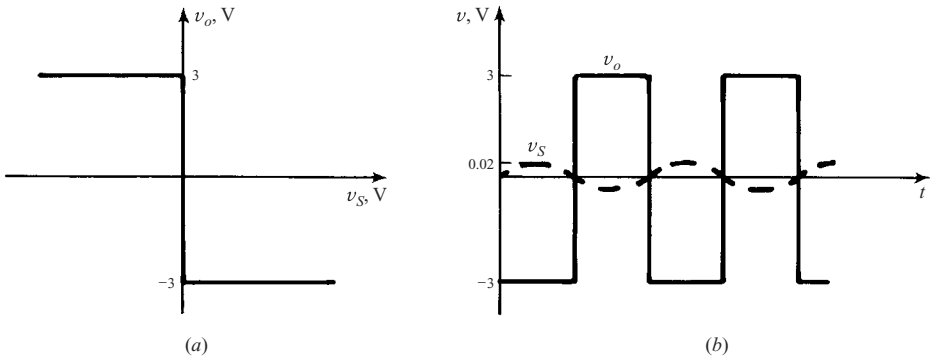


Fig. 9-19

9.12 Design a first-order low-pass filter with dc gain of magnitude 2 and input impedance 5 kΩ. The gain should be flat to 100 Hz.

The filter is shown in Fig. 9-8. For an ideal op amp, Problem 9.4 gives $Z_1 = R_1 = 5\,\text{k}\Omega$. The dc gain is given by (*9.20*) as $A(0) = -R/R_1$, whence $R = 2R_1 = 10\,\text{k}\Omega$. Figure 9-8(*b*) shows that the magnitude of the gain is flat to $\omega = 0.1/RC$, so the capacitor must be sized such that

$$C = \frac{0.1}{2\pi fR} = \frac{0.1}{2\pi(100)(10 \times 10^3)} = 15.9\,\text{nF}$$

9.13 The analog computer utilizes operational amplifiers to solve differential equations. Devise an analog solution for $i(t)$, $t > 0$, in the circuit of Fig. 9-20(*a*). Assume that you have available an inverting integrator with unity gain ($R_1C_1 = 1$), inverting amplifiers, a variable dc source, and a switch.

For $t > 0$, the governing differential equation for the circuit of Fig. 9-20(*a*) may be written as

$$-\frac{di}{dt} = -\frac{V_b}{L} + \frac{R}{L}\,i \tag{1}$$

The sum on the right side of (*1*) can be simulated by the left-hand inverting adder of Fig. 9-20(*b*), where $v_{o1} = -di/dt$ and where R_2 and R_3 are chosen such that $R_3/R_2 = R/L$. Then $v_{o2} = -\int v_{o1}\,dt$ will be an analog of $i(t)$, on a scale of 1 A/V.

9.14 Find the relationship between v_o and v_i in the circuit of Fig. 9-21.

Since the inverting terminal is a virtual ground, the Laplace-domain input current is given by

$$I_i = \frac{V_i}{R + (R \| 1/sC)} = \frac{V_i(sRC + 1)}{sR^2C + 2R}$$

With zero current flowing into the op amp inverting terminal, current division yields

$$I_2 = I_1 = \frac{1/sC}{R + 1/sC}\,I_i = \frac{1}{sRC + 1}\,\frac{V_i(sRC + 1)}{R(sRC + 2)} = \frac{V_i}{R(sRC + 2)}$$

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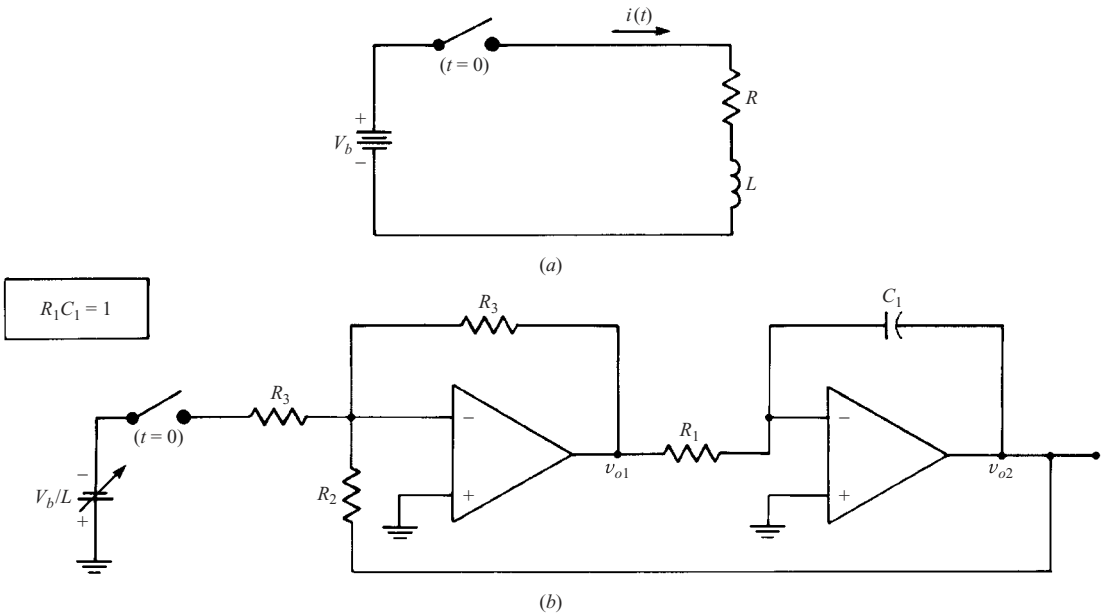


Fig. 9-20

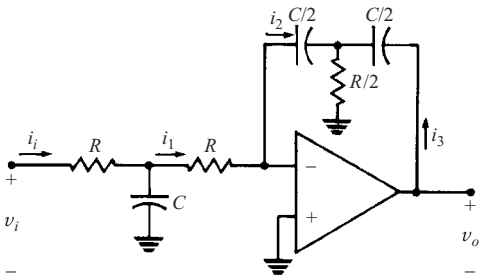


Fig. 9-21

Again, because the inverting terminal is a virtual ground,

$$I_3 = \frac{V_o}{\dfrac{1}{sC/2} + \dfrac{1}{sC/2} \Big\| \dfrac{R}{2}} = \frac{sC(sRC+4)}{4(sRC+2)} V_o$$

and, by current division,

$$I_2 = \frac{-R/2}{2/sC + R/2} I_3 = \frac{-sRC}{sRC+4} \frac{sC(sRC+4)}{4(sRC+2)} V_o = \frac{-s^2RC^2V_o}{4(sRC+2)}$$

Equating the two expressions for I_2 yields a Laplace-domain expression relating V_o and V_i:

$$V_o = -\frac{4}{s^2R^2C^2} V_i \tag{1}$$

or, after inverse transformation,

$$v_o = -\frac{4}{(RC)^2} \int \left(\int v_i \, dt \right) dt$$

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9.15 The circuit of Fig. 9-22 is, in essence, a noninverting amplifier with a feedback impedance Z_N and is known as a *negative-impedance converter* (NIC). Find the Thévenin or driving-point impedance to the right of the input terminals, and explain why such a name is appropriate.

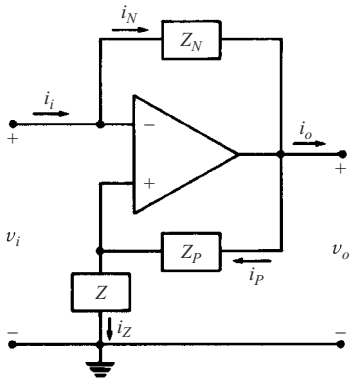


Fig. 9-22

At the inverting node, the phasor input current is given by

$$I_i = I_N = \frac{V_i - V_o}{Z_N}$$

so that

$$V_o = V_i - I_i Z_N \tag{1}$$

Since $V_d \approx 0$,

$$I_P = \frac{V_o - V_i}{Z_P} = I_Z = \frac{V_i}{Z}$$

so that

$$V_o = \frac{Z_P}{Z} V_i + V_i \tag{2}$$

If (*1*) and (*2*) are equated and rearranged, they result in

$$Z_{dp} = \frac{V_i}{I_i} = -\frac{Z_N}{Z_P} Z \tag{3}$$

Observe that if $Z_P = Z_N$, then the impedance Z appears to be converted to the negative of its value; hence the name. See Problem 9.16 for another example.

9.16 (*a*) Describe a circuit arrangement that makes use of the NIC of Problem 9.15 and Fig. 9-22, with only resistors and capacitors, to simulate a pure inductor. (*b*) If only four 10-kΩ resistors and a 0.01-μF capacitor are available for use in the circuit, determine the value of L that can be simulated.

(*a*) Consider the circuit of Fig. 9-23. According to (*3*) of Problem 9.15,

$$Z'_{\text{IN}} = \frac{Z_N}{Z_P} Z = -\frac{R}{R} R = -R$$

and

$$Z_{\text{IN}} = -\frac{Z_N}{Z_P} Z = -\frac{R}{1/sC}(-R) = sR^2C \equiv sL_{eq}$$

(*b*) The value of L_{eq} is

$$L_{eq} = R^2C = (10^4)^2(0.01 \times 10^{-6}) = 1\,\text{H}$$

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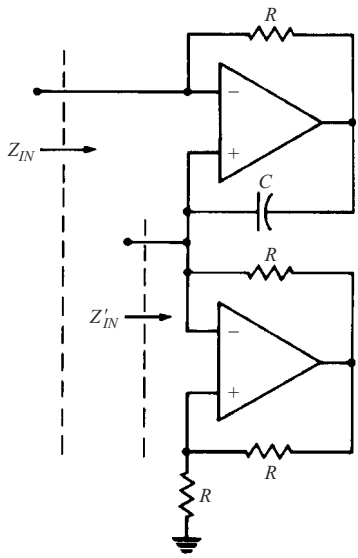


Fig. 9-23

9.17 The logarithmic amplifier of Fig. 9-7 has two undesirable aspects: V_T and I_o are temperature-dependent, and $\ln RI_o$ may not be negligibly small. A circuit that can overcome these shortcomings is presented in Fig. 9-24. Show that if Q_1 and Q_2 are matched transistors, then v_o is truly proportional to $\ln v_S$.

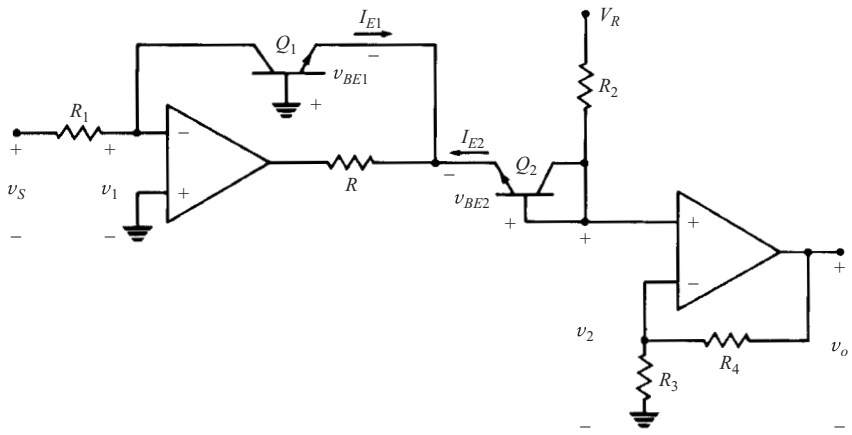


Fig. 9-24

In matched transistors, reverse saturation currents are equal. By KVL, with $v_1 \approx 0$,

$$v_2 = v_{BE2} - v_{BE1} \tag{1}$$

Taking the logarithm of both sides of (*9.15*) leads to

$$v_{BE} = V_T \ln \frac{I_E}{I_S} \tag{2}$$

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Now the use of (*2*) in (*1*), with $I_C \approx I_E$, gives

$$v_2 = V_T \ln \frac{I_{E2}}{I_S} - V_T \ln \frac{I_{E1}}{I_S} = -V_T \ln \frac{I_{C1}}{I_{C2}} \tag{3}$$

According to (*1*), v_2 is the difference between two small voltages. Thus, if V_R is several volts in magnitude, then $v_2 \ll V_R$, and

$$I_{C2} \approx I_{E2} = \frac{V_R - v_2}{R_2} \approx \frac{V_R}{R_2} \tag{4}$$

Also, since $v_1 \approx 0$,

$$I_{C1} \approx I_{E1} = \frac{v_S - v_1}{R_1} \approx \frac{v_S}{R_1} \tag{5}$$

Thus, by (*9.7*) along with (*3*) to (*5*),

$$v_o = \frac{R_3 + R_4}{R_3} v_2 = -V_T \frac{R_3 + R_4}{R_3} \ln \frac{I_{C1}}{I_{C2}} = -V_T \left(1 + \frac{R_4}{R_3}\right) \left[\ln v_S - \ln\left(\frac{R_1}{R_2} V_R\right)\right] \tag{6}$$

The selection of $(R_1/R_2)V_R = 1$ forces the last term on the right-hand side of (*6*) to zero. Also, R_3 can be selected with a temperature sensitivity similar to that of V_T, to offset changes in V_T. Further, it is simple to select $R_4/R_3 \gg 1$, so that (*6*) becomes

$$v_o \approx -V_T \frac{R_4}{R_3} \ln v_S$$

9.18 The circuit of Fig. 9-25 is an *exponential* or *inverse log* amplifier. Show that the output v_o is proportional to the inverse logarithm of the input v_i.

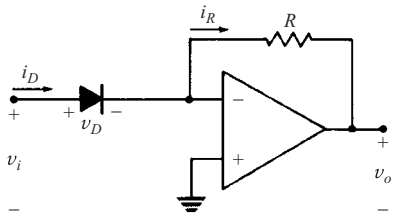


Fig. 9-25

Since the input current to the op amp is negligible,

$$i_R \approx i_D = I_o e^{v_D/\eta V_T}$$

But since the inverting terminal is a virtual ground, $v_D = v_i$. Thus,

$$v_o = -i_R R \approx -RI_o e^{v_i/\eta V_T} = -RI_o \ln^{-1} \frac{v_i}{\eta V_T}$$

9.19 Having now at your disposal a logarithmic amplifier (Example 9.8 and Problem 9.17) and an exponential (inverse log) amplifier (Problem 9.18), devise a circuit that will multiply two numbers together.

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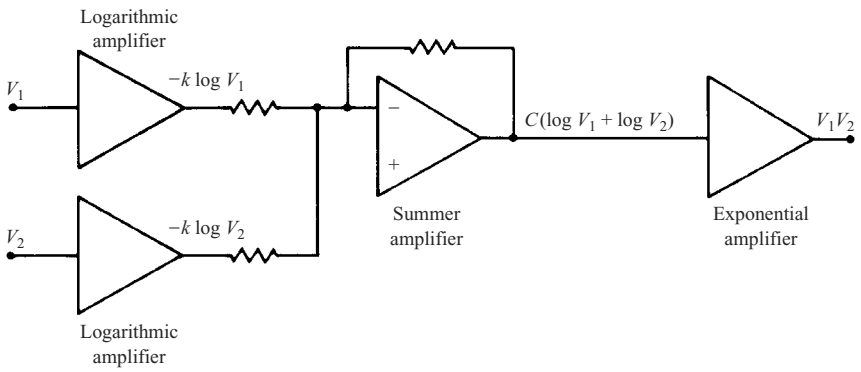


Fig. 9-26

Since $xy = e^{\ln x + \ln y}$, the circuit of Fig. 9-26 is a possible realization.

9.20 Two identical passive RC low-pass filter sections are to be connected in cascade so as to create a double-pole filter with corner frequency at $1/\tau = 1/RC$. (*a*) Will simple cascade connection of these filters yield the desired transfer function $T(s) = (1/\tau)^2/(s + 1/\tau)^2$? (*b*) If not, how may the desired result be realized?

(*a*) With simple cascading, the overall transfer function would be

$$\frac{V_o}{V_i} = T' = \frac{(1/\tau)^2}{s^2 + 3(1/\tau)s + (1/\tau)^2}$$

which has two distinct negative roots. The desired result is not obtained because the impedance looking into the second stage is not infinite, and thus, the transfer function of the first stage is not simply $(1/\tau)/(s + 1/\tau)$.

(*b*) The desired result can be obtained by adding a unity follower (Fig. 9-13) between stages (see Problem 9.44), as illustrated in Fig. 9-27.

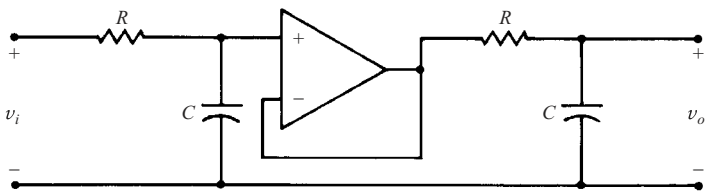


Fig. 9-27

9.21 (*a*) Find the transfer function for the circuit of Fig. 9-28. (*b*) In control theory, there is a compensation network whose transfer function is of the form $(s + 1/\tau_1)/(s + 1/\tau_2)$; it is called a lead-lag network if $1/\tau_1 < 1/\tau_2$, and a lag-lead network if $1/\tau_2 < 1/\tau_1$. Explain how the circuit of Fig. 9-28 may be used as such a compensation network.

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(*a*) By extension of (*9.5*),

$$T(s) = \frac{V_o}{V_S} = -\frac{Z_2}{Z_1} = -\frac{\dfrac{R_2}{sR_2C_2 + 1}}{\dfrac{R_1}{sR_1C_1 + 1}} = -\frac{C_1}{C_2}\frac{s + 1/\tau_1}{s + 1/\tau_2} \tag{1}$$

where $\tau_1 = R_1C_1$ and $\tau_2 = R_2C_2$.

(*b*) To obtain unity gain, set $C_1 = C_2$. To obtain a positive transfer function, insert an inverter stage either before or after the circuit. Then, the selection of $R_1 > R_2$ yields $1/\tau_1 < 1/\tau_2$, giving the lead-lag network, and $R_1 < R_2$ results in $1/\tau_2 < 1/\tau_1$, giving the lag-lead network.

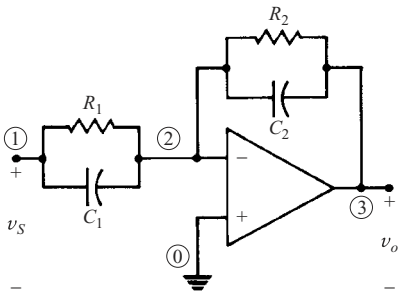


Fig. 9-28

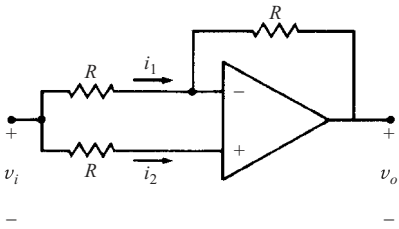


Fig. 9-29

9.22 Show that the transfer function for the op amp circuit of Fig. 9-29 is $v_o/v_i = 1$.

Because the op amp draws negligible current, $i_2 = 0$. Hence, $v_2 = v_i$. However, since $v_d \approx 0$, $v_1 \approx v_2 = v_i$ and

$$i_1 = \frac{v_i - v_1}{R} \approx 0$$

Also, by the method of node voltages,

$$i_1 = \frac{v_i - v_o}{2R} = 0$$

Thus, $v_i = v_o$ and so $v_o/v_i = 1$.

9.23 Use an op amp to design a noninverting voltage source (see Problem 9.9). Determine the conditions under which regulation is maintained in your source.

Simply replace the inverting amplifier of Fig. 9-17 with the noninverting amplifier of Fig. 9-3. Since the op amp draws negligible current, regulation is preserved if V_S and R_S are selected so that i_Z remains within the regulation range of the Zener diode. Specifically, regulation is maintained if $0.1I_Z \le V_S/R_S \le I_Z$.

9.24 For the noninverting amplifier of Fig. 9-3: (*a*) Compare the expressions obtained for voltage gain with common-mode rejection (Example 9.4) and without (in the ideal amplifier of Example 9.3), for $A_{OL} \to -\infty$. (*b*) Show that if CMRR is very large, then it need not be considered in computing the gain.

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(*a*) We let $A_{OL} \to -\infty$ in (*9.13*), since that is implicit in Example 9.3:

$$\lim_{A_{OL}\to-\infty} A_v = \lim_{A_{OL}\to-\infty}\left[\frac{-A_{OL}}{1 - A_{OL}R_1/(R_1+R_2)} + \frac{-A_{OL}/\text{CMRR}}{1 - A_{OL}R_1/(R_1+R_2)}\right]$$
$$= 1 + \frac{R_2}{R_1} + \frac{1}{\text{CMRR}}\left(1 + \frac{R_2}{R_1}\right) \tag{1}$$

Now we can compare (*1*) above with (*9.7*); the difference is the last term on the right-hand side of (*1*) above.

(*b*) Let $\text{CMRR} \to \infty$ in (*1*) above to get

$$\lim_{\substack{\text{CMRR}\to\infty \\ A_{OL}\to-\infty}} A_v = 1 + \frac{R_2}{R_1}$$

which is identical to the ideal case of Example 9.3.

9.25 The amplifier of Fig. 9-9 has been shown in Example 9.10 to be a signal-conditioning amplifier with gain sensitive to the polarity of v_S. Use SPICE methods to simulate this amplifier if $R_1 = 10\,\text{k}\Omega$ and $R_2 = R_3 = 20\,\text{k}\Omega$. Use the op amp model of Section 9.12. The ideal diode can be realized by specifying the emission coefficient $n = 1 \times 10^{-10}$. Use the simulation results to validate (*9.21*) and (*9.22*).

The netlist code that describes the circuit is as follows:

```
Prb9_25.CIR
vs 1 0 SIN( 0V 0.5V 1000Hz )
R1 1 2 10kohm
R2 2 4 20kohm
D2 4 3 DMOD
R3 2 3 20kohm
X1 2 0 3 0 OPAMP
.SUBCKT  OPAMP  1    2     3     4
*        Model  Inv  NInv  Out   Com
Rd 1 2 500kohm
E  5 4 (1,2) -1e5
Ro 5 3 100ohm
.ENDS OPAMP
.MODEL DMOD D(n=1e-10) ; Ideal diode
.TRAN 1us 2ms
.PROBE
.END
```

Execute ⟨Prb9_25.CIR⟩ and use the Probe feature of PSpice to yield Fig. 9-30 where it is seen that for $v_S > 0$, $A_v = -0.5/0.5 = -1$. By (*9.21*), the predicted gain is

$$A_v = -\frac{R_2R_3}{R_1(R_2+R_3)} = -\frac{(20\times10^3)(20\times10^3)}{(10\times10^3)(20\times10^3+20\times10^3)} = -1$$

Thus, (*9.21*) is validated.

From Fig. 9-30 for $v_S < 0$, $A_v = -1/0.5 = -2$. By (*9.22*), the expected gain is

$$A_v = -\frac{R_3}{R_1} = -\frac{20\times10^3}{10\times10^3} = -2$$

Hence, (*9.22*) is also validated.

9.26 Add an inverting amplifier (see Fig. 9-2) to the output for the circuit of Fig. 9-28 to give a positive transfer function. Select the resistor values for this inverting amplifier to adjust the low-

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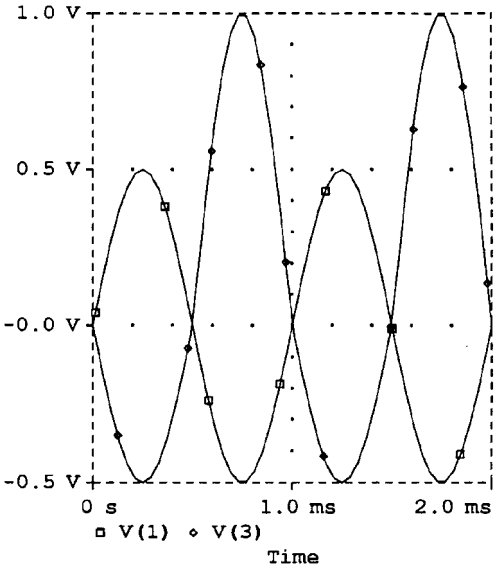


Fig. 9-30

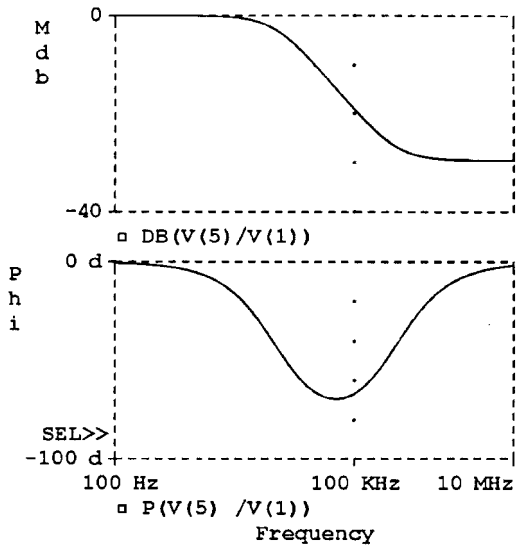


Fig. 9-31

frequency voltage gain of the complete network to unity. Let $C_1 = C_2 = 0.001\,\mu$F, $R_1 = 500\,\text{k}\Omega$, and $R_2 = 15\,\text{k}\Omega$. Then from Problem 9.21, $1/\tau_1 = 1/R_1C_1 = 2 \times 10^6$ rad/s $> 1/\tau_2 = 1/R_2C_2 = 66.7$ krad/s, making the circuit a lag-lead network. Use SPICE methods to generate the Bode plot of this circuit over the frequency range from 100 Hz to 10 MHz. The op amp model of Section 9.12 is applicable.

Netlist code describing the circuit is shown below:

```
Prb9_26.CIR
vs 1 0 AC 1V
R1 1 2 500ohm
C1 1 2 0.001uF
R2 2 3 15kohm
C2 2 3 0.001uF
X1 2 0 3 0 OPAMP
* Inverting amplifier to set
* dc gain to unity
R3 3 4 15kohm
R4 4 5 500ohm
X2 4 0 5 0 OPAMP
.SUBCKT  OPAMP  1    2     3    4
*        Model  Inv  NInv  Out  Com
Rd 1 2 500kohm
E  5 4 (1,2) -1e5
Ro 5 3 10ohm
.ENDS OPAMP
.AC DEC 250 100Hz 10MegHz
.PROBE
.END
```

Execute ⟨Prb9_26.CIR⟩ and use the Probe feature of PSpice to generate the gain magnitude plot (Mdb) and the phase plot (Phi) shown in Fig. 9-31. Notice that the phase angle plot begins to lag toward -90° at $0.1/\tau_2$ and then moves in a leading sense back to 0° at $10/\tau_1$. Thus, the lag-lead characteristic is exemplified.

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Supplementary Problems

9.27 For the noninverting amplifier of Fig. 9-3, (*a*) find an exact expression for the voltage-gain ratio, and (*b*) evaluate it for $R_1 = 1\,\text{k}\Omega$, $R_2 = 10\,\text{k}\Omega$, $R_d = 1\,\text{k}\Omega$, and $A_{OL} = -10^4$. (*c*) Compare your result in part *b* with the value produced by the ideal expression (*9.7*).

Ans. (*a*) $A_v = \dfrac{R_1 + R_2}{R_1 - \dfrac{R_1 R_2}{A_{OL} R_d} - \dfrac{R_1 + R_2}{A_{OL}}}$; (*b*) 10.977;

(*c*) $A_{v\text{ideal}} = 11$, for a $+0.21\%$ difference

9.28 In the first-order low-pass filter of Example 9.9, $R = 10\,\text{k}\Omega$, $R_1 = 1\,\text{k}\Omega$, and $C = 0.1\,\mu\text{F}$. Find (*a*) the gain for dc signals, (*b*) the break frequency f_1 at which the gain drops off by 3 db, and (*c*) the frequency f_u at which the gain has dropped to unity (called the *unity-gain bandwidth*).
Ans. (*a*) -10; (*b*) 159.2 Hz; (*c*) 1583.6 Hz

9.29 The noninverting amplifier circuit of Fig. 9-3 has an infinite input impedance if the basic op amp is ideal. If the op amp is not ideal, but instead $R_d = 1\,\text{M}\Omega$ and $A_{OL} = -10^6$, find the input impedance. Let $R_2 = 10\,\text{k}\Omega$ and $R_1 = 1\,\text{k}\Omega$. *Ans.* $1\,\text{T}\Omega$

9.30 Let $R_1 = R_2 = R_3 = 3R_F$ in the inverting summer amplifier of Fig. 9-4. What mathematical operation does this circuit perform? *Ans.* Gives the negative of the instantaneous average value

9.31 An inverting summer (Fig. 9-4) has n inputs with $R_1 = R_2 = R_3 = \cdots = R_n = R$. Assume that the open-loop basic op amp gain A_{OL} is finite, but that the inverting-terminal input current is negligible. Derive a relationship that shows how gain magnitude is reduced in the presence of multiple inputs.

Ans. $A_n \equiv \dfrac{v_o}{v_{S1} + v_{S2} + \cdots v_{Sn}} = -\dfrac{R_F/R}{1 - \dfrac{nR_F}{(R+1)A_{OL}}}$

For a single input v_{S1}, the gain is A_1. For the same input v_{S1} together with $n-1$ zero inputs $v_{S2} = \cdots = v_{Sn} = 0$, the gain is A_n. But since $A_{OL} < 0$, $|A_n| < |A_1|$ for $n > 1$

9.32 The basic op amp in Fig. 9-32 is ideal. Find v_o and determine what mathematical operation is performed by the amplifier circuit. *Ans.* $v_o = (1 + R_2/R_1)(v_{S2} - v_{S1})$, a subtractor

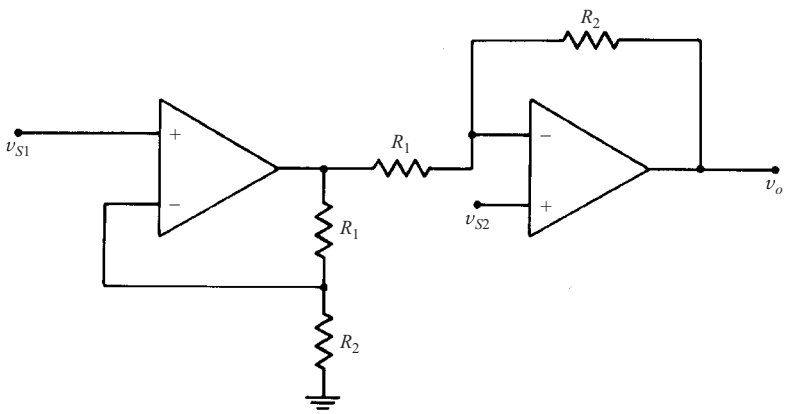


Fig. 9-32

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9.33 Describe the transfer characteristic of the level-clamp circuit of Fig. 9-16(*a*) if diode Z_2 is shorted.
Ans. Let $V_{Z2} = 0$ in Fig. 9-16(*b*)

9.34 Find the gain of the inverting amplifier of Fig. 9-33 if the op amp and diodes are ideal.
Ans. $A_v = -R_2/R_1$ for $v_S > 0$; $A_v = -R_3/R_1$ for $v_S \leq 0$

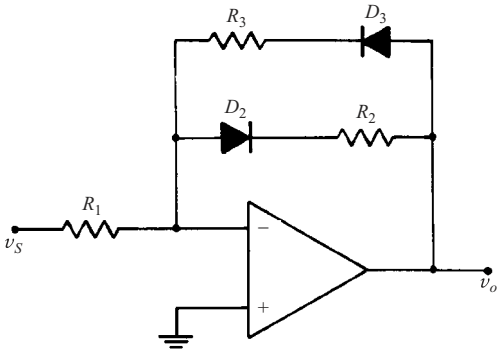


Fig. 9-33

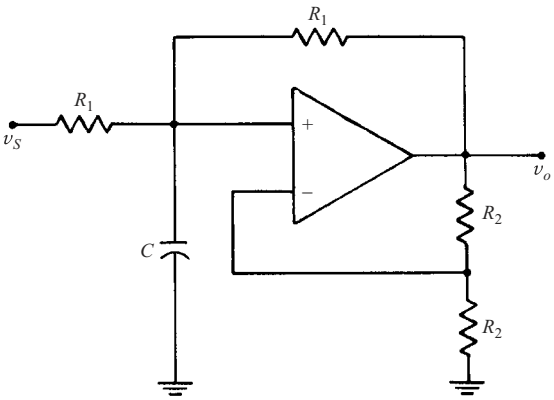


Fig. 9-34

9.35 The op amp in the circuit of Fig. 9-34 is ideal. Find an expression for v_o in terms of v_S, and determine the function of the circuit. *Ans.* $v_o = (2/R_1C)\int v_S\,dt$, a noninverting integrator

9.36 If the nonideal op amp of the circuit of Fig. 9-35 has an open-loop gain $A_{OL} = -10^4$, find v_o.
Ans. $0.9999E_b$

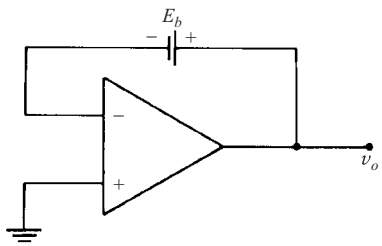


Fig. 9-35

9.37 How can the square-wave generator of Problem 9.11 be used to make a triangular-wave generator?
Ans. Cascade the integrator of Fig. 9-6 to the output of the square-wave generator

9.38 Describe an op amp circuit that will simulate the equation $3v_1 + 2v_2 + v_3 = v_o$.
Ans. The summer of Fig. 9-4, with $R_F/R_1 = 3$, $R_F/R_2 = 2$, and $R_F/R_3 = 1$, cascaded into the inverting amplifier of Fig. 9-2, with $R_F/R_1 = 1$

9.39 The circuit of Fig. 9-36 (called a *gyrator*) can be used to simulate an inductor in active RC filter design. Assuming ideal op amps, find (*a*) the *s*-domain input impedance $Z(s)$ and (*b*) the value of the inductance that is simulated if $C = 1\,\text{nF}$, $R_1 = 2\,\text{k}\Omega$, $R_2 = 100\,\text{k}\Omega$, and $R_3 = R_4 = 10\,\text{k}\Omega$.
Ans. (*a*) $Z(s) = sR_1R_2R_3C/R_4$; (*b*) 200 mH

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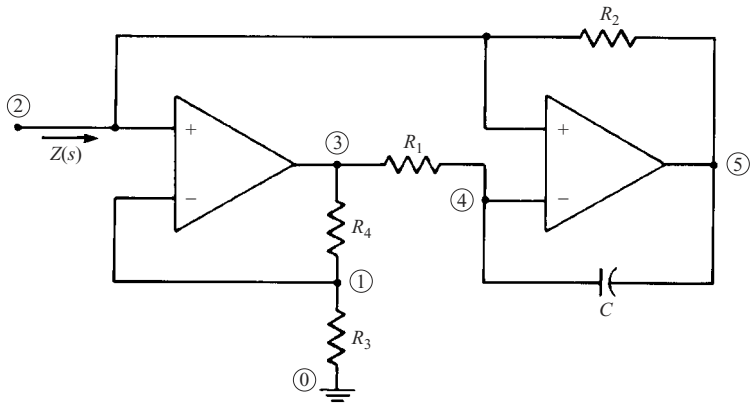


Fig. 9-36

9.40 For the double integrator circuit of Problem 9.14, if the output is connected to the input so that $v_i = v_o$, an oscillator is formed. Show that this claim is so, and that the frequency of oscillation is $f = 1/\pi RC$ Hz. [*Hint*: Replace V_o with V_i in (*1*) of Problem 9.14 to get an expression of the form $V_i f(s) = 0$.]

9.41 In the logarithmic amplifier circuit of Fig. 9-7, v_o must not exceed approximately 0.6 V, or else i_D will not be a good exponential function of v_D. Frequently, a second-stage inverting amplifier is added as shown in Fig. 9-7, so that v_o' is conveniently large. If the second-stage gain is selected to be $A_v = -R_F/R_1 = -1/V_T$, then its output becomes $v_o' = \ln v_i$. In the circuit of Fig. 9-7, v_D is exponential for $0 \le i_D \le 1$ mA, $0 \le v_i \le 10$ V, and $I_o = 100$ pA. Size R, R_F, and R_1 so that v_o' is as given above.
Ans. $R = 10\,\text{m}\Omega$; arbitrarily select $R_1 = 1\,\text{k}\Omega$, and then $R_F = 38.46\,\text{k}\Omega$

9.42 In the logarithmic amplifier of Fig. 9-24, let $v_S = 5$ V, $V_R = 10$ V, $R_1 = 1\,\text{k}\Omega$, $R_2 = 10\,\text{k}\Omega$, $R_3 = 1\,\text{k}\Omega$, and $R_4 = 50\,\text{k}\Omega$. The matched BJTs are operating at 25°C, with $V_T = 0.026$ V. Find (*a*) v_2 and (*b*) v_o (see Problem 9.17). *Ans.* (*a*) -41.8 mV; (*b*) -2.13 V

9.43 Having at your disposal a logarithmic amplifier and an exponential amplifier, devise a circuit that will produce the quotient of two numbers. (*Hint*: $x/y = e^{\ln x - \ln y}$.) *Ans.* See Fig. 9-37

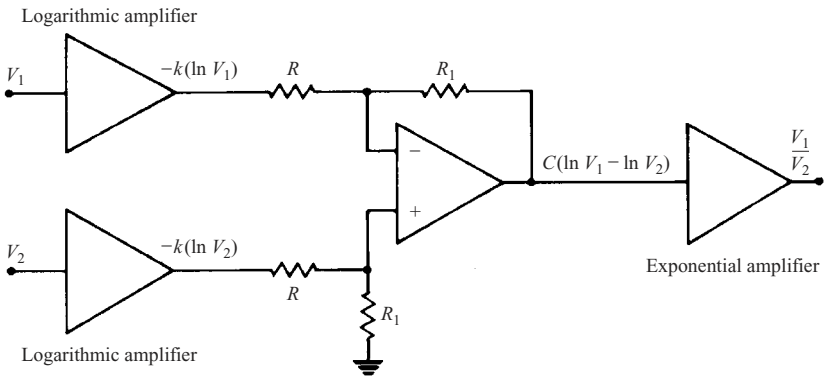


Fig. 9-37

9.44 The unity follower of Fig. 9-13 is the noninverting amplifier of Fig. 9-3 if $R_1 \to \infty$ and $R_2 \to 0$. (*a*) Find the output impedance R_{out} of the noninverting amplifier of Fig. 9-3 subject to the approximation $i_i = 0$.

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Model the op amp with the practical equivalent circuit of Fig. 9-1(*a*). (*b*) Let $R_1 \to \infty$ and $R_2 \to 0$ in your answer to part *a*, to find the output impedance of the unity follower.
Ans. (*a*) $R_{\text{out}} = R_o(R_1 + R_2)/[R_o + R_2 + R_1(1 - A_{OL})]$; (*b*) $R_{\text{out}} \approx R_o/(1 - A_{OL})$

9.45 The circuit of Fig. 9-28 is to be used as a high-pass filter having a gain of 0.1 at low frequencies, unity gain at high frequencies, and a gain of 0.707 at 1 krad/s. Arbitrarily select $C_1 = C_2 = 0.1\,\mu\text{F}$, and size R_1 and R_2.
Ans. $R_1 = 100\,\text{k}\Omega$, $R_2 = 10\,\text{k}\Omega$

9.46 Find the transfer function for the circuit of Fig. 9-38, and explain the use of the circuit.
Ans. $T(s) = 1/(sRC + 1)$, a low-pass filter with zero output impedance

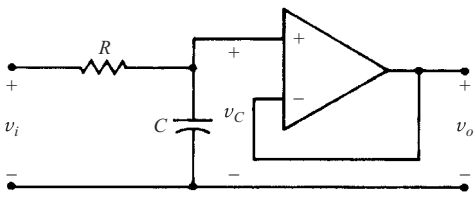


Fig. 9-38

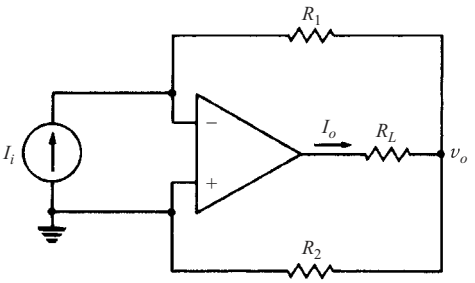


Fig. 9-39

9.47 For the circuit of Fig. 9-39, show that $I_o = -(1 + R_1/R_2)I_i$, so that the circuit is a true current amplifier. (Note that I_o is independent of R_L.)

9.48 If the noninverting terminal of the op amp in Fig. 9-29 is grounded, find the transfer function v_o/v_i. (Compare with Problem 9.22.) *Ans.* $v_o/v_i = -1$

9.49 Devise a method for using the inverting op amp circuit of Fig. 9-2 as a current source.
Ans. Let I_F be the output current; then $i_F = i_1 = v_S/R_1$ regardless of the value of R_F

9.50 A noninverting amplifier with gain $A_v = 21$ is desired. Based on ideal op amp theory, values of $R_1 = 10\,\text{k}\Omega$ and $R_2 = 200\,\text{k}\Omega$ are selected for the circuit of Fig. 9-3. If the op amp is recognized as nonideal in that $A_{OL} = -10^4$ and $\text{CMRR}_{db} = 40\,\text{db}$, find the actual gain $A_v = v_o/v_2$. *Ans.* $A_v = 21.17$

9.51 Use SPICE methods to simulate the differential amplifier of Fig. 9-12. Let $R_1 = R = 10\,\text{k}\Omega$ for a unity gain. Use the op amp model of Section 9.12. Apply signals $v_{S1} = \sin(2000\pi t)\,\text{V}$ and $v_{S2} = 2\sin(2000\pi t)\,\text{V}$ to show that the circuit is indeed a differential amplifier yielding $v_o = v_{S2} - v_{S1} = \sin(2000\pi t)\,\text{V}$. (*Netlist code available from author's website.*)

9.52 Use SPICE methods to simulate the circuit of Fig. 9-36 with values of Problem 9.39. Apply a 1-kHz sinusoidal source and verify that the input impedance $Z = 1256.7\angle 90^\circ = j2\pi(1000)(0.200)\,\Omega$; thus, the circuit does, in fact, simulate a 200-mH inductor as predicted by Problem 9.39. (*Netlist code available from author's website.*)

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CHAPTER 10

Switched Mode Power Supplies

10.1. INTRODUCTION

A *switched mode power supply* (SMPS) is a dc–dc converter with an unregulated input dc voltage and a regulated output voltage. The converter circuitry consists of arrangements of inductor, capacitors, diodes, and transistors. The transistors are switched between the ON state (saturation) and the OFF state (cutoff) at rates that typically range from 10 kHz to 40 kHz. Regulation of the output voltage is realized by control of the percentage of time that the transistor is in the ON state. The SMPS efficiency is significantly higher than that of the so-called linear power supplies that realize output voltage control by active region operation of the transistors.

The material of this chapter will be limited to steady-state operation covering the common case of continuous inductor current.

10.2. ANALYTICAL TECHNIQUES

Although numerous circuit topologies exist for SMPS, certain analysis techniques are universally applicable. Clear understanding of the results significantly simplifies analysis of the various SMPS arrangements. Notation adopted for analysis uses lowercase v and i for instantaneous values and upper case V and I for average values (dc quantities).

Inductor Voltage and Current

Consider the current i flowing through the inductor L of Fig. 10-1(a). If v_C changes insignificantly over an interval of interest (good approximation of C is sufficiently large) so that $v_C(t) \simeq V_C$, then

$$v_L(t) = V_B - V_C = L\frac{di}{dt} \tag{10.1}$$

Whence,

$$\int_{i(0)}^{i(t)} di = \frac{V_B - V_C}{L}\int_0^t dt$$

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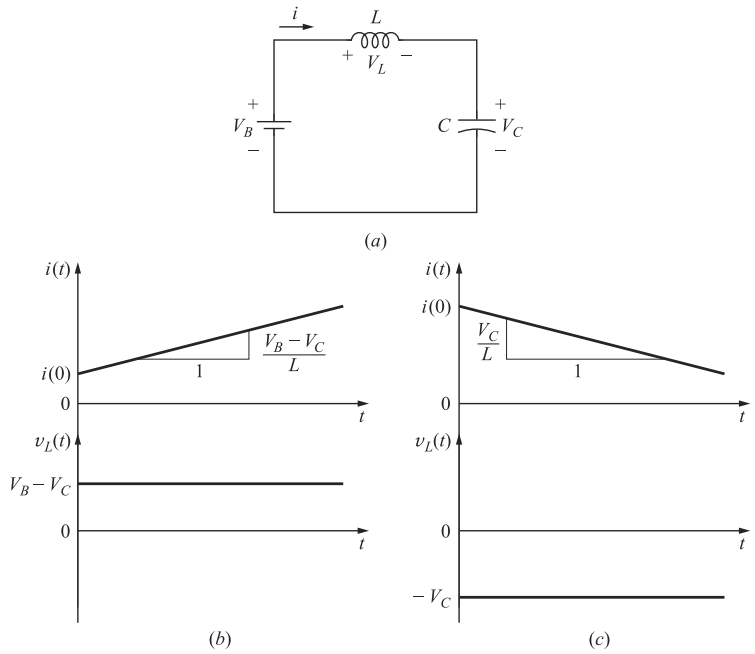


Fig. 10-1

or

$$i(t) = i(0) + \frac{V_B - V_C}{L}\, t \tag{10.2}$$

From (*10.1*) and (*10.2*), it is seen that the inductor voltage is constant and that the inductor current is a straight line segment as shown by Fig. 10-1(*b*).

Example 10.1. Let $V_B = 0$ and inductor current i have a nonzero initial value for the circuit of Fig. 10-1(*a*). Assume that v_C changes insignificantly over the interval of interest, and determine the nature of v_L and i.

By KVL,

$$v_L(t) = -V_C = L\,\frac{di}{dt} \tag{1}$$

From (*1*), it follows that

$$\int_{i(0)}^{i(t)} di = -\frac{V_C}{L}\int_0^t d\tau$$

or

$$i(t) = i(0) - \frac{V_C}{L}\, t \tag{2}$$

From (*1*) and (*2*) it is concluded that the inductor voltage is constant and that the inductor current is a straight line segment, as shown by Fig. 10-1(*c*).

Average Inductor Voltage

Consider the case of an inductor L that carries a periodic current $i_L(t)$, so that over a period T_s, $i_L(0) = i_L(T_s)$. The average value of inductor voltage is given by

$$V_L = \langle v_L \rangle = \frac{1}{T_s}\int_0^{T_s} v_L\, dt = \frac{1}{T_s}\int_0^{T_s}\left(L\,\frac{di_L}{dt}\right)dt = \frac{L}{T_s}\int_{i_L(0)}^{i_L(T_s)} di_L = 0 \tag{10.3}$$

As long as the inductor current i_L is periodic, the average value of voltage across the inductor is zero.

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Average Capacitor Current

Consider the case of a capacitor C for which the capacitor voltage $v_C(t)$ is periodic over T_s so that $v_C(0) = v_C(T_s)$. The average value of current through the capacitor is found as

$$I_C = \langle i_C \rangle = \frac{1}{T_s}\int_0^{T_s} i_C\,dt = \frac{1}{T_s}\int_0^{T_s}\left(C\,\frac{dv_C}{dt}\right)dt = \frac{C}{T_s}\int_{v_C(0)}^{v_C(T_s)} dv_C = 0 \qquad (10.4)$$

As long as the capacitor voltage v_C is periodic, the average value of current through the capacitor is zero.

10.3. BUCK CONVERTER

The SMPS circuit of Fig. 10-2, known as a *buck converter*, produces an average value output voltage $V_2 = \langle v_2 \rangle \le V_1$. The *duty cycle* D is defined as the ratio of the ON time of transistor Q to the *switching period* $T_s = 1/f_s$ (*switching frequency*). When the ideal transistor Q is ON, $v_D = V_1$. Conversely, when Q is OFF, continuity of current through inductor L requires that diode D be in the forward conducting state; thus, $v_D = 0$ for the ideal diode. Thus, v_D is a rectangular pulse of duration DT_s with period T_s.

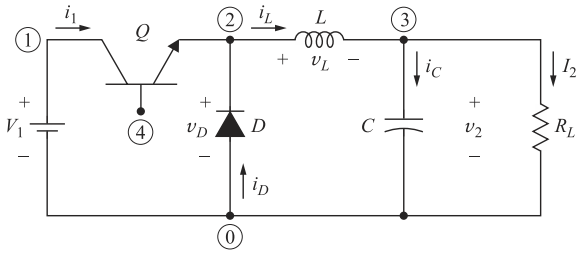


Fig. 10-2 Buck converter

If capacitor C is large, reasonable approximations are that the time-varying component of i_L flows through C and that the voltage across the load resistor R_L is constant. Since Q is switched periodically, voltage v_L and current i_C are periodic once initial transients die out.

As a consequence of the above approximations, v_L and i_L can be appropriately determined by (*10.1*) and (*10.2*), respectively, when Q is ON and by (*1*) and (*2*) of Example 10.1 when Q is OFF. Figure 10-3 displays the resulting waveforms for diode voltage v_D, inductor current i_L, inductor voltage v_L, and capacitor current i_C. The positive volt-second area of v_L must be equal in value to its negative volt-second area so that $\langle v_L \rangle = 0$. As a result of (*10.4*), current i_C must be the time-varying component of i_L.

Based on (*10.3*) and the v_L waveform of Fig. 10-3,

$$(V_1 - V_2)DT_s = V_2(1 - D)T_s$$

Rearrangement gives the buck converter voltage gain as

$$G_V = \frac{V_2}{V_1} = D \qquad (10.5)$$

The common case of continuous current i_L exists only if L is sized sufficiently large. Let $L = L_c$, the *critical inductance* that results in marginally continuous i_L. For this case, $I_{\min} = 0$ in Fig. 10-3. Since $i_L(0) = 0$, application of (*10.2*) yields

$$i_L(t) = \frac{V_1 - V_2}{L_c}\,t \qquad 0 \le t \le DT_s$$

Evaluate for $t = DT_s$ and use (*10.5*) to find

$$i_L(DT_s) = I_{\max} = \frac{V_1 - V_2}{L_c}\,DT_s = \frac{V_2(1 - D)T_s}{L_c}$$

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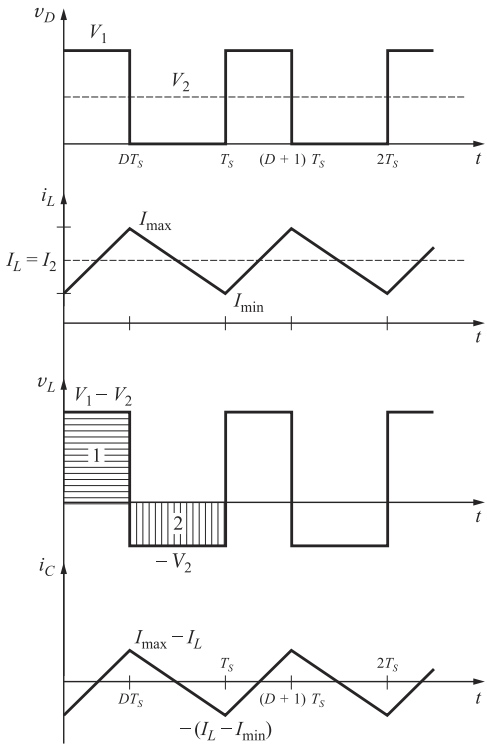


Fig. 10-3 Buck converter waveform

For this triangular waveform, under the assumption that the ac component of i_L flows through C and the dc component of i_L flows through R_L,

$$I_2 = \frac{1}{2} I_{max} = \frac{V_2(1-D)T_s}{2L_c}$$

However, $I_2 = V_2/R_L$ which can be equated to the above expression for I_2. Rearrangement of the result gives

$$L_c = \frac{R_L(1-D)T_s}{2} = \frac{R_L(1-D)}{2f_s} \tag{10.6}$$

Example 10.2. A buck converter having a switching frequency of 25 kHz is to be operated with a duty cycle such that $0.1 \le D \le 1$. The load is described by $R_L = 5\,\Omega$. Determine the value of critical inductance $L = L_c$ so that current i_L is continuous.

The critical inductance must be determined for the minimum value of duty cycle. By (*10.6*),

$$L_c = \frac{R_L(1-D)}{2f_s} = \frac{(5)(1-0.1)}{2(25\times 10^3)} = 90\,\mu\text{H}$$

10.4. BOOST CONVERTER

The *boost converter* SMPS circuit of Fig. 10-4 produces an average value output voltage $V_2 = \langle v_2 \rangle > V_1$. When the ideal transistor Q is ON, $v_Q = 0$. Conversely, when Q is OFF continuity of current through inductor L requires that ideal diode D be in the forward conducting state. With $v_D = 0$, $v_Q = V_2$. Thus, v_Q is a rectangular pulse with a delay of DT_s and duration $(1-D)T_s$.

If capacitor C is large, reasonable approximations are that the time-varying component of i_D flows through C and that the voltage across the load resistor R_L is constant. Due to periodic switching of Q, voltage v_L and current i_C are periodic once initial transients die out.

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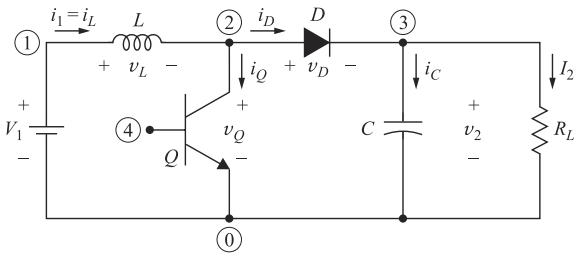


Fig. 10-4 Boost converter

As a consequence of the above approximations, v_L and i_L can be appropriately determined by (*10.1*) and (*10.2*) when Q is OFF and by (*1*) and (*2*) of Example 10.1 when Q is ON (replace V_C with $-V_1$). Diode current i_D must be equal to i_L when Q is OFF. Since load current I_2 is the average value of i_D, $i_C = i_D - I_2$. Figure 10-5 displays the resulting waveforms for v_Q, i_L, v_L, i_D, and i_C.

Based on (*10.3*) and the v_L waveform of Fig. 10-5,

$$V_1 DT_s = (V_2 - V_1)(1 - D)T_s$$

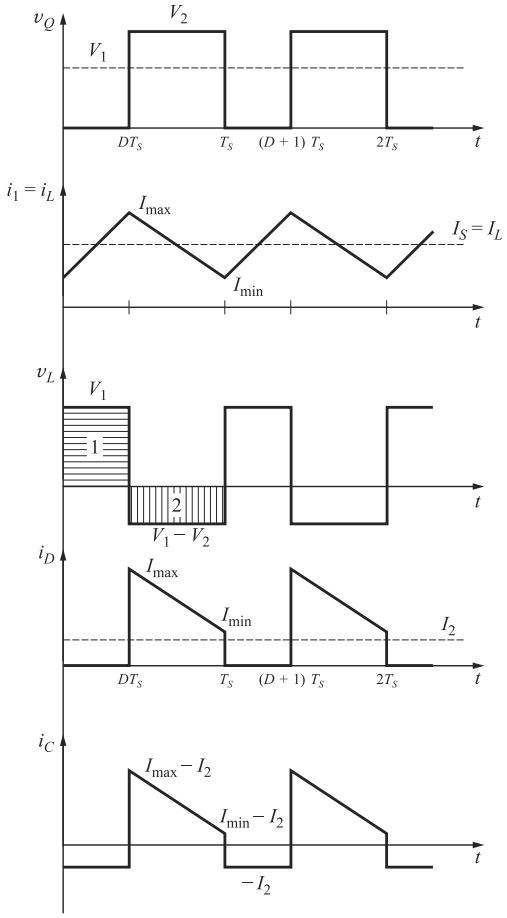


Fig. 10-5 Boost converter waveform

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Rearrangement finds the ideal boost converter voltage gain as

$$G_V = \frac{V_2}{V_1} = \frac{1}{1-D} \tag{10.7}$$

Unlike the buck converter, the boost converter gain is not a linear function of D. From (*10.7*), the ideal gain approaches infinity as D approaches 1. When parasitic resistances of the inductor and capacitor are considered, the actual gain (G_V') departs significantly from the ideal gain for values of $D > 0.8$. (See Problem 10.11.)

The common case of continuous current i_L exists only if the value of $L \geq L_c$ (critical inductance) that results in marginally continuous conduction for i_L. For this case, $I_{\min} = 0$ in Fig. 10-5 and $i_L(0) = 0$. By application of (*10.2*),

$$i_L(t) = \frac{V_1}{L_c}\, t \qquad 0 \leq t \leq DT_s$$

Evaluate for $t = DT_s$ and use (*10.7*) to find

$$i_L(DT_s) = i_D(DT_s) = I_{\max} = \frac{V_1}{L_c}\, DT_s = \frac{V_2(1-D)}{L_c}\, DT_s$$

For the triangular i_D waveform,

$$I_2 = \langle i_D \rangle = \frac{1}{2}\, I_{\max}\, \frac{(1-D)T_s}{T_s} = \frac{V_2}{2L_c}\, D(1-D)^2 T_s$$

But $I_2 = V_2/R_L$, which can be equated to the above expression for I_2. After rearrangement,

$$L_c = \frac{(1-D)^2 DT_s R_L}{2} = \frac{(1-D)^2 DR_L}{2f_s} \tag{10.8}$$

Example 10.3. A boost converter with a 20-kHz switching frequency is operating with a 50 percent duty cycle. The connected load is 7 Ω. Determine the value of critical inductance so that current i_L is continuous.

By (*10.8*),

$$L_c = \frac{(1-D)^2 DR_L}{2f_s} = \frac{(1-0.5)^2(0.5)(7)}{2(20 \times 10^3)} = 21.9\,\mu\text{H}$$

10.5. BUCK-BOOST CONVERTER

The SMPS circuit of Fig. 10-6 is a *buck-boost converter*. The value of output voltage for this converter may either be less than or greater than the input voltage, depending on the value of duty cycle D. Unlike the buck and boost converters, the buck-boost converter produces an output voltage with polarity opposite to input voltage V_1. The polarity of v_2 and the direction of I_2 in Fig. 10-6 are chosen so that $V_2 = \langle v_2 \rangle \geq 0$ and $I_2 \geq 0$.

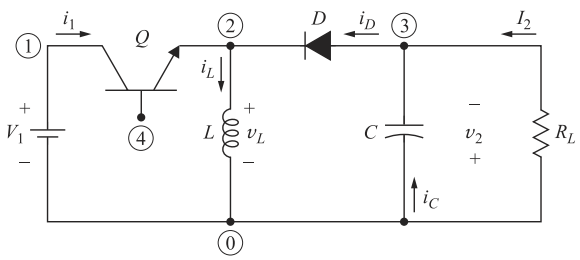


Fig. 10-6 Buck-boost converter

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For a large value of capacitor C, reasonable approximations are that the time-varying component of i_D flows through C and that the voltage across R_L is constant. For periodic switching of Q, voltage v_L and current i_C are periodic after initial transients subside.

As a direct consequence of the preceding approximations, v_L and i_L can be appropriately determined by (*10.1*) and (*10.2*) when Q is ON (let $V_C = 0$) and by (*1*) and (*2*) of Example 10.1 when Q is OFF. Since load current I_2 is the average value of i_D, $i_C = i_D - I_2$. Figure 10-7 shows sketches of the resulting waveforms for v_L, i_L, i_C, and i_D.

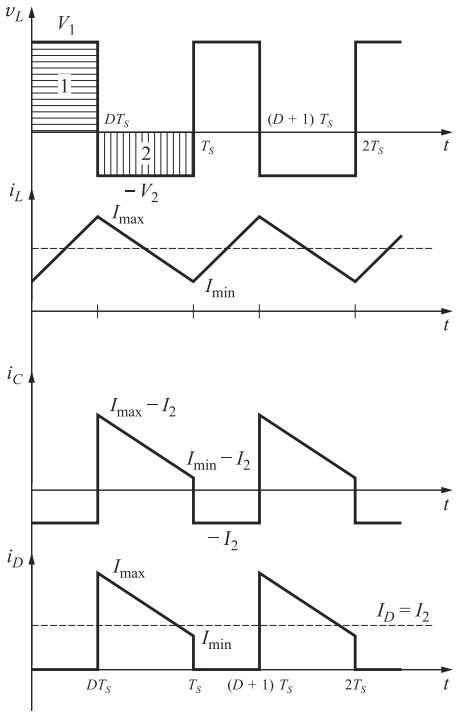


Fig. 10-7 Buck-boost converter waveforms

Based on (*10.3*) and the v_L waveform of Fig. 10-7,

$$V_1 DT_s = V_2(1 - D)T_s$$

Rearrangement gives the ideal buck-boost converter voltage gain as

$$G_V = \frac{V_2}{V_1} = \frac{D}{1 - D} \tag{10.9}$$

As with the boost converter, the buck-boost converter gain is not a linear function of duty cycle D. Further, (*10.9*) shows that the ideal gain G_V approaches infinity as D approaches 1. When parasitic resistances of the inductor and capacitor are considered, the actual gain (G_V') departs significantly from the ideal gain for values of $D > 0.75$. (See Problem 10.14.)

The common case of continuous current i_L exists only if the value of $L \geq L_c$ (critical inductance) that results in marginally continuous conduction for i_L. For such case, $I_{\min} = 0$ in Fig. 10-7 and $i_L(0) = 0$. By application of (*10.2*),

$$i_L(t) = \frac{V_1}{L_c}\, t \qquad 0 \leq t \leq DT_s$$

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Evaluate for $t = DT_s$ and use (*10.9*) to yield

$$I_{\max} = i_L(DT_s) = \frac{V_1}{L_c}\, DT_s = \frac{V_2(1-D)}{L_c}\, T_s$$

For the triangular waveform of i_D,

$$I_2 = \langle i_D \rangle = \frac{1}{2}\, I_{\max}\, \frac{(1-D)T_s}{T_s} = \frac{V_2}{2L_c}\,(1-D)^2 T_s$$

But $I_2 = V_2/R_L$ which can be equated to the above expression for I_2. After rearrangement,

$$L_c = \frac{(1-D)^2 T_s R_L}{2} = \frac{(1-D)^2 R_L}{2f_s} \tag{10.10}$$

Example 10.4. A buck-boost converter with a 30-kHz switching frequency is operating with $D = 0.25$. The connected load is described by $R_L = 10\,\Omega$. Find the value of critical inductance so that i_L is continuous.

By (*10.10*),

$$L_c = \frac{(1-D)^2 R_L}{2f_s} = \frac{(1-0.25)^2(10)}{2(30 \times 10^3)} = 93.75\,\mu\text{H}$$

10.6. SPICE ANALYSIS OF SMPS

For simulation of near ideal (lossless) SMPS, the switch element Q can readily be modeled using the PSpice voltage-controlled switch. The element specification statement for the voltage-controlled switch has the form

$$\text{S}\cdots n_1 \;\; n_2 \;\; c_1 \;\; c_2 \;\; \text{VCS}$$

Any alpha-numeric combination suffix can follow S to uniquely specify the voltage-controlled switch. The nodes are clarified by Fig. 10-8. A fast rise and fall time (5 ns), 1-V pulse should be used for the control voltage v_{SW}. Accepting the default ON state and OFF state control voltages of 1 V and 0 V, respectively, results in duty cycle ON time approximately equal to the pulse duration. For minimum

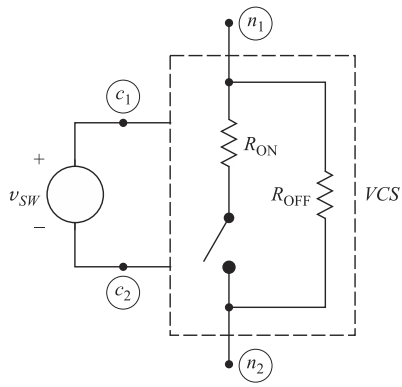


Fig. 10-8 Voltage-controlled switch

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conduction losses, the ON state resistance of the voltage-controlled switch should be specified in the .MODEL statement by

.MODEL VCS VSWITCH (RON = 1e-6)

Example 10.5. Use SPICE methods to model the buck converter of Fig. 10-2; let $D = 0.5$, $f_s = 25\,\text{kHz}$, $L = 100\,\mu\text{H}$, $C = 50\,\mu\text{F}$, and $R_L = 5\,\Omega$. Generate the set of waveforms analogous to Fig. 10-3.

The netlist code follows, where the initial conditions on inductor current and capacitor voltage were determined after running a large integer number of cycles to find the repetitive values.

```
Ex10_5.CIR
* BUCK CONVERTER
* D=DUTY CYCLE, fs=SWITCHING FREQUENCY
.PARAM D=0.5 fs=25e3Hz
V1   1 0 DC 12V
SW   1 2 4 2 VCS
VSW 4 2 PULSE(0V 1V 0s 5ns 5ns {D/fs} {1/fs})
L    2 3 100uH IC=0.6A
D    0 2 DMOD
C    3 0 50uF IC=6V
RL   3 0 5ohm
.MODEL DMOD D(N=0.01)
.MODEL VCS VSWITCH (RON=1e-6ohm)
.TRAN 5us 0.2ms 0s 100ns UIC
.PROBE
.END
```

Execute ⟨Ex10_5.CIR⟩ and use the Probe feature of PSpice to plot the waveforms of Fig. 10-9.

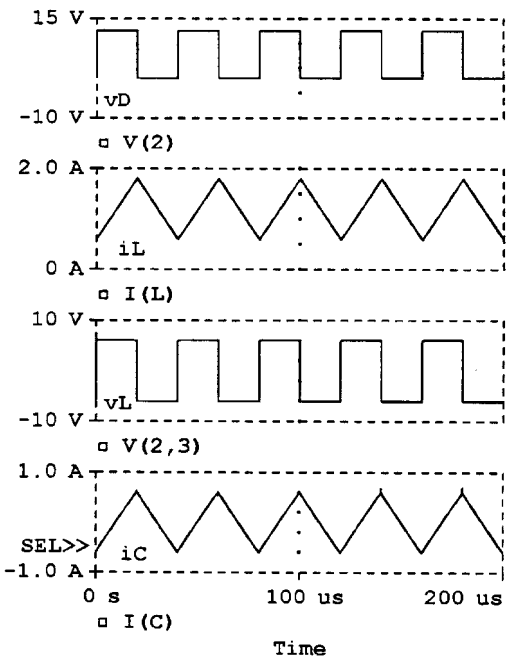


Fig. 10-9

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Solved Problems

10.1 A lossless buck converter supplies an average power of 20 W to a load with a regulated 12-V output while operating at a duty cycle of 0.8 with continuous inductor current. Find the average values of (*a*) input voltage and (*b*) input current.

(*a*) By (*10.5*),

$$V_1 = \frac{V_2}{D} = \frac{12}{0.8} = 15\,\text{V}$$

(*b*) Since the converter is lossless, output power is equal to input power; thus,

$$V_1 I_1 = P_o = P_{in}$$

or

$$I_1 = \frac{P_o}{V_1} = \frac{20}{15} = 1.333\,\text{A}$$

10.2 A buck converter is connected to a 7 Ω load. Inductor $L = 50\,\mu\text{H}$ and the switching frequency $f_s = 30\,\text{kHz}$. Determine the smallest value of duty cycle possible if the inductor current is continuous.

Solve (*10.6*) for D to find

$$D = D_{\min} = 1 - \frac{2f_s L_c}{R_L} = 1 - \frac{2(30 \times 10^3)(50 \times 10^{-6})}{7} = 0.4286$$

10.3 Assume the buck converter of Fig. 10-2 is lossless so that the input power (P_{in}) is equal to the output power (P_o). Derive an expression for the current gain $G_I = I_2/I_1$.

The input power and output power are found by use of (*1.20*).

$$P_{in} = \frac{1}{T_s}\int_0^{T_s} V_1 i_1\,dt = V_1\,\frac{1}{T_s}\int_0^{T_s} i_1\,dt = V_1 I_1 \qquad (1)$$

$$P_o = \frac{1}{T_s}\int_0^{T_s} v_2 i_2\,dt = V_2 I_2\,\frac{1}{T_s}\int_0^{T_s} dt = V_2 I_2 \qquad (2)$$

Constant values for v_2 and i_2 were assumed in (*2*). Equate (*1*) and (*2*). Rearrange the result and use (*10.5*) to find

$$G_I = \frac{I_2}{I_1} = \frac{V_1}{V_2} = \frac{1}{D}$$

10.4 A buck converter is fed from a 12-V dc source. It supplies a regulated 5 V to a connected 5 Ω load. The inductor current is continuous. Determine (*a*) the duty cycle and (*b*) the output power.

(*a*) Based on (*10.5*),

$$D = \frac{V_2}{V_1} = \frac{5}{12} = 0.4167$$

(*b*) By (*1.23*),

$$P_o = \frac{V_2^2}{R_L} = \frac{(5)^2}{5} = 5\,\text{W}$$

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10.5 Sketch the source current i_1 and the diode current i_D for the buck converter of Fig. 10-2 with continuous inductor current.

When Q is ON, $i_1 = i_L$ and $i_D = 0$. If Q is OFF, $i_1 = 0$ and $i_D = i_L$. From these observations, the current i_1 and i_D can be sketched based on Fig. 10-3. The results are shown in Fig. 10-10.

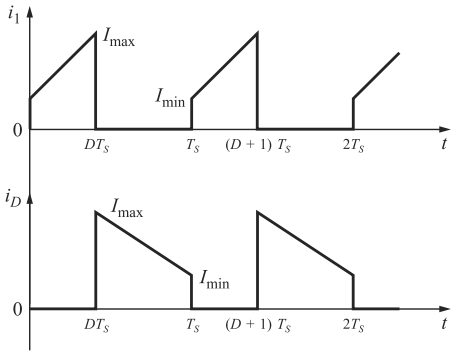


Fig. 10-10

10.6 Determine a set of equations that describe the instantaneous inductor current $i_L(t)$ over a period T_s for the buck converter.

Refer to i_L and v_L of Fig. 10-3. For $0 \le t \le DT_s$, application of (*10.2*) gives

$$i_L(t) = I_{\min} + \frac{V_1 - V_2}{L}\, t \tag{1}$$

For $DT_s \le t \le T_s$, create a t'-coordinate frame with origin at $t = DT_s$ so that $t' = t - DT_s$. In the t' frame, application of (*2*) from Example 10.1 yields

$$i_L(t') = I_{\max} - \frac{V_2}{L}\, t' = I_{\max} - \frac{V_2}{L}\,(t - DT_s) \tag{2}$$

To complete the work, expressions for $I_{\max}$ and $I_{\min}$ must be found. Evaluate (*1*) for $t = DT_s$ to find

$$i_L(DT_s) = I_{\max} = I_{\min} + \frac{V_1 - V_2}{L}\, DT_s \tag{3}$$

Since $\langle i_L \rangle = I_L = I_2$, and since the i_L waveform of Fig. 10-3 is made up of straight line segments,

$$I_2 = \frac{I_{\max} + I_{\min}}{2} = \frac{V_2}{R_L} \tag{4}$$

Simultaneous solution of (*3*) and (*4*) result in

$$I_{\max} = \frac{V_2}{R_L} + \frac{(V_1 - V_2)D}{2f_sL} \tag{5}$$

$$I_{\min} = \frac{V_2}{R_L} - \frac{(V_1 - V_2)D}{2f_sL} \tag{6}$$

where $f_s = 1/T_s$.

10.7 Find the maximum and minimum values of the inductor current for the buck converter of Problem 10.2 if the duty cycle $D = 0.6$ and $V_1 = 24\,\text{V}$.

Since $D = 0.6 > D_{\min} = 0.4286$, continuous inductor current is assured. Also, by (*10.5*),

$$V_2 = DV_1 = 0.6(24) = 14.4\,\text{V}$$

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By (5) and (6) of Problem 10.6,

$$I_{\max} = \frac{V_2}{R_L} + \frac{(V_1 - V_2)D}{2f_s L} = \frac{14.4}{7} + \frac{(24 - 14.4)(0.6)}{2(30 \times 10^3)(50 \times 10^{-6})} = 3.977\,\text{A}$$

$$I_{\min} = \frac{V_2}{R_L} - \frac{(V_1 - V_2)D}{2f_s L} = \frac{14.4}{7} - \frac{(24 - 14.4)(0.6)}{2(30 \times 10^3)(50 \times 10^{-6})} = 0.137\,\text{A}$$

10.8 For work to this point, the output voltage of the buck converter has been assumed constant ($v_2 \simeq V_2$) for sufficiently large values of C; however, since i_C is a time-varying quantity, v_2 does display a small peak-to-peak ripple Δv_2. Use the change in capacitor charge (Q_C), under the assumption that the time-varying component of i_L flows through C, to calculate the voltage ripple Δv_2 for the case of continuous inductor current.

Since $v_2 = Q_C/C$, the total increment in v_2 is

$$\Delta v_2 = \Delta Q_C / C \tag{1}$$

The total increment in charge Q_C is given by the half-period duration amp-second, triangle-shaped area of i_L above $I_2 = I_L$ in Fig. 10-3.

$$\Delta Q_C = \frac{1}{2}(I_{\max} - I_2)\,\frac{T_s}{2} \tag{2}$$

Use $I_2 = V_2/R_L$ and (5) of Problem 10.6 in (2) and substitute the result into (1) to yield the peak-to-peak ripple voltage.

$$\Delta v_2 = \frac{1}{C}\left(\frac{1}{2}\right)\frac{(V_1 - V_2)D}{2f_s L}\,\frac{T_s}{2} \tag{3}$$

From (*10.5*), $V_1 = V_2/D$. Substitute into (3), use $T_s = 1/f_s$, and rearrange to find

$$\Delta v_2 = \frac{(1 - D)V_2}{8f_s^2 LC} \tag{4}$$

10.9 For the buck converter of Example 10.5, (*a*) calculate the percent voltage ripple by (4) of Problem 10.8 and (*b*) formulate a SPICE simulation to numerically determine the percentage ripple.

(*a*) By (4) of Problem 10.8 with the values of Example 10.5 and using (*10.5*),

$$\frac{\Delta v_2}{V_2} = \frac{(1 - D)}{8f_s^2 LC}\,100\% = \frac{(1 - 0.5)}{8(25 \times 10^3)^2(100 \times 10^{-6})(50 \times 10^{-6})}\,100\% = 2\%$$

(*b*) Execute ⟨Ex10_5.CIR⟩ and use the Probe feature of PSpice to plot $v_2 = \text{V(3)}$ with marked values shown in Fig. 10-11. Then,

$$V_2 \simeq \frac{6.064 + 5.943}{2} = 6.0035$$

$$\Delta v_2 = 6.064 - 5.943 = 0.121$$

$$\frac{\Delta v_2}{V_2} = \frac{0.121}{6.0035}\,100\% = 2.01\%$$

The error in the two methods is much less than 1 percent.

10.10 A boost converter with continuous inductor current is fed from a 12-V source with a 60 percent duty cycle while supplying a power of 60 W to the connected load. Determine (*a*) the output voltage, (*b*) the load resistance, and (*c*) the load current.

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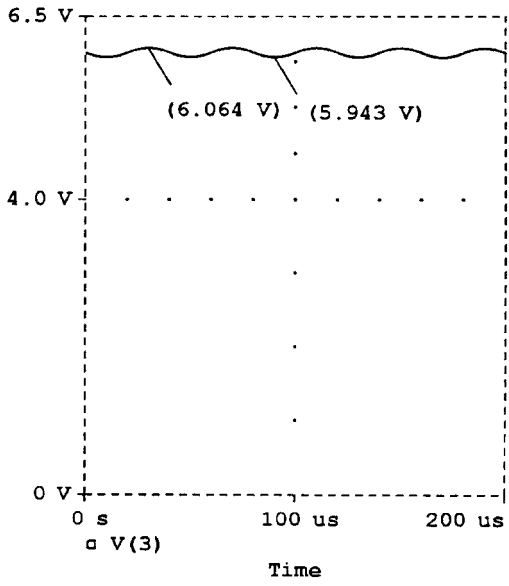


Fig. 10-11

(*a*) By (*10.7*),

$$V_2 = \frac{V_1}{1-D} = \frac{12}{1.06} = 30\,\text{V}$$

(*b*) Based on (*1.23*),

$$R_L = \frac{V_2^2}{P_o} = \frac{(30)^2}{60} = 15\,\Omega$$

(*c*) By Ohm's law,

$$I_2 = \frac{V_2}{R_L} = \frac{30}{15} = 2\,\text{A}$$

10.11 Let R_x be the inherent resistance of the inductor L for the boost converter of Fig. 10-4 and derive an expression for the actual voltage gain ($G_V' = V_2/V_1$) that is valid for continuous inductor current. Treat V_2 as constant in value. Assume that i_L can be described by straight line segments.

Figure 10-12(*a*) represents the circuit of Fig. 10-4 with Q ON and D OFF from which KVL gives

$$L\frac{di_L}{dt} + R_x i_L = V_1 \qquad 0 \le t \le DT_s \tag{1}$$

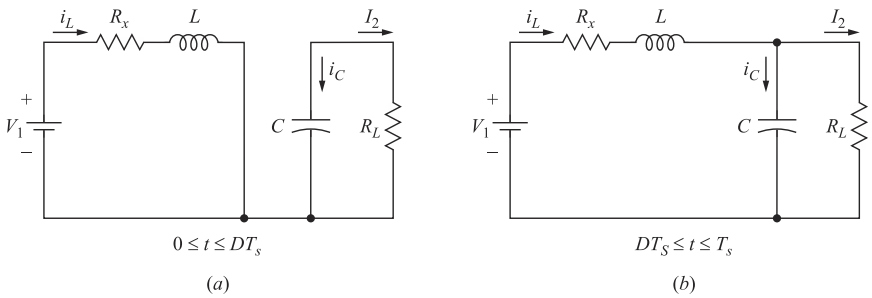


Fig. 10-12

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The equivalent circuit of Fig. 10-12(*b*) is valid for Q OFF and D ON, yielding

$$L\frac{di_L}{dt} + R_x I_L = V_1 - V_2 \qquad DT_s \le t \le T_s \tag{2}$$

Integrate both (*1*) and (*2*) over their time regions of validity to give

$$L\int_{i_L(0)}^{i_L(DT_s)} di_L + R_x \int_0^{DT_s} dt = V_1 \int_0^{DT_s} dt \tag{3}$$

$$L\int_{i_L(DT_s)}^{i_L(T_s)} di_L + R_x \int_{DT_s}^{T_s} dt = V_1 \int_{DT_s}^{T_s} dt - V_2 \int_{DT_s}^{T_s} dt \tag{4}$$

Add (*3*) and (*4*) and divide by T_s to find

$$\frac{L}{T_s}\int_{i_L(0)}^{i_L(T_s)} di_L + R_x \frac{1}{T_s}\int_0^{T_s} i_L\, dt = \frac{V_1}{T_s}\int_0^{DT_s} dt - \frac{V_2}{T_s}\int_{DT_s}^{T_s} dt \tag{5}$$

If i_L is periodic, $i_L(0) = i_L(T_s)$. Hence, the first term of (*5*) has a value of zero. The second term is $R_x\langle i_L\rangle = R_x I_L$. Thus, (*5*) can be written as

$$R_x I_L = V_1 - (1-D)V_2 \tag{6}$$

From the waveform sketch of Fig. 10-5,

$$I_2 = \frac{1}{T_s}\int_{DT_s}^{T_s} i_L\, dt$$

Since i_L is described by straight line segments, it follows that

$$I_2 T_s = I_L(1-D)T_s$$

or

$$I_L = \frac{I_2}{1-D} = \frac{V_2}{R_L(1-D)} \tag{7}$$

Substitute (*7*) into (*6*) and rearrange to yield

$$G_V' = \frac{V_2}{V_1} = \frac{(1-D)R_L}{R_x + R_L(1-D)^2} \tag{8}$$

10.12 Use SPICE methods to model the boost converter of Fig. 10-4 with $f_s = 20\,\text{kHz}$, $D = 0.25$, $L = 50\,\mu\text{H}$, $C = 100\,\mu\text{F}$, and $R_L = 7.5\,\Omega$. From the model, generate a set of waveforms analogous to Fig. 10-5.

The netlist code is shown below where the initial conditions on inductor current and capacitor voltage were determined after running a large integer number of cycles to find the repetitive values.

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```
Prb10_12.CIR
* BOOST CONVERTER
* D=DUTY CYCLE, fs=SWITCHING FREQUENCY
.PARAM D=0.25 fs=20e3Hz
V1   1 0 DC 15V
SW   2 0 4 0 VCS
VSW 4 0 PULSE(0V 1V 0s 5ns 5ns {D/fs} {1/fs})
L    1 2 50uH IC=1.657A
D    2 3 DMOD
C    3 0 100uF IC=20.05V
RL   3 0 7.5ohm
.MODEL DMOD D(N=0.01)
.MODEL VCS VSWITCH(RON=1e-6ohm)
.TRAN 1us 0.25ms 0s 100ns UIC
.PROBE
.END
```

Execute ⟨Prb10_12.CIR⟩ and use the Probe feature of PSpice to plot the waveforms shown in Fig. 10-13.

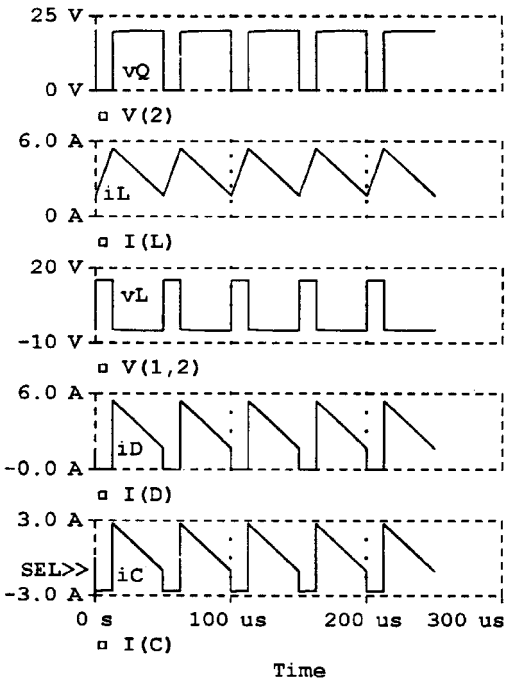


Fig. 10-13

10.13 A lossless buck-boost converter with continuous inductor current supplies a 10 Ω load with a regulated output voltage of 15 V. The input voltage is 12 V. Determine the value of (*a*) duty cycle, (*b*) input power, and (*c*) average value of input current.

(*a*) Solve (*10.9*) for D to find

$$D = \frac{V_2}{V_1 + V_2} = \frac{15}{12 + 15} = 0.5555$$

(*b*) Based on (*1.23*) for this lossless converter,

$$P_{in} = P_o = \frac{V_2^2}{R_L} = \frac{(15)^2}{10} = 22.5\,\text{W}$$

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(*c*) The average value of input current follows as

$$I_1 = \frac{P_{in}}{V_1} = \frac{22.5}{12} = 1.875\,\text{A}$$

10.14 If R_x is the inherent resistance of the inductor L for the buck-boost converter of Fig. 10-6, derive an expression for the actual voltage gain ($G_V' = V_2/V_1$) that is valid for continuous inductor current. Assume that i_L is described by straight line segments.

The circuit of Fig. 10-14(*a*) represents the circuit of Fig. 10-6 with Q ON and D OFF. By KVL,

$$L\frac{di_L}{dt} + R_x I_L = V_1 \qquad 0 \le t \le DT_s \tag{1}$$

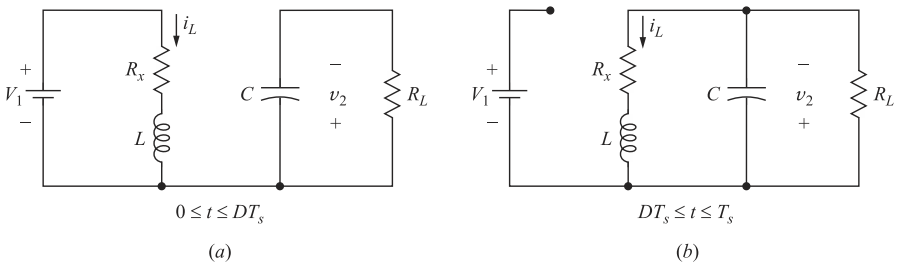


Fig. 10-14

The circuit of Fig. 10-14(*b*) is valid for Q OFF and D ON. Whence,

$$L\frac{di_L}{dt} + R_x i_L = -v_2 \qquad DT_s \le t \le T_s \tag{2}$$

In similar manner to the procedure of Problem 10.11, integrate (*1*) and (*2*), add the results, and divide by T_s to find

$$\frac{L}{T_s}\int_{i_L(0)}^{i_L(T_s)} di_L + R_x\frac{1}{T_s}\int_0^{T_s} i_L\,dt = \frac{V_1}{T_s}\int_0^{DT_s} dt - \frac{1}{T_s}\int_{DT_s}^{T_s} v_s\,dt \tag{3}$$

For a periodic i_L, the first term of (*3*) must be zero. Recognize the average values of i_L and v_2, respectively, in the second term on each side of the equation to give

$$R_x I_L = DV_1 - (1-D)V_2 \tag{4}$$

From Fig. 10-14,

$$C\frac{dv_2}{dt} = -\frac{v_2}{R_L} \qquad 0 \le t \le DT_s \tag{5}$$

$$C\frac{dv_2}{dt} = i_L - \frac{v_2}{R_L} \qquad DT_s \le t \le T_s \tag{6}$$

Integrate, add, and divide by T_s for (*5*) and (*6*).

$$\frac{C}{T_s}\int_{v_2(0)}^{v_2(T_s)} dv_2 = \frac{1}{T_s}\int_{DT_s}^{T_s} i_L\,dt - \frac{1}{R}\frac{1}{T_s}\int_0^{T_s} v_2\,dt \tag{7}$$

The first term of (*7*) must be zero for periodic v_2. Owing to the straight-line segment description of i_L, the first term on the right-hand side of (*7*) can be written as $(1-D)I_L$. Recognize the average value of v_2 in the last term. Thus, (*7*) becomes

$$0 = (1-D)I_L - \frac{V_2}{R_L} \tag{8}$$

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Solve (*8*) for I_L, substitute the result into (*4*), and rearrange to yield

$$G'_V = \frac{V_2}{V_1} = \frac{D(1-D)R_L}{R_x + (1-D)^2 R_L} \tag{9}$$

10.15 By SPICE methods, model the buck-boost converter of Fig. 10-6 with $f_s = 30\,\text{kHz}$, $D = 0.4$, $L = 70\,\mu\text{H}$, $C = 100\,\mu\text{F}$, and $R_L = 10\,\Omega$. Use the model to generate a set of waveforms analogous to Fig. 10-7.

The netlist code is shown below where the initial conditions on inductor current and capacitor voltage were determined after running a large integer number of cycles to find the repetitive values.

```
Prb10_15.CIR
* BUCK-BOOST CONVERTER
* D=DUTY CYCLE, fs=SWITCHING FREQUENCY
.PARAM D=0.4 fs=30e3Hz
V1   1 0 DC 15V
SW   1 2 4 2 VCS
VSW 4 2 PULSE(0V 1V 0s 5ns 5ns {D/fs} {1/fs})
L    2 0 70uH IC=0.229A
D    3 2 DMOD
C    0 3 100uF IC=10.02V
RL   0 3 10ohm
.MODEL DMOD D(N=0.01)
.MODEL VCS VSWITCH(RON=1e-6ohm)
.TRAN 1us 0.166667ms 0s 100ns UIC
.PROBE
.END
```

Execute ⟨Prb10_15.CIR⟩ and use the Probe feature of PSpice to plot the waveforms of Fig. 10-15.

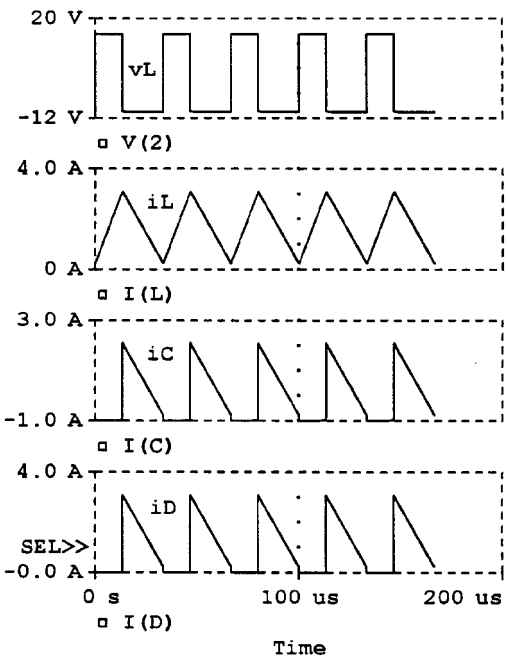


Fig. 10-15

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Supplementary Problems

10.16 Determine the smallest value of inductance that could have been used for the buck converter of Example 10.5 and the inductor current remain continuous. *Ans.* $L = L_c = 50\,\mu\text{H}$

10.17 Find the values of $I_{\max}$ and $I_{\min}$ for the buck converter of Example 10.5 if the value of $L = L_c = 50\,\mu\text{H}$, as determined in Problem 10.16. *Ans.* $I_{\max} = 2.4\,\text{A}$; $I_{\min} = 0$

10.18 Use the procedure of Problem 10.3 to find an expression for the current gain $G_I = I_2/I_1$ for the ideal boost converter of Fig. 10-4. *Ans.* $G_I = 1 - D$

10.19 Use Problem 10.6 as a guideline to derive expressions for $I_{\max}$ and $I_{\min}$ shown on the boost converter waveforms of Fig. 10-5.

Ans. $I_{\max} = \dfrac{V_2}{(1-D)R_L} + \dfrac{V_1 D}{2f_s L}$; $\quad I_{\min} = \dfrac{V_2}{(1-D)R_L} - \dfrac{V_1 D}{2f_s L}$

10.20 The actual gain G_V' for the boost converter with inherent inductor resistance was determined in Problem 10.11. Determine the duty cycle $D = D_p$ for which G_V' has a maximum value.
Ans. $D_p = 1 - \sqrt{R_x/R_L}$

10.21 Find an expression for the peak-to-peak ripple voltage of a boost converter.
Ans. $\Delta v_2 = DV_2/(f_s R_L C)$

10.22 Execute ⟨Prb10_12.CIR⟩ of Problem 10.12 and plot $v_2 = \text{V}(3)$. From the plot, determine the peak-to-peak ripple voltage Δv_2. *Ans.* $\Delta v_2 \simeq 0.383\,\text{V}$

10.23 Determine the smallest value of inductance that could have been used for the buck-boost converter of Problem 10.15 and the inductor current remain continuous. *Ans.* $L = L_c = 24\,\mu\text{H}$

10.24 The actual gain G_V' for the buck-boost converter with inherent inductor resistance was determined in Problem 10.14. Determine the duty cycle $D = D_p$ for which G_V' has a maximum value.

Ans. $D_p = \left(1 + \dfrac{R_x}{R_L}\right) - \left[\dfrac{R_x}{R_L}\left(1 + \dfrac{R_x}{R_L}\right)\right]^{1/2}$

10.25 Use the procedure of Problem 10.3 to find an expression for the current gain $G_I = I_2/I_1$ for the ideal buck-boost converter of Fig. 10-6. *Ans.* $G_I = (1 - D)/D$

10.26 Show that the expressions for $I_{\max}$ and $I_{\min}$ shown on the buck-boost converter waveforms of Fig. 10-7 are identical to those determined for the boost converter in Problem 10.19.

10.27 Execute ⟨Prb10_15.CIR⟩ of Problem 10.15 and plot $v_2 = -\text{V}(3)$. From the plot, determine peak-to-peak ripple voltage Δv_2. *Ans.* $\Delta v_2 \simeq 0.153\,\text{V}$

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